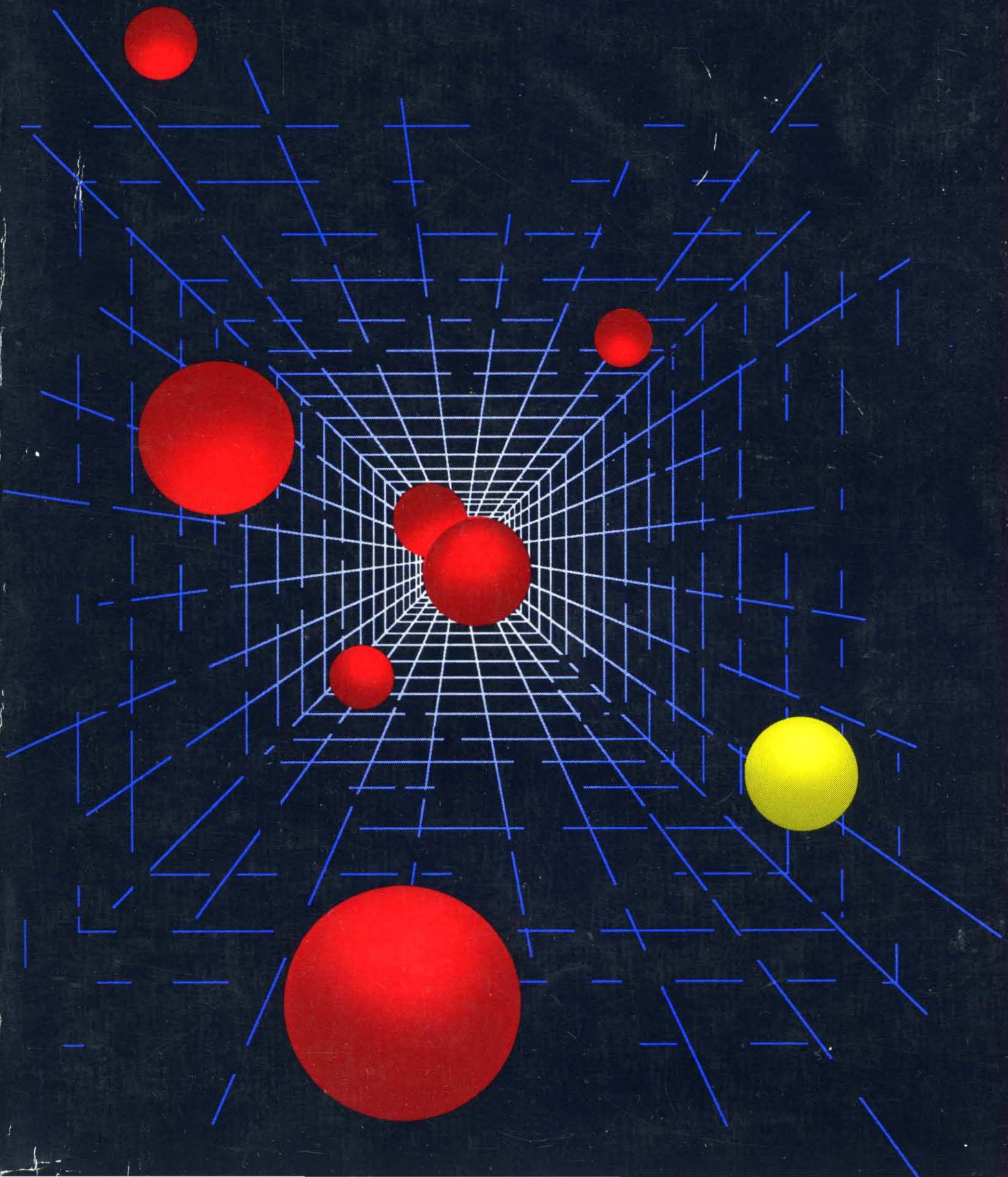
8/16-Bit Microprocessors Microcomputers Peripherals



1987 Data Book

FUJITSU

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8 / 16-Bit Microprocessors Microcomputers Peripherals

1987 Data Book

Fujitsu Limited

Fujitsu Microelectronics, Inc.

Fujitsu Mikroelektronik GmbH

Fujitsu Microelectronics Pacific Asia Ltd.

Worldwide Suppliers of Communications
and Electronics Equipment

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Edition 1.0

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is Japan's largest supplier of computers and ranks in the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors. Fujitsu operates subsidiaries worldwide in two dozen countries and employs over 80,000 people to generate annual sales in excess of nine billion US dollars. (Year ended March 31, 1986 consolidated base.)

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and Europe to help meet the growing worldwide demand for Fujitsu semiconductor products. In all, Fujitsu operations occupy over 1.6 million square meters of manufacturing space worldwide.

Semiconductor Products

In 1975, Fujitsu developed 8-bit microcomputers. In 1977, Fujitsu introduced proprietary 4-bit microcomputers. Today, their 4-bit microcomputer family is the largest 4-bit product line in the world. With the development of the high performance 16-bit micropcocessors, Fujitsu offers a full line of microprocessors, microcomputers, and peripherals to provide designers with a total of 150 products, including 90 products in CMOS families, 50 products in NMOS families and 10 products in bipolar peripherals.

In 1983, Fujitsu introduced the world's first CMOS single-chip Digital Signal Processor, the MB8764. Fujitsu's DSP provides telecommunication designers with high-speed signal processing capabilities and at a cost-effective solution.

Other Fujitsu industry standard products include GaAs FETs, GaAs FET amplifiers, Si microwave transistors and light wave semiconductors. Discrete products include power-switching transistors and Darlington Array transistors.

Fujitsu's custom product lines include application-specific gate arrays and standard-cell arrays using high-speed Bipolar and ECL technologies and advanced CMOS technologies. Gate arrays ranging in size from 350 to 20,000 gates are available in up to 8,000 gate equivalents and include on-chip memory and program logic array.

Virtually every major type of electronics equipment on the globe utilizes Fujitsu technology in integrated circuits. Fujitsu's leadership position in worldwide integrated circuit development and manufacturing assures equipment manufacturers that they will always be able to design with the latest in technology utilizing the highest standards of quality and reliability.

Fujitsu Microelectronics, Inc.

Established in 1979, Fujitsu Microelectronics, Inc., headquartered in Santa Clara, California, markets Fujitsu semiconductors through representatives located throughout the U.S. and North America.

The Component Division, Fujitsu Component of America, Inc., markets bubble memories, keyboards, plasma displays, relay switches and hybrid ICs.

FMI's San Diego manufacturing facility provides capacity for manufacturing of many high-technology devices for the U.S. and North American market.

Customer support for custom designs is available through Fujtsu's design centers in Santa Clara, Dallas and Boston. Technology Centers offering on-site customer training, CAE design facilities and design assistance are planned.

Fujitsu Mikroelektronik GmbH (European Sales Center)

Fujitsu Mikroelektronick GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a totally owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Western Europe. The wide range of IC products, LSI memories and, in particular, gate arrays are noted throughout Western Europe for design excellence and unmatched reliability. Five branch offices to support Fujitsu's semiconductor operations are located in Munich, London, Paris, Stockholm, and Milan.

Fujitsu Microelectronics Ireland, Ltd (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME supplies 64K/256K DRAMs, 64K CMOS/NMOS EPROMs, 256K EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with a highly-sophisticated CAD system to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Pacific Asia Ltd. (Asian/Oceanian Sales Centre)

Fujitsu Microelectronics Pacific Asia Ltd. (FMP) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

Fujitsu MCU/MPU Development History

August 1986

Part No.	Features	History												
		75	76	77	78	79	80	81	82	83	84	85	86	87
MB8840 SERIES	4-bit NMOS MCU			▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
MB8850 SERIES	4-bit CMOS MCU					▨	▨	▨	▨	▨	▨	▨	▨	▨
MB88400 SERIES	4-bit High End NMOS MCU							▨	▨	▨	▨	▨	▨	▨
MB88500 SERIES	4-bit High End CMOS MCU									▨	▨	▨	▨	▨
MB88700 SERIES	New 4-bit MOS MCU												▨	▨
MB89700 SERIES	New 8-bit CMOS MCU												▨	▨
MBL8049/39	8-bit NMOS MCU (Intel 8049/39 compatible)					▨	▨	▨	▨	▨	▨	▨	▨	▨
MBL8051/31	8-bit NMOS MCU (Intel 8051/31 compatible)											▨	▨	▨
MBL8086/8088	16-bit NMOS MPU (Intel 8086/88 compatible)								▨	▨	▨	▨	▨	▨
MBL80186/188	16-bit NMOS MPU (Intel 80186/188 compatible)											▨	▨	▨
MBL80286	16-bit NMOS High End (Intel 80286 compatible)											▨	▨	▨

▨ Production

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Section 1

Microprocessors and Peripherals

MBL80286 Microprocessor Family

MBL8086/8088/80186/80188 Microprocessor Family and Peripherals

FUJITSU

NMOS HIGH-PERFORMANCE 16-BIT MICROPROCESSOR WITH MEMORY MANAGEMENT AND PROTECTION

MBL 80286-8
MBL 80286-6

January 1986
Edition 1.0

NMOS HIGH PERFORMANCE 16-BIT MICROPROCESSOR WITH MEMORY MANAGEMENT AND PROTECTION

The Fujitsu MBL 80286 is an advanced, high-performance 16-bit microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The MBL 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. An 8 MHz MBL 80286 provides up to six times greater throughout than the standard 5 MHz MBL 8086. The MBL 80286 includes memory management capabilities that map up to 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The MBL 80286 is upward compatible with MBL 8086 and 88 software. Using MBL 8086 real address mode, the MBL 80286 is object code compatible with existing MBL 8086, 88 software. In protected virtual address mode, the MBL 80286 is source code compatible with MBL 8086, 88 software and may require upgrading to use virtual addresses supported by the MBL 80286's integrated memory management and protection mechanism. Both modes operate at full MBL 80286 performance and execute a superset of the MBL 8086 and 88's instructions.

The MBL 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The MBL 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

The MBL 80286 is housed in a 68-pad ceramic LCC (Leadless Chip Carrier: JEDEC Type A) or a 68-pin ceramic PGA (Pin Grid Array) package.

- **High Performance Processor (Up to six times MBL 8086)**
- **Large Address Space:**
  - **16 Megabytes Physical**
  - **1 Gigabyte Virtual per Task**
- **Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems**
- **Two MBL 8086 Upward Compatible Operating Modes:**
  - **MBL 8086 Real Address Mode**
  - **Protected Virtual Address Mode**
- **Two Ranges of Clock Rates:**
  - **8 MHz for MBL 80286-8**
  - **6 MHz for MBL 80286-6**
- **Optional Processor Extension:**
  - **MBL 80286 and Intel 80287 High Performance 80-bit Numeric Data Processor**
- **High Bandwidth Bus Interface (8 Megabyte/Sec)**
- **Two Package Options:**
  - **68-Pad Ceramic LCC (Suffix – CV) (JEDEC Type A)**
  - **68-Pin Ceramic PGA (Suffix – CR)**

Fig. 1 – BLOCK DIAGRAM

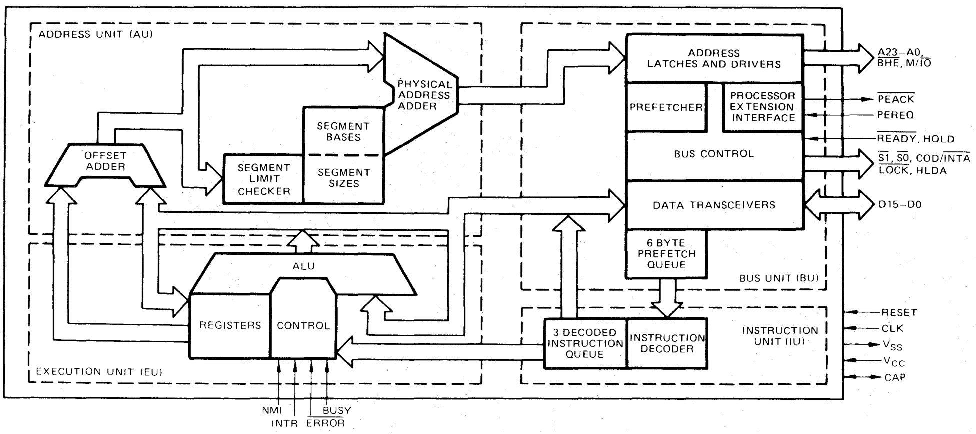
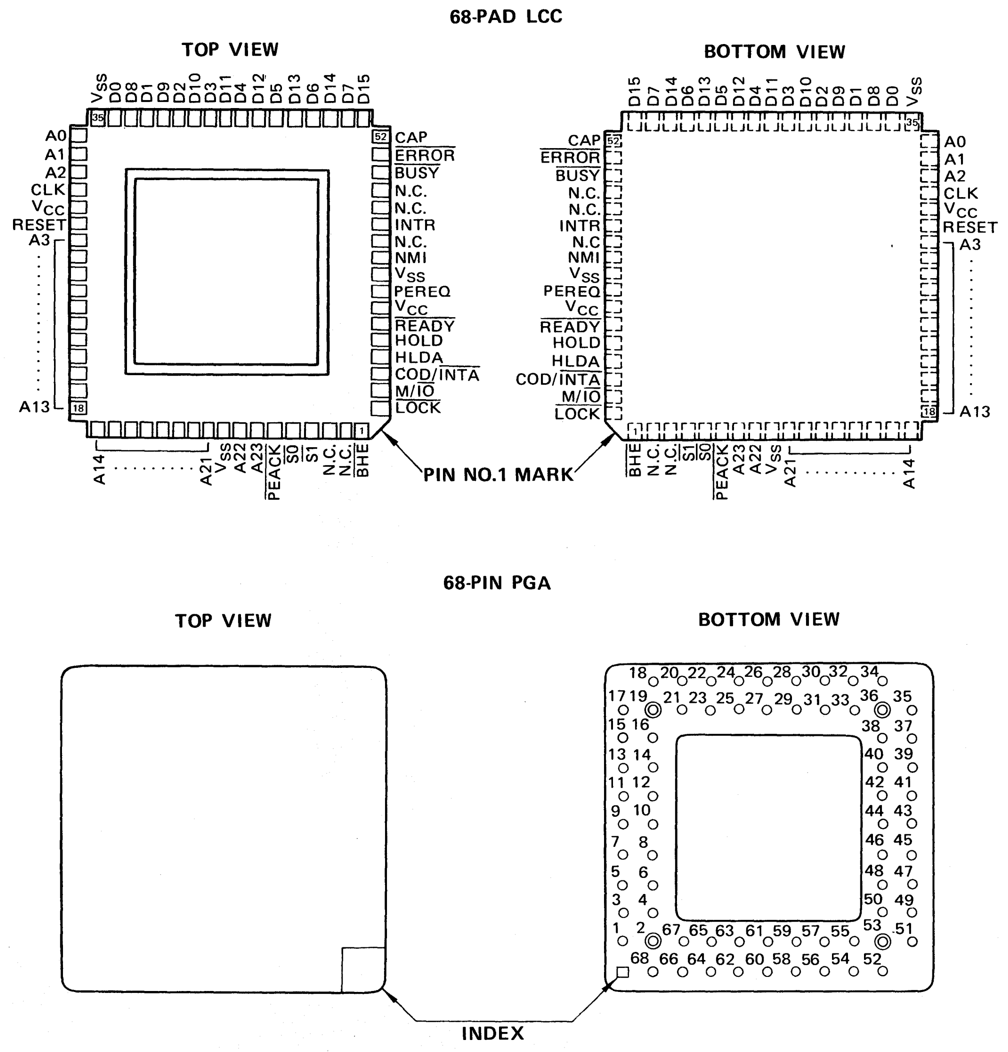


Fig. 2 – PIN CONFIGURATIONS



NOTE: N.C. pads and pins must not be connected.

PIN DESCRIPTION

The following pin function descriptions are for the MBL 80286 microprocessor:

Table 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
CLK	I	**System Clock** provides the fundamental timing for MBL 80286 systems. It is divided by two inside the MBL 80286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D15–D0	I/O	**Data Bus** inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
A23–A0	O	**Address Bus** outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred on pins D7–D0. A23–A16 are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
$\overline{BHE}$	O	**Bus High Enable** indicates transfer of data on the upper byte of the data bus, D15–D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.

$\overline{BHE}$ and A0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15–D8)
1	0	Byte transfer on lower half of data bus (D7–D0)
1	1	Reserved

Symbol	Type	Name and Function
$\overline{S1}$, $\overline{S0}$	O	**Bus Cycle Status** indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defineds the type of bus cycle. The bus is in a TS state whenever one or both are LOW. $\overline{S1}$ and $\overline{S0}$ are active LOW and float to 3-state OFF during bus hold acknowledge.

MBL 80286 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0 (LOW)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None: not a status cycle
0	1	0	0	If A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None: not a status cycle
1 (HIGH)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None: not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None: not a status cycle

Table 1 – PIN DESCRIPTION (Cont.)

Symbol	Type	Name and Function
M/$\overline{\text{IO}}$	O	**Memory/IO Select** distinguishes memory access from I/O access. If HIGH during TS, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{\text{IO}}$ floats to 3-state OFF during bus hold acknowledge.
COD/$\overline{\text{INTA}}$	O	**Code/Interrupt Acknowledge** distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{\text{INTA}}$ floats to 3-state OFF during bus hold acknowledge. Its timing is the same as M/$\overline{\text{IO}}$.
$\overline{\text{LOCK}}$	O	**Bus Lock** indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{\text{LOCK}}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by MBL 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{\text{LOCK}}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.
$\overline{\text{READY}}$	I	**Bus Ready** terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ LOW. $\overline{\text{READY}}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{\text{READY}}$ is ignored during bus hold acknowledge.
HOLD HLDA	I O	**Bus Hold Request and Hold Acknowledge** control ownership of the MBL 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the MBL 80286 will float its bus drivers to 3-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the MBL 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH.
INTR	I	**Interrupt Request** requests the MBL 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the MBL 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.
NMI	I	**Non-maskable Interrupt Request** interrupts the MBL 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the MBL 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
PEREQ $\overline{\text{PEACK}}$	I O	**Processor Extension Operand Request and Acknowledge** extend the memory management and protection capabilities of the MBL 80286 to processor extensions. The PEREQ input requests the MBL 80286 to perform a data operand transfer for a processor extension. The $\overline{\text{PEACK}}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to 3-state OFF during bus hold acknowledge. $\overline{\text{PEACK}}$ may be asynchronous to the system clock. $\overline{\text{PEACK}}$ is active LOW.

Table 1 – PIN DESCRIPTION (Cont.)

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{\text{BUSY}}$
$\overline{\text{ERROR}}$</td><td>I
I</td><td><b>Processor Extension Busy and Error</b> indicate the operating condition of a processor extension to the MBL 80286. An active $\overline{\text{BUSY}}$ input stops MBL 80286 program execution on WAIT and some ESC instructions until $\overline{\text{BUSY}}$ becomes inactive (HIGH). The MBL 80286 may be interrupted while waiting for $\overline{\text{BUSY}}$ to become inactive. An active $\overline{\text{ERROR}}$ input causes the MBL 80286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.</td></tr>
<tr><td>RESET</td><td>I</td><td><b>System Reset</b> clears the internal logic of the MBL 80286 and is active HIGH. The MBL 80286 may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the MBL 80286 enter the state shown below:
<table>
<tr><th colspan="2">MBL 80286 Pin State During Reset</th></tr>
<tr><th>Pin Value</th><th>Pin Names</th></tr>
<tr><td>1 (HIGH)</td><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{PEACK}}$, A23–A0, $\overline{\text{BHE}}$, $\overline{\text{LOCK}}$</td></tr>
<tr><td>0 (LOW)</td><td>M/$\overline{\text{IO}}$, COD/$\overline{\text{INTA}}$, HLDA</td></tr>
<tr><td>3-state OFF</td><td>D15–D0</td></tr>
</table>
Operation of the MBL 80286 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the MBL 80286 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed.
A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.</td></tr>
<tr><td>V_{SS}</td><td>I</td><td><b>System Ground:</b> 0 Volts.</td></tr>
<tr><td>V_{CC}</td><td>I</td><td><b>System Power:</b> +5 Volt Power Supply.</td></tr>
<tr><td>CAP</td><td>I</td><td><b>Substrate Filter Capacitor:</b> a 0.047μF ± 20% 12V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1μA is allowed through the capacitor.
For correct operation of the MBL 80286, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor chargeup time is 5 milliseconds (max.) after V_{CC} and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the MBL 80286 processor clock can be phase synchronized to another clock by pulsing RESET LOW synchronous to the system clock.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

Introduction

The MBL 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. Depending on the application, the MBL 80286's performance is up to six times faster than the standard 5 MHz MBL 8086's, while providing complete upward software compatibility with Fujitsu's MBL 8086, 88, and 186 family of CPU's.

The. MBL 80286 operates in two modes: MBL 8086 real address mode and protected virtual address mode. Both modes execute a superset of the MBL 8086 and 88 instruction set.

In MBL 8086 real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the MBL 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each tasks' programs and data. Both modes provide the same base instruction set, registers, and addressing modes.

The following Functional Description describes first, the base MBL 80286 architecture common to both modes, second, MBL 8086 real address mode, and third, protected mode.

MBL 8086 BASE ARCHITECTURE

The MBL 8086, 88, 186, and 286 CPU family all contain the same basic set of registers, instructions, and addressing modes. The MBL 80286 processor is upward compatible with the MBL 8086, 8088, and 80186 CPU's.

Register Set

The MBL 80286 base architecture has fifteen registers as shown in Fig. 3. These registers are grouped into the following four categories:

General Registers: Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

Segment Registers: Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

Base and Index Registers: Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

Status and Control Registers: The 3 16-bit special purpose registers in Fig. 3a record or control certain aspects of the MBL 80286 processor state including the Instruction Pointer, which contains the offset address of the next sequential instruction to be executed.

Fig. 3 – REGISTER SET

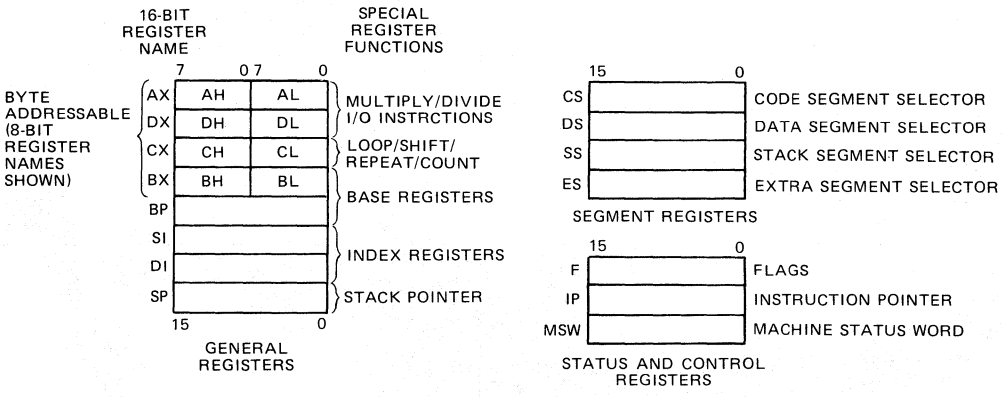
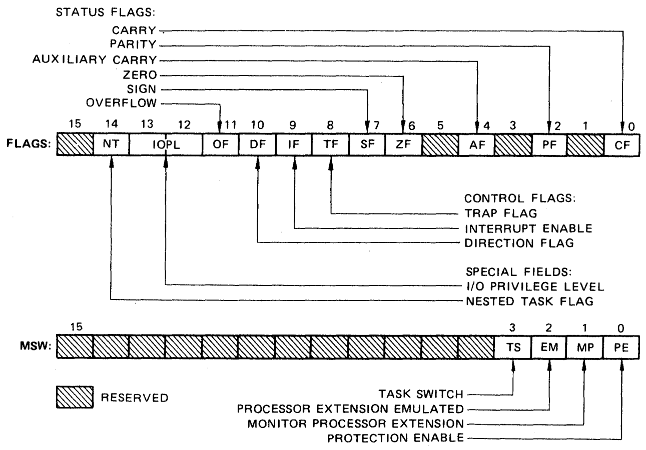


Fig. 3a — STATUS AND CONTROL REGISTER BIT FUNCTIONS



Flags Word Description

The Flags word (Flags) records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the MBL 80286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in Table 2.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high level instructions, and processor control. These categories are summarized in Fig. 4.

An MBL 80286 instruction can reference zero, one, or two operands; where an operand resides in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. NOP and HLT) are usually one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location. Two-operand instructions permit the following six types of instruction operations:

— Register to Register
— Memory to Register
— Immediate to Register
— Memory to Memory
— Register to Memory
— Immediate to Memory

Table 2 — FLAGS WORD BIT FUNCTIONS

Bit Position	Name	Function
0	CF	Carry Flag — Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag — Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag — Set if result is zero; cleared otherwise
7	SF	Sign Flag — Set equal to high-order bit or result (0 if positive, 1 if negative)
8	TF	Single Step Flag — Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag — When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag — Causes string instructions to auto decrement the appropriate index registers when set. Clearing DF causes auto increment.
11	OF	Overflow Flag — Set if result is a too-large positive number or a too-small negative number (excluding sign-bit) to fit in destination operand; cleared otherwise

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory to memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary at the end of this document.

For detailed operation and usage of each instruction, see Appendix of MBL 80286 Programmer's Reference Manual.

Fig. 4a – DATA TRANSFER INSTRUCTIONS

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

Fig. 4c – STRING INSTRUCTIONS

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

Fig. 4b – ARITHMETIC INSTRUCTIONS

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

Fig. 4d – SHIFT/ROTATE/LOGICAL INSTRUCTIONS

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"TEST" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

Fig. 4e — PROGRAM TRANSFER INSTRUCTIONS

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign
JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign

UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Fig. 4f — PROCESSOR CONTROL INSTRUCTIONS

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for TEST pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
EXECUTION ENVIRONMENT CONTROL	
LMSW	Load machine status word
SMSW	Store machine status word

Fig. 4g — HIGH LEVEL INSTRUCTIONS

ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Memory Organization

Memory is organized as sets of variable length segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit segment selector, and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment.

Fig. 5 — TWO COMPONENT ADDRESS

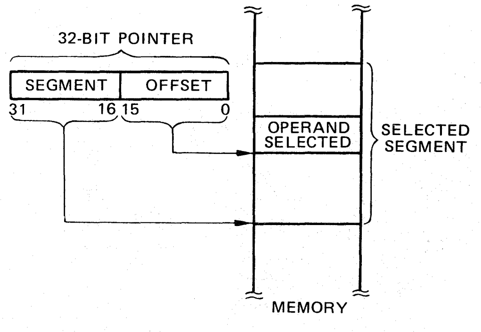


Table 3 – SEGMENT REGISTER SELECTION RULES

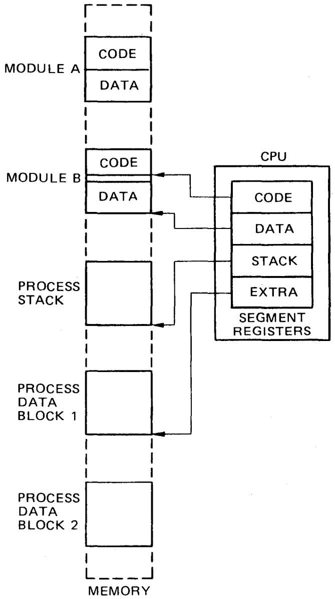
Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register.
Local Data	Data (DS)	All data references except when relative to stack or string destination
External (Global) Data	Extra (ES)	Alternate data segment and destination of string operation

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high speed segment registers. An instruction need specify only the desired segment register and an offset in order to address a memory operand.

Most instructions need not explicitly specify which segment register is used. The correct segment register is automatically chosen according to the rules of Table 3. These rules follow the way programs are written (see Fig. 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

Fig. 6 – SEGMENTED MEMORY HELPS STRUCTURE SOFTWARE



Addressing Modes

The MBL 80286 provides a total of eight addressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

Register Operand Mode: The operand is located in one of the 8 or 16-bit general registers.

Immediate Operand Mode: The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: segment selector and offset. The segment selector is supplied by a segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset is calculated by summing any combination of the following three address elements:

the **displacement** (an 8 or 16-bit immediate value contained in the instruction)

the **base** (contents of either the BX or BP base registers)

the **Index** (contents of either the SI or DI index registers)

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

Direct Mode: The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

Register Indirect Mode: The operand's offset is in one of the registers SI, DI, BX, or BP.

Based Mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a based register (BX or BP).

Indexed Mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

Based Indexed Mode: The operand's offset is the sum of the contents of a base register and an index register.

Based Indexed Mode with Displacement: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

Data Types

The MBL 80286 directly supports the following data types:

Integer: A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the MBL 80286 and Intel 80287 Numeric Data Processor.

Ordinal: An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.

Pointer: A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.

String: A contiguous sequence of bytes or words. A string may contain from 1 byte to 64K bytes.

ASCII: A byte representation of alphanumeric and control characters using the ASCII standard of character representation.

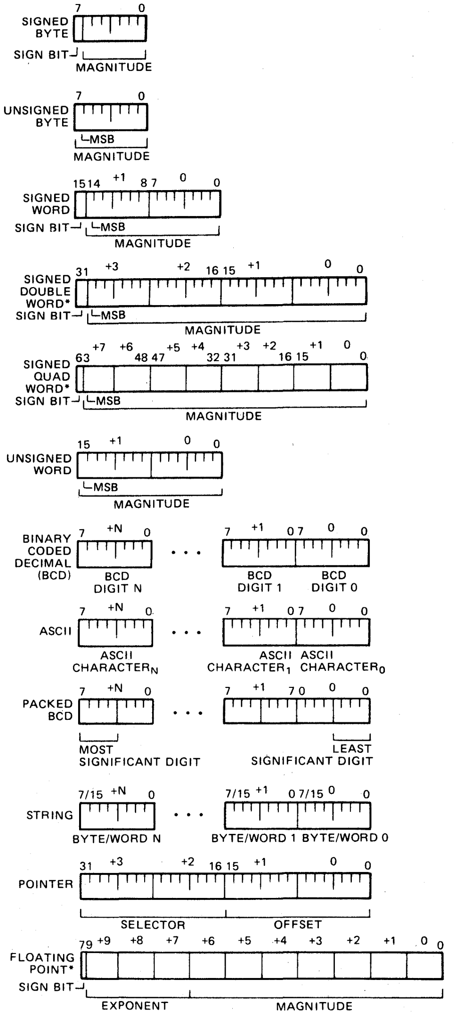
BCD: A byte (unpacked) representation of the decimal digits 0–9.

Packed BCD: A byte (packed) representation of two decimal digits 0–9 storing one digit in each nibble of the byte.

Floating Point: A signed 32, 64, or 80-bit real number representation. (Floating point operands are supported using the MBL 80286 and Intel 80287 Numeric Processor configuration.)

Fig. 7 graphically represents the data types supported by the MBL 80286.

Fig. 7 – MBL 80286 SUPPORTED DATA TYPES



*Supported by MBL 80286 and Intel 80287 Numeric Data Processor Configuration

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports.

I/O instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A15–A8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Table 4 – INTERRUPT VECTOR ASSIGNMENTS

Function	Interrupt Number	Related Instructions	Does Return Address Point to Instruction Causing Exception?
Divide error exception	0	DIV, IDIV	Yes
Single step interrupt	1	All	
NMI Interrupt	2	INT 2 or NMI pin	
Breakpoint interrupt	3	INT 3	
INTO detected overflow exception	4	INTO	No
BOUND range exceeded exception	5	BOUND	Yes
Invalid opcode exception	6	Any undefined opcode	Yes
Processor extension not available exception	7	ESC or WAIT	Yes
Reserved – do not use	8–15		
Processor extension error interrupt	16	ESC or WAIT	
Reserved – do not use	17–31		
User defined	32–255		

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS: IP) and machine state (Flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. The return address from an exception will always point at the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. For each interrupt, an 8-bit vector must be supplied to the MBL 80286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

MASKABLE INTERRUPT (INTR)

The MBL 80286 provides a maskable hardware interrupt request pin, INTR. Software enables this input by setting the interrupt flag bit (IF) in the flag word. All 224 user-defined interrupt sources can share this input, yet they can retain separate interrupt handlers. An 8-bit vector read by the CPU during the interrupt acknowledge sequence (discussed in System Interface section) identifies the source of the interrupt.

Further maskable interrupts are disabled while servicing an interrupt by resetting the IF but as part of the response to an interrupt or exception. The saved flag word will reflect the enable status of the processor prior to the interrupt. Until the flag word is restored to the flag register, the interrupt flag will be zero unless specifically set. The interrupt return instruction includes restoring the flag word, thereby restoring the original status of IF.

NON-MASKABLE INTERRUPT REQUEST (NMI)

A non-maskable interrupt input (NMI) is also provided. NMI has higher priority than INTR. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed.

While executing the NMI servicing procedure, the MBL 80286 will service neither further NMI requests, INTR requests, nor the processor extension segment overrun interrupt until an interrupt return (IRET) instruction is executed or the CPU is reset. If NMI occurs while currently servicing an NMI, its presence will be saved for servicing after executing the first IRET instruction. IF is cleared at the beginning of an NMI interrupt to inhibit INTR interrupts.

SINGLE STEP INTERRUPT

The MBL 80286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single stepped.

Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in Table 5. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If other interrupts remain enabled they are processed before the first instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

Table 5 – INTERRUPT PROCESSING ORDER

Order	Interrupt
1	Instruction exception
2	Single step
3	NMI
4	Processor extension segment overrun
5	INTR
6	INT instruction

Initialization and Processor Reset

Processor initialization or start up is accomplished by driving the RESET input pin HIGH. RESET forces the MBL 80286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET becomes inactive and an internal processing interval elapses, the MBL 80286 begins execution in real address mode with the instruction at physical location FFFFF0(H). RESET also sets some registers to predefined values as shown as shown in Table 6.

Table 6 – MBL 80286 INITIAL REGISTER STATE AFTER RESET

Flag word	0002(H)
Machine Status Word	FFF0(H)
Instruction pointer	FFF0(H)
Code segment	F000(H)
Data segment	0000(H)
Extra segment	0000(H)
Stack segment	0000(H)

Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the MBL 80286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in Table 7, control the processor extension interface. After RESET, this register contains FFF0(H) which places the MBL 80286 in MBL 8086 real address mode.

Table 7 – MSW BIT FUNCTIONS

Bit Position	Name	Function
0	PE	Protected mode enable places the MBL 80286 into protected mode and can not be cleared except by RESET.
1	MP	Monitor processor extension allows WAIT instructions to cause a processor extension not present exception (number 7).
2	EM	Emulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension.
3	TS	Task switched indicates the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task.

Table 8 – RECOMMENDED MSW ENCODINGS FOR PROCESSOR EXTENSION CONTROL

TS	MP	EM	Recommended Use	Instructions Causing Exception 7
0	0	0	Initial encoding after RESET. MBL 80286 operation is identical to MBL 8086, 88.	None
0	0	1	No processor extension is available. Software will emulate its function.	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task.	ESC
0	1	0	A processor extension exists.	None
1	1	0	A propessor extension exists. The current processor extension context may belong to another task. The Exception 7 on WAIT allows software to test for an error pending from a previous processor extension operation.	ESC or WAIT

The LMSW and SMSW instructions can load and store the MSW in real address mode. The recommended use of TS, EM, and MP is shown in Table 8.

Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET will force the MBL 80286 out of halt. If interrupted, the saved CS:IP will point to the next instruction after the HLT.

MBL 8086 REAL ADDRESS MODE

The MBL 80286 executes a fully upward-compatible superset of the MBL 8086 instruction set in real address mode. In real address mode the MBL 80286 is object code compatible with MBL 8086 and 8088 software. The real address mode architecture (registers and addressing modes) is exactly as described in the MBL 80286 Base Architecture section of this Functional Description.

Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A0 through A19 and $\overline{\text{BHE}}$. A20 through A23 may be ignored.

Memory Addressing

In real address mode physical memory is a contiguous array of up to 1,048,576 bytres (one megabyte) addressed by pins A0 through A19 and $\overline{\text{BHE}}$. A20 through A23 may be ignored.

The selector portion of a pointer is interpreted as the upper 16 bits of a 20-bit segment address. The lower four bits of the 20-bit segment address are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See Fig. 8 for a graphic representation of address formation.

All segments in real address mode are 64K bytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low order byte at offset FFFF(H) and its high order byte at offset 0000(H)). If, in real address mode, the information contained in a segment does not use the full 64K bytes, the unused end of the segment may be overlayed by another segment to reduce physical memory requirements.

Reserved Memory Locations

The MBL 80286 reserves two fixed areas of memory in real address mode (see Fig. 9); system initialization area and interrupt table area. Locations from addresses FFFF0(H) through FFFFF(H) are reserved for system initialization. Initial execution begins at location FFFF0(H). Locations 00000(H) through 003FF(H) are reserved for interrupt vectors.

Fig. 8 – MBL 8086 REAL ADDRESS MODE ADDRESS CALCULATION

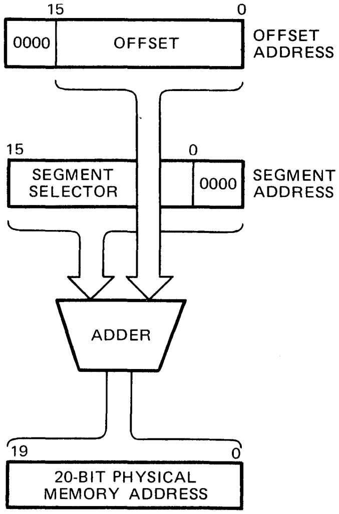
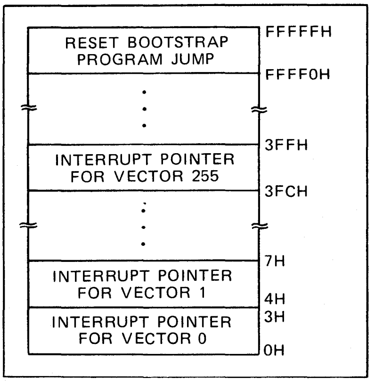


Fig. 9 – MBL 8086 REAL ADDRESS MODE INITIALLY RESERVED MEMORY LOCATIONS


RESET BOOTSTRAP PROGRAM JUMP
FFFFFH
FFFF0H
INTERRUPT POINTER FOR VECTOR 255
3FFH
3FCH
INTERRUPT POINTER FOR VECTOR 1
7H
4H
INTERRUPT POINTER FOR VECTOR 0
3H
0H

INITIAL CS:IP VALUE IS F000:FFF0.

Table 9 – REAL ADDRESS MODE ADDRESSING INTERRUPTS

Function	Interrupt Number	Related Instructions	Return Address Before Instruction?
Interrupt table limit too small exception	8	INT vector is not within table limit.	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H).	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment.	Yes

Interrupts

Table 9 shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA). Refer to the next section on protected mode initialization for a discussion on exception 8.

Protected Mode Initialization

To prepare the MBL 80286 for protected mode, the LIDT instruction is used to load the 24-bit interrupt table base and 16-bit limit for the protected mode interrupt table. This instruction can also set a base and limit for the inter rupt vector table in real address mode. After reset, the interrupt table base is initialized to 000000(H) and its size set to 03FF(H). These values are compatible with MBL 8086, 88 software. LIDT should only be executed in preparation for protected mode.

Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A1 HIGH for halt and A1 LOW for shutdown. In real address mode, shutdown can occur under two conditions.

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL INT or PUSH instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

PROTECTED VIRTUAL ADDRESS MODE

The MBL 80286 executes a fully upward-compatible superset of the MBL 8086 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The MBL 80286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating systems and virtual memory.

All registers, instructions, and addressing modes described in the MBL 80286 Base Architecture section of this Functional Description remain the same. Programs for the MBL 8086, 88, 186, and real address mode MBL 80286 can be run in protected mode; however, embedded constants for segment selectors are different.

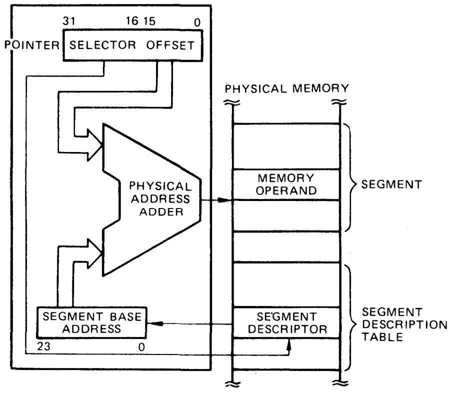
Memory Size

The protected mode MBL 80286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pins A23–A0 and $\overline{\text{BHE}}$. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit base address of the desired segment is obtained from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in Fig. 10. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All MBL 80286 instructions which load a segment register will reference the memory based tables without additional software. The memory based tables contain 8 byte values called descriptors.

Fig. 10 – PROTECTED MODE MEMORY ADDRESSING



DESCRIPTORS

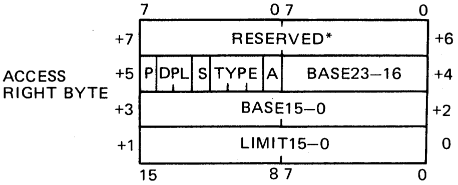
Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The MBL 80286 has segment descriptors for code, stack and data segments, and system control descriptors for special system data segments and control transfer ôperations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multi-processor systems.

CODE AND DATA SEGMENT DESCRIPTORS (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64K bytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems) (See Fig. 11). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.

Fig. 11 – CODE AND DATA SEGMENT DESCRIPTOR FORMATS

Code or Data Segment Descriptor



*Must be set to 0 for compatability with iAPX386.

Access Rights Byte Definition

	Bit Position	Name	Function		
	7	Present (P)	P = 1 P = 0	Segment is mapped into physical memory. No mapping to physical memory exists, base and limit are not used.	
	6-5	Descriptor Privilege Level (DPL)		Segment privilege attribute used in privilege tests.	
	4	Segment Descriptor (S)	S = 1 S = 0	Code or Data (includes stacks) segment descriptor System Segment Descriptor or Gate Descriptor	
Type Field Definition	3	Executable (E)	E = 0	Data segment descriptor type is:	If Data Segment (S = 1, E = 0)
	2	Expansion Direction (ED)	ED = 0 ED = 1	Expand up segment, offsets must be ≤ limit. Expand down segment, offsets must be > limit.	
	1	Writeable (W)	W = 0 W = 1	Data segment may not be written into. Data segment may be written into.	
	3	Executable (E)	E = 1	Code Segment Descriptor type is:	If Code Segment (S = 1, E = 1)
	2	Conforming (C)	C = 1	Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged.	
	1	Readable (R)	R = 0 R = 1	Code segment may not be read. Code segment may be read.	
	0	Accessed (A)	A = 0 A = 1	Segment has not been accessed. Segment selector has been loaded into segment register or used by selector test instructions.	

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors (S = 1). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte. The access rights byte of both code and data segment descriptor types have three fields in common: present (P) bit, Descriptor Privilege Level (DPL), and accessed (A) bit. If P = 0, any attempted use of this segment will cause a not-present exception. DPL specifies the privilege level of the segment descriptor. DPL controls when the descriptor may be used by a task (refer to privilege discussion below). The A bit shows whether the segment has been previously accessed for usage profiling, a necessity for virtual memory systems. The CPU will always set this bit when accessing the descriptor.

Data segments (S = 1, E = 0) may be either read-only or read-write as controlled by the W bit of the access rights byte. Read-only (W = 0) data segments may not be written into. Data segments may grow in two directions, as determined by the Expansion Direction (ED) bit: upwards (ED = 0) for data segments, and downwards (ED = 1) for a segment containing a stack. The limit field for a data segment descriptor is interpreted differently depending on the ED bit (see Fig. 11).

A code segment (S = 1, E = 1) may be execute-only or execute/read as determined by the Readable (R) bit. Code segments may never be written into and execute-only code segments (R = 0) may not be read. A code segment may also have an attribute called conforming (C). A conforming code segment may be shared by programs that execute at different privilege levels. The DPL of a conforming code segment defines the range of privilege levels at which the segment may be executed (refer to privilege discussion below). The limit field identifies the last byte of a code segment.

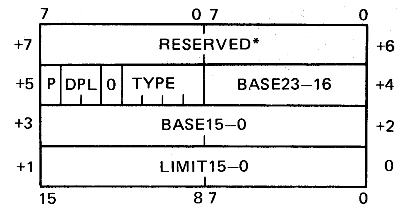
SYSTEM SEGMENT DESCRIPTORS (S = 0, TYPE = 1-3)

In addition to code and data segment descriptors, the protected mode MBL 80286 defines System Segment Descriptors. These descriptors define special system data segments which contain a table of descriptors (Local Descriptor Table Descriptor) or segments which contain the execution state of a task (Task State Segment Descriptor).

Fig. 12 gives the formats for the special system data segment descriptors. The descriptors contain a 24-bit base address of the segment and a 16-bit limit. The access byte defines the type of descriptor, its state and privilege level. The descriptor contents are valid and the segment is in physical memory if P = 1. If P = 0, the segment is not valid. The DPL field is only used in Task State Segment descriptors and indicates the privilege level at which the descriptor may be used (see Privilege). Since the Local Descriptor Table descriptor may only be used by a special privileged instruction, the DPL field is not used. Bit 4 of the access byte is 0 to indicate that it is a system control descriptor. The type field specifies the descriptor type as indicated in Fig. 12.

Fig. 12 — SYSTEM SEGMENT DESCRIPTOR FORMAT

System Segment Descriptor



*Must be set to 0 for compatability with iAPX386.

System Segment Descriptor Fields

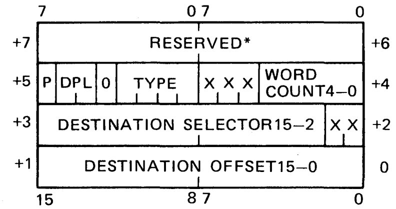
Name	Value	Description
TYPE	1 2 3	Available Task State Segment (TSS) Local Descriptor Table Busy Task State Segment (TSS)
P	0 1	Descriptor contents are not valid. Descriptor contents are valid.
DPL	0–3	Descriptor Privilege Level
BASE	24-bit number	Base Address of special system data segment in real memory
LIMIT	16-bit number	Offset of last byte in segment

GATE DESCRIPTORS (S = 0, TYPE = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are call gates, task gates, interrupt gates and trap gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see Privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

Fig. 13 shows the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. These gate descriptors contain the entry point to prevent a program from constructing and using an illegal entry point. Task gates may only refer to a task state segment. Since task gates invoke a task switch, the destination offset is not used in the task gate.

Fig. 13 – GATE DESCRIPTOR FORMAT
Gate Descriptor



*Must be set to 0 for compatibility with iAPX 386.
(X is don't care)

Gate Descriptor Fields

Name	Value	Description
TYPE	4 5 6 7	– Call Gate – Task Gate – Interrupt Gate – Trap Gate
P	0 1	– Descriptor Contents are not valid. – Descriptor Contents are valid.
DPL	0–3	Descriptor Privilege Level
WORD COUNT	0–31	Number of words to copy from callers stack to called procedures stack. Only used with call gate.
DESTINATION SELECTOR	16-bit selector	Selector to the target code segment (Call, Interrupt or Trap Gate) Selector to the target task state segment (Task Gate)
DESTINATION OFFSET	16-bit offset	Entry point within the target code segment

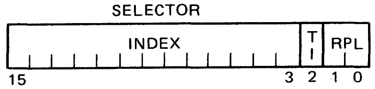
Exception 13 is generated when the gate is ued if a destination selector does not refer to the correct descriptor type. The word count field is used in the call gate descriptor to indicate the number of parameters (0-31 words) to`be automatically copied from the caller's stack to the stack of the called routine when a control transfer changes privilege levels. The word count field is not used by any other gate descriptor.

The access byte format is the same for all gate descriptors. P = 1 indicates that the gate contents are valid. P = 0 indicates the contents are not valid and causes exception 11 if referenced. DPL is the descriptor privilege level and specifies when this descriptor may be used by a task (refer to privilege discussion below). Bit 4 must equal 0 to indicate a system control descriptor. The type field specifies the descriptor type as indicated in Fig. 13.

SEGMENT DESCRIPTOR CACHE REGISTERS

A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment

Fig. 15 – SELECTOR FIELDS

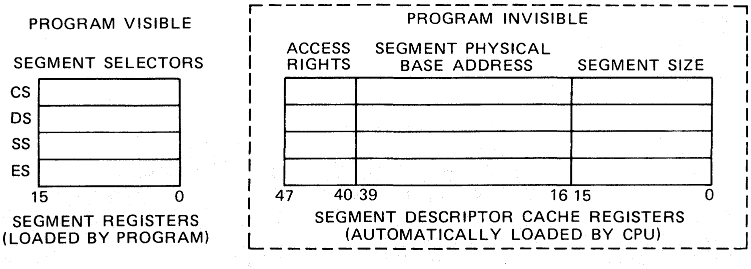


BITS	NAME	FUNCTION
1–0	REQUESTED PRIVILEGE LEVEL (RPL)	INDICATES SELECTOR PRIVILEGE LEVEL DESIRED

2	TABLE INDICATOR (TI)	TI = 0 USE GLOBAL DESCRIPTOR TABLE (GDT)
		TI = 1 USE LOCAL DESCRIPTOR TABLE (LDT)

15–3	INDEX	SELECT DESCRIPTOR ENTRY IN TABLE

Fig. 14 – DESCRIPTOR CACHE REGISTERS



descriptors are automatically loaded (cached) into a segment descriptor cache register (Fig. 14) whenever the associated segment register is loaded with a selector. Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing the descriptor. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.

SELECTOR FIELDS

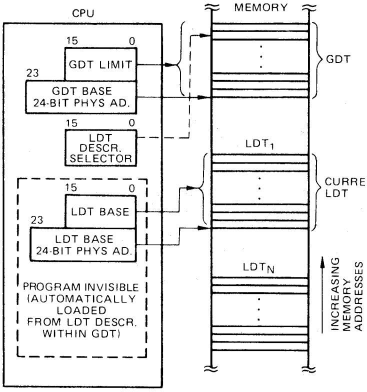
A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (TI), and selector privilege (RPL) as shown in Fig. 15. These fields select one of two memory based tables of descriptors, select the appropriate table entry and allow high-speed testing of the selector's privilege attribute.

LOCAL AND GLOBAL DESCRIPTOR TABLES

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in Fig. 16. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

One table, called the Global Descriptor Table (GDT), contains descriptors available to all tasks. The other table, called the Local Descriptor Table (LDT), contains descriptors that can be private to a task. Each task may have its own private LDT. The GDT may contain all descriptor types except interrupt and trap descriptors. The LDT may contain only segment, task gate, and call gate descriptors. A segment cannot be accessed by a task if its segment descriptor does not exist in either descriptor table at the time of access.

Fig. 16 – LOCAL AND GLOBAL DESCRIPTOR TABLE DEFINITION



The LGDT and LLDT instructions load the base and limit of the global and local descriptor tables. LGDT and LLDT are privileged, i.e. they may only be executed by trusted programs operating at level 0. The LGDT instruction loads a six byte field containing the 16-bit table-limit and 24-bit physical base address of the Global Descriptor Table as shown in Fig. 17. The LDT instruction loads a selector which refers to a Local Descriptor Table descriptor containing the base address and limit for an LDT, as shown in Fig. 12.

Fig. 17 – GLOBAL DESCRIPTOR TABLE AND INTERRUPT DESCRIPTOR TABLE DATA TYPE

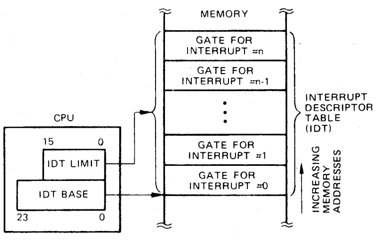
	7 0	7 0	
+5	RESERVED*	BASE23–16	+4
+3	BASE15–0		+2
+1	LIMIT15–0		0
	15 8	7 0	

*Must be set to 0 for compatibility with iAPX 386.

INTERRUPT DESCRIPTOR TABLE

The protected mode MBL 80286 has a third descriptor table, called the Interrupt Descriptor Table (IDT) (see Fig. 18), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT (Interrupt Descriptor Table) has a 24-bit physical base and 16-bit limit register in the CPU. The privileged LIDT instruction loads these registers with a six byte value of identical form to that of the LGDT instruction (see Fig. 17 and Protected Mode Initialization).

Fig. 18 – INTERRUPT DESCRIPTOR TABLE DEFINITION

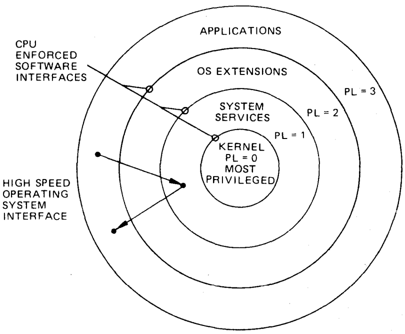


References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.

Privilege

The MBL 80286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors (and their associated segments) within a task. Four-level privilege, as shown in Fig. 19, is an extension of the user/supervisor mode commonly found in minicomputers. The privilege levels are numbered 0 through 3. Level 0 is the most privileged level. Privilege levels provide protection within a task. (Tasks are isolated by providing private LDT's for each task.) Operating system routines, interrupt handlers, and other system software can be included and protected within the virtual address space of each task using the four levels of privilege. Each task in the system has a separate stack for each of its privilege levels.

Fig. 19 – HIERARCHICAL PRIVILEGE LEVELS


APPLICATIONS
CPU ENFORCED SOFTWARE INTERFACES
OS EXTENSIONS
PL = 3
SYSTEM SERVICES
PL = 2
PL = 1
KERNEL PL = 0 MOST PRIVILEGED
HIGH SPEED OPERATING SYSTEM INTERFACE

NOTE: PL BECOMES NUMERICALLY LOWER AS PRIVILEGE LEVEL INCREASES

Tasks, descriptors, and selectors have a privilege level attribute that determines whether the descriptor may be used. Task privilege effects the use of instructions and descriptions. Descriptor and selector privilege only effect access to the descriptor.

TASK PRIVILEGE

A task always executes at one of the four privilege levels. The task privilege level at any specific instant is called the Current Privilege Level (CPL) and is defined by the lower two bits of the CS register. CPL cannot change during execution in a single code segment. A task's CPL may only be changed by control transfers through gate descriptors to a new code segment (See Control Transfer). Tasks begin executing at the CPL value specified by the code segment selector within TSS when the task is initiated via a task switch operation (See Fig. 20). A task executing at Level 0 can access all data segments defined in the GDT and the task's LDT and is considered the most trusted level. A task executing a Level 3 has the most restricted access to data and is considered the least trusted level.

DESCRIPTOR PRIVILEGE

Descriptor privilege is specified by the Descriptor Privilege Level (DPL) field of the descriptor access byte. DPL specifies the least trusted task privilege level (CPL) at which a task may access the descriptor. Descriptors with DPL = 0 are the most protected. Only tasks executing at privilege level 0 (CPL = 0) may access them. Descriptors with DPL = 3 are the least protected (i.e. have the least restricted access) since tasks can access them when CPL = 0, 1, 2, or 3. This rule applies to all descriptors, except LDT descriptors.

SELECTOR PRIVILEGE

Selector privilege is specified by the Requested Privilege Level (RPL) field in the least significant two bits of a selector. Selector RPL may establish a less trusted privilege level than the current privilege level for the use of a selector. This level is called the task's effective privilege level (EPL). RPL can only reduce the scope of a task's access to data with this selector. A task's effective privilege is the numeric maximum of RPL and CPL. A selector with RPL = 0 imposes no additional restriction on its use while a selector with RPL = 3 can only refer to segments at privilege Level 3 regardless of the task's CPL. RPL is generally used to verify that pointer parameters passed to a more trusted procedure are not allowed to use data at a more privileged level than the caller (refer to pointer testing instructions).

Descriptor Access and Privilege Validation

Determining the ability of a task to access a segment involves the type of segment to be accessed, the instruction used, the type of descriptor used and CPL, RPL, and DPL. The two basic types of segment accesses are control transfer (selectors loaded into CS) and data (selectors loaded into DS, ES or SS).

DATA SEGMENT ACCESS

Instructions that load selectors into DS and ES must refer to a data segment descriptor or readable code segment descriptor. The CPL of the task and the RPL of the selector must be the same as or more privileged (numerically equal to or lower than) than the descriptor DPL. In general, a task can only access data segments at the same or less privileged levels than the CPL or RPL (whichever is numerically higher) to prevent a program from accessing data it cannot be trusted to use.

An exception to the rule is a readable conforming code segment. This type of code segment can be read from any privilege level.

If the privilege checks fall (e.g. DPL is numerically less than the maximum of CPL and RPL) or an incorrect type of descriptor is referenced (e.g. gate descriptor or execute only code segment) exception 13 occurs. If the segment is not present, exception 11 is generated.

Instructions that load selectors into SS must refer to data segment descriptors for writable data segments. The descriptor privilege (DPL) and RPL must equal CPL. All other descriptor types or a privilege level violation will cause exception 13. A not present fault causes exception 12.

CONTROL TRANSFER

Four types of control transfer can occur when a selector is loaded into CS by a control transfer operation (see Table 10). Each transfer type can only occur if the operation which loaded the selector references the correct descriptor type. Any violation of these descriptor usage rules (e.g. JMP through a call gate or RET to a Task State Segment) will cause exception 13.

The ability to reference a descriptor for control transfer is also subject to rules of privilege. A CALL or JUMP instruction may only reference a code segment descriptor with DPL equal to the task CPL or a conforming segment with DPL of equal or greater privilege than CPL. The RPL of the selector used to reference the code descriptor must have as much privilege as CPL.

RET and IRET instructions may only reference code segment descriptors with descriptor privilege equal to or less privileged than the task CPL. The selector loaded into CS is the return address from the stack. After the return, the selector RPL is the task's new CPL. If CPL changes, the old stack pointer is popped after the return address.

When a JMP or CALL references a Task State Segment descriptor, the descriptor DPL must be the same or less privileged than the task's CPL. Reference to a valid Task State Segment descriptor causes a task switch (see Task Switch Operation). Reference to a Task State Segment descriptor at a more privileged level than the task's CPL generates exception 13.

When an instruction or interrupt references a gate descriptor, the gate DPL must have the same or less privilege than the task CPL. If DPL is at a more privileged level than CPL, exception 13 occurs. If the destination selector contained in the gate references a code segment descriptor, the code segment descriptor DPL must be the same or more privileged than the task CPL. If not, Exception 13 is issued. After the control transfer, the code segment descriptors DPL is the task's new CPL. If the destination selector in the gate references a task state segment, a task switch is automatically performed (see Task Switch Operation).

Table 10 – DESCRIPTOR TYPES USED FOR CONTROL TRANSFER

Control Transfer Types	Operation Types	Descriptor Referenced	Descriptor Table
Intersegment within the same privilege level	JMP, CALL, RET, IRET*	Code Segment	GDT/LDT
Intersegment to the same or higer privilege level Interrupt within task may change CPL	CALL	Call Gate	GDT/LDT
	Interrupt Instruction, Exception, External Interrupt	Trap or Interrupt Gate	IDT
Intersegment to a lower privilege level (changes task CPL)	RET, IRET*	Code Segment	GDT/LDT
	CALL, JMP	Task State Segment	GDT
Task Switch	CALL, JMP	Task Gate	GDT/LDT
	IRET** Interrupt Instruction, Exception, External Interrupt	Task Gate	IDT

* NT (Nested Task bit of flag word) = 0
** NT (Nested Task bit of flag word) = 1

The privilege rules on control transfer require:

- JMP or CALL direct to a code segment (code segment descriptor) can only be to a conforming segment with DPL of equal or greater privilege than CPL or a non-conforming segment at the same privilege level.
- interrupts within the task or calls that may change privilege levels, can only transfer control through a gate at the same or a less privileged level than CPL to a code segment at the same or more privileged level than CPL.
- return instructions that don't switch tasks can only return control to a code segment at the same or less privileged level.
- task switch can be performed by a call, jump or interrupt which references either a task gate or task state segment at the same or less privileged level.

PRIVILEGE LEVEL CHANGES

Any control transfer that changes CPL within the task, causes a change of stacks as part of the operation. Initial values of SS:SP for privilege levels 0, 1, and 2 are kept in the task state segment (refer to Task Switch Operation). During a JMP or CALL control transfer, the new stack pointer is loaded into the SS and SP registers and the previous stack pointer is pushed onto the new stack.

When returning to the original privilege level, its stack is restored as part of the RET or IRET instruction operation. For subroutine calls that pass parameters on the stack and cross privilege levels, a fixed number of words, as specified in the gate, are copied from the previous stack to the current stack. The inter-segment RET instruction with a stack adjustment value will correctly restore the previous stack pointer upon return.

Protection

The MBL 80286 includes mechanisms to protect critical instructions that affect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These protection mechanisms are grouped into three forms:

Restricted usage of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the Local Descriptor Table (LDT) and Global Descriptor Table (GDT).

Restricted access to segments via the rules of privilege and descriptor usage.

Privileged instructions or operations that may only be executed at certain privilege levels as determined by the CPL and I/O Privilege Level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

Table 11 – SEGMENT REGISTER LOAD CHECKS

Error Description	Exception Number
Descriptor table limit exceeded	13
Segment descriptor not-present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: – Read only data segment load to SS – Special control descriptor load to DS, ES, SS – Execute only segment load to DS, ES, SS – Data segment load to CS – Read/Execute code segment load to SS	13

Table 12 – OPERAND REFERENCE CHECKS

Error Description	Exception Number
Write into code segment	13
Read from execute-only code segment	13
Write to read-only data segment	13
Segment limit exceeded	12 or 13

Note 1: Carry out in offset calculations is ignored.

Table 13 – PRIVILEGED INSTRUCTION CHECKS

Error Description	Exception Number
CPL ≠ 0 when executing the following instructions: LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPL > IOPL when executing the following instructions: INS, IN, OUTS, OUT, STI, CLI, LOCK	13

These checks are performed for all instructions and can be split into three categories: segment load checks (Table 11), operand reference checks (Table 12), and privileged instruction checks (Table 13). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). Precisely these are:

- The IF bit is not changed if CPL > IOPL
- The IOPL field of the flag word is not changed if CPL > 0.

No exceptions or other indication are given when these conditions occur.

EXCEPTIONS

The MBL 80286 detects several types of exceptions and interrupts, in protected mode (see Table 14). Most are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions can read an error code, pushed on the stack after the return address, that

Table 14 – PROTECTED MODE EXCEPTIONS

Interrupt Vector	Function	Return Address At Failing Instruction?	Always Restartable?	Error Code on Stack?
8	Double exception detected	Yes	No[2]	Yes
9	Processor extension segment overrun	No	No[2]	No
10	Invalid task state segment	Yes	Yes	Yes
11	Segment not present	Yes	Yes	Yes
12	Stack segment overrun or stack segment not present	Yes	Yes[1]	Yes
13	General protection	Yes	No[2]	Yes

NOTE 1: When a PUSHA or POPA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable because stack segment wrap around is not permitted. This condition is identified by the value of the saved SP being eigher 0000(H), 0001(H), FFFE(H), or FFFF(H).

NOTE 2: These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

identifies the selector involved (0 if none). The return address normally points to the failing instruction, including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

All these checks are performed for all instructions and can be split into three categories: segment load checks (Table 11), operand reference checks (Table 12), and privileged instruction checks (Table 13). Any violation of the rules shown will result in an exception. A not-present exception causes exception 11 or 12 and is restartable.

Special Operations

TASK SWITCH OPERATION

The MBL 80286 provides a built-in task switch operation which saves the entire MBL 80286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a Task State Segment (TSS) or task gate descriptor in the GDT or LDT. An INT instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see Fig. 20) containing the entire MBL 80286 execution state while a task gate descriptor contains a TSS selector. The limit field of the descriptor must be > 002B(H).

Each task must have a TSS associated with it. The current TSS is identified by a special register in the MBL 80286 called the Task Register (TR). This register contains a selector referring to the task state segment descriptor that defines the current TSS. A hidden base and limit register associated with TR are loaded whenever TR is loaded with a new selector.

The IRET instruction is used to return control to the task that called the current task or was interrupted. Bit 14 in the flag register is called the Nested Task (NT) bit. It controls the function of the IRET instruction. If NT = 0, the IRET instruction performs the regular current task return by popping values off the stack; when NT = 1, IRET performs a task switch operation back to the previous task.

When a CALL, JMP, or INT instruction initiates a task switch, the old and new TSS will be marked busy and the back link field of the new TSS set to the old TSS selector. The NT bit of the new task is set by CALL or INT initiated task switches. An interrupt that does not cause a task switch will clear NT. NT may also be set or cleared by POPF or IRET instructions.

The task state segment is marked busy by changing the descriptor type field from Type 1 to Type 3. Use of a selector that references a busy task state segment causes Exception 13.

PROCESSOR EXTENSION CONTEXT SWITCHING

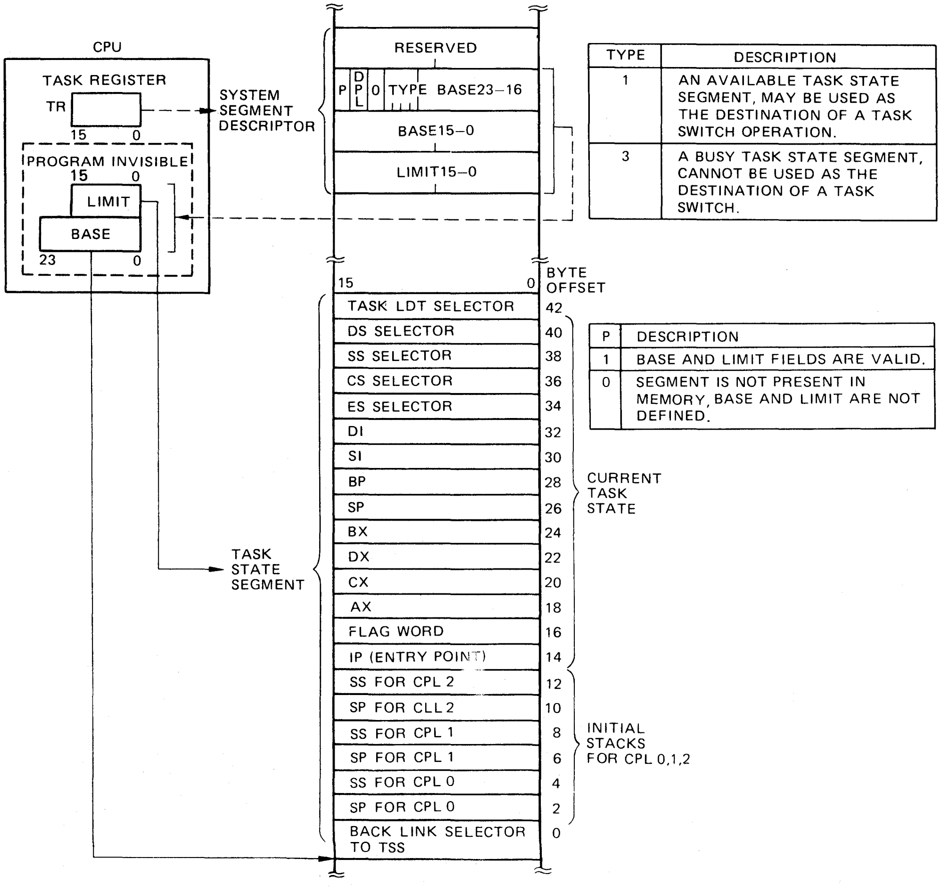
The context of a processor extension (such as the 80287 numerics processor) is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task). The MBL 80286 detects the first use of a processor extension after a task switch by causing the processor extension not present exception (7). The interrupt handler may then decide whether a context change is necessary.

Whenever the MBL 80286 switches tasks, if sets the Task Switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS = 1 and a processor extension is present (MP = 1 in MSW).

POINTER TESTING INSTRUCTIONS

The MBL 80286 provides several instructions to speed pointer testing and consistency checks for maintaining system integrity (see Table 15). These instructions use the memory management hardware to verify that a selector value refers to an appropriate segment without risking an exception. A condition flag (ZF) indicates whether use of the selector or segment will cause an exception.

Fig. 20 – TASK STATE SEGMENT AND TSS REGISTERS



TYPE	DESCRIPTION
1	AN AVAILABLE TASK STATE SEGMENT, MAY BE USED AS THE DESTINATION OF A TASK SWITCH OPERATION.
3	A BUSY TASK STATE SEGMENT, CANNOT BE USED AS THE DESTINATION OF A TASK SWITCH.

P	DESCRIPTION
1	BASE AND LIMIT FIELDS ARE VALID.
0	SEGMENT IS NOT PRESENT IN MEMORY, BASE AND LIMIT ARE NOT DEFINED.

Table 15 – MBL 80286 POINTER TEST INSTRUCTIONS

Instruction	Operands	Function
ARPL	Selector, Register	Adjust Requested Privilege Level: adjusts the RPL of the selector to the numeric maximum of current selector RPL value and the RPL value in the register. Set zero flag if selector RPL was changed by ARPL.
VERR	Selector	VERify for Read: sets the zero flag if the segment referred to by the selector can be read.
VERW	Selector	VERify for Write: sets the zero flag if the segment referred to by the selector can be written.
LSL	Register, Selector	Load Segment Limit: reads the segment limit into the register if privilege rules and descriptor type allow. Set zero flag if successful.
LAR	Register, Selector	Load Access Rights: reads the descriptor access rights byte into the register if privilege rules allow. Set zero flag if successful.

DOUBLE FAULT AND SHUTDOWN

If two separate exceptions are detected during a single instruction execution, the MBL 80286 performs the double fault exception (8). If an exception occurs during processing of the double fault exception, the MBL 80286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the MBL 80286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A1 HIGH.

PROTECTED MODE INITIALIZATION

The MBL 80286 initially executes in real address mode after RESET. To allow initialization code to be placed at the top of physical memory, A23–A20 will be HIGH When the MBL 80286 performs memory references relative to the CS register until CS is changed. A23–A20 will be zero for references to the DS, ES, or SS segments. Changing CS in real address mode will force A23–A20 LOW whenever CS is used again. The initial CS:IP value of F000:FFF0 provides 64K bytes of code space for initialization code without changing CS.

Protected mode operation requires several registers to be initialized. The GDT and IDT base registers must refer to a valid GDT and IDT. After executing the LMSW instruction to set PE, the MBL 80286 must immediately execute an intra-segment JMP instruction to clear the instruction queue of instructions decoded in real address mode.

To force the MBL 80286 CPU registers to match the initial protected mode state assumed by software, execute a JMP instruction with a selector referring to the initial TSS used in the system. This will load the task register, local descriptor table register, segment registers and initial general register state. The TR should point at a valid TSS since any task switch operation involves saving the current task state.

SYSTEM INTERFACE

The MBL 80286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines and/or timing and loading of signals. The MBL 80286 family includes several devices to generate standard system buses such as the IEEE 796 standard Multibus^{TM*}.

Bus Interface Signals and Timing

The MBL 80286 microsystem local bus interfaces the MBL 80286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The MBL 80286 CPU, MBL 82284 clock generator, MBL 82288 bus controller, Intel 82289 bus arbiter, MBL 8286/7 transceivers, and MBL 8282/3 latches provide a buffered and decoded system bus interface. The MBL 82284 generates the system clock and synchronizes $\overline{\text{READY}}$ and RESET. The MBL 82288 converts bus operation status encoded by the MBL 80286 into command and bus control signals. The 82289 bus arbiter generates Multibus bus arbitration signals. These components can provide the timing and electrical power drive levels required for most system bus interfaces including the Multibus.

Physical Memory and I/O Interface

A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address.

Byte transfers occur on either half of the 16-bit local data bus. Even bytes are accessed over D7–D0 while odd bytes

* Multibus is a patented bus of Intel.

are transferred over D15–D8. Even-addressed words are transferred over D15–D0 in one bus cycle, while odd-addressed words require two bus operations. The first transfers data on D15–D8, and the second transfers data on D7–D0. Both byte data transfers occur automatically, transparent to software.

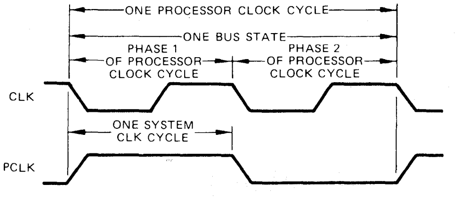
Two bus signals, A0 and $\overline{\text{BHE}}$, control transfers over the lower and upper halves of the data bus. Even address byte transfers are indicated by A0 LOW and $\overline{\text{BHE}}$ HIGH. Odd address byte transfers are indicated by A0 HIGH and $\overline{\text{BHE}}$ LOW. Both A0 and $\overline{\text{BHE}}$ are LOW for even address word transfers.

The I/O address space contains 64K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte wide peripheral devices may be attached to either the upper or lower byte of the data bus. Byte-wide I/O devices attached to the upper data byte (D15–D8) are accessed with odd I/O addresses. Devices on the lower data byte are accessed with even I/O addresses. An interrupt controller such as MBL 8259A must be connected to the lower data byte (D7–D0) for proper return of the interrupt vector.

Bus Operation

The MBL 80286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The MBL 82284 clock generator output (PCLK) identifies the next phase of the processor clock. (See Fig. 21.)

Fig. 21 – SYSTEM AND PROCESSOR CLOCK RELATIONSHIPS

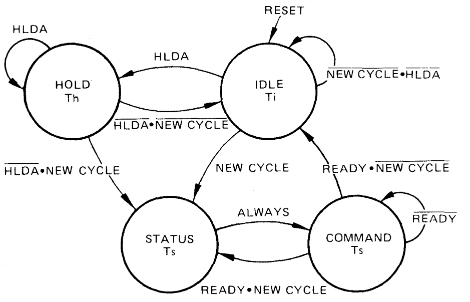

ONE PROCESSOR CLOCK CYCLE
ONE BUS STATE
PHASE 1 OF PROCESSOR CLOCK CYCLE
PHASE 2 OF PROCESSOR CLOCK CYCLE
CLK
ONE SYSTEM CLK CYCLE
PCLK

Six types of bus operations are supported; memory read, memory write, I/O read, I/O write, interrupt ackowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The MBL 80286 bus has three basic states: idle (Ti), send status (Ts), and perform command (Tc). The MBL 80286 CPU also has a fourth local bus state called hold (Th). Th indicates that the MBL 80286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. Fig. 22 shows the four MBL 80286 local bus states and allowed transitions.

Fig. 22 – MBL 80286 BUS STATES



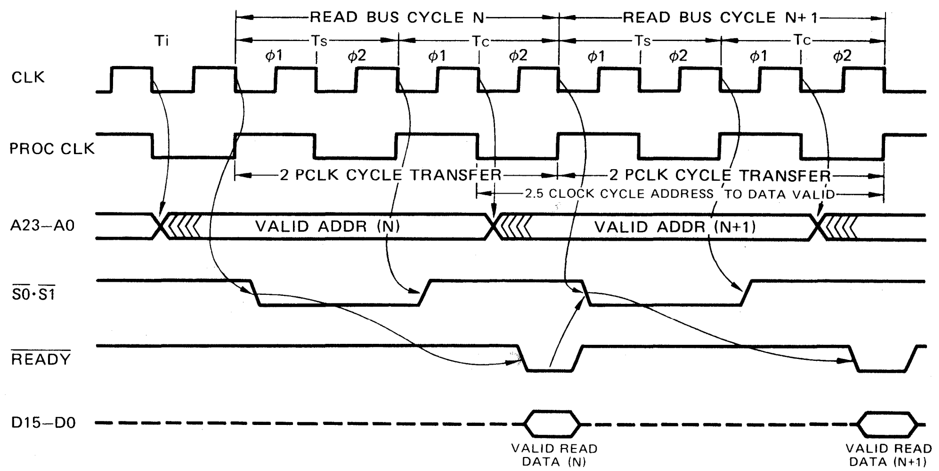
Bus States

The idle (Ti) state indicates that no data transfers are in progress or requested. The first active state Ts is signaled by status line $\overline{\text{S1}}$ or $\overline{\text{S0}}$ going LOW and identifying phase 1 of the processor clock. During Ts, the command encoding, the address, and data (for a write operation) are available on the MBL 80286 output pins. The MBL 82288 bus controller decodes the status signals and generates Multibus compatible read/write command and local transceiver control signals.

After Ts, the perform command (Tc) state is entered. Memory or I/O devices respond to the bus operation during Tc, either transferring read data to the CPU or accepting write data. Tc states may be repeated as often as necessary to assure sufficient time for the memory or I/O device to respond. The $\overline{\text{READY}}$ signal determines whether Tc is repeated. A repeated Tc state is called a wait state.

During hold (Th), the MBL 80286 will float all address, data, and status output pins enabling another bus master to use the local bus. The MBL 80286 HOLD input signal is used to place the MBL 80286 into the Th state. The MBL 80286 HLDA output signal indicates that the CPU has entered Th.

Fig. 23 – BASIC BUS CYCLE



PIPELINING: VALID ADDRESS (N+1) AVAILABLE IN LAST PHASE OF BUS CYCLE (N).

Pipelined Addressing

The MBL 80286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows a new bus operation to be initiated every two processor cycles, while allowing each individual bus operation to last for three processor cycles.

The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decode and routing logic can operate in advance of the next bus operation. External address latches may hold the address stable for the entire bus operation, and provide additional AC and DC buffering.

The MBL 80286 does not maintain the address of the current bus operation during all Tc states. Instead, the address for the next bus operation may be emitted during phase 2 of any Tc. The address remains valid during phase 1 of the first Tc to guarantee hold time, relative to ALE, for the address latch inputs.

Bus Control Signals

The MBL 82288 bus controller provides control signals; address latch enable (ALE), Read/Write commands, data transmit/receive (DT/$\overline{R}$), and data enable (DEN) that control the address latches, data transceivers, write enable, and output enable for memory and I/O systems.

The Address Latch Enable (ALE) output determines when the address may be latched. ALE provides at least one system CLK period of address hold time from the end of the previous bus operation until the address for the next bus operation appears at the latch outputs. This address hold time is required to support Multibus®* and common memory systems.

The data bus transceivers are controlled by MBL 82288 outputs Data Enable (DEN) and Data Transmit/Receive (DT/$\overline{R}$). DEN enables the data transceivers; while DT/$\overline{R}$ controls transceiver direction. DEN and DT/$\overline{R}$ are timed to prevent bus contention between the bus master, data bus transceivers, and system data bus transceivers.

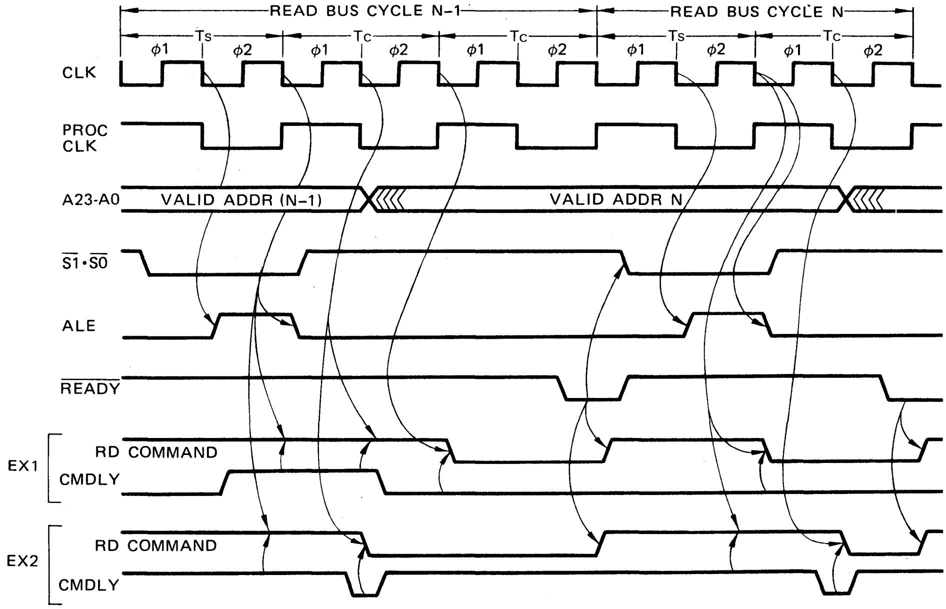
Command Timing Controls

Two system timing customization options, command extension and command delay, are provided on the MBL 80286 local bus.

Command extension allows additional time for external devices to respond to a command and is analogous to inserting wait states on the MBL 80286. External logic can control the duration of any bus operation such that the operation is only as long as necessary. The $\overline{READY}$ input signal can extend any bus operation for as long as necessary.

* Multibus is a patented bus of Intel.

Fig. 24 – CMDLY CONTROLS THE LEADING EDGE OF COMMAND SIGNAL



Command delay allows an increase of address or write data setup time to system bus command active for any bus operation by delaying when the system bus command becomes active. Command delay is controlled by the MBL 82288 CMDLY input. After Ts, the bus controller samples CMDLY at each failing edge of CLK. If CMDLY is HIGH, the MBL 82288 will not activate the command signal. When CMDLY is LOW, the MBL 82288 will activate the command signal. After the command becomes active, the CMDLY input is not sampled.

When a command is delayed, the available response time from command active to return read data or accept write data is less. To customize system bus timing, an address decoder can determine which bus operations require delaying the command. The CMDLY input does not affect the timing of ALE, DEN, or DT/$\overline{R}$.

Fig. 24 illustrates four uses of CMDLY. Example 1 shows delaying the read command two system CLKs for cycle N-1 and no delay for cycle N, and example 2 shows delaying the read command one system CLK for cycle N-1 and one system CLK delay for cycle N.

Bus Cycle Termination

At maximum transfer rates, the MBL 80286 bus alternates between the status and command states. The bus status signals become inactive after Ts so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of Tc exists on the MBL 80286 local bus. The bus master and bus controller enter Tc directly after Ts and continue executing Tc cycles until terminated by $\overline{\text{READY}}$.

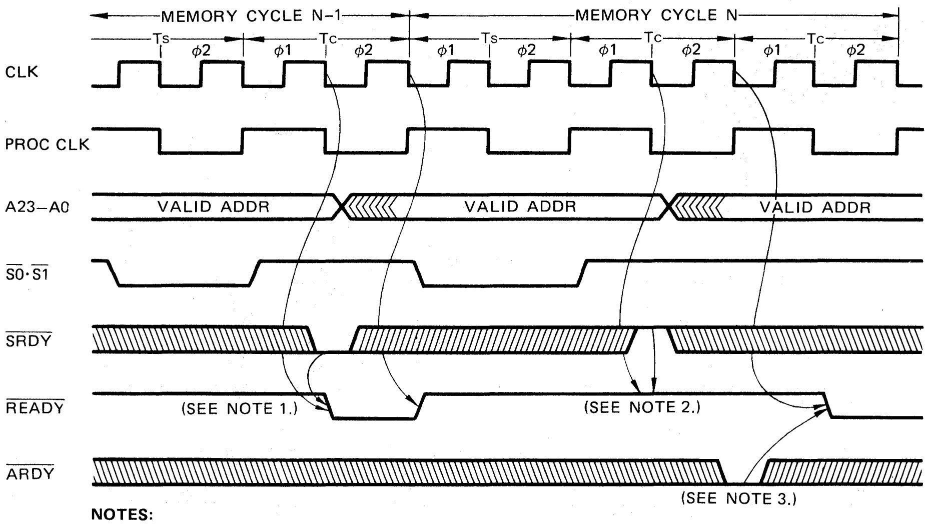
$\overline{\text{READY}}$ Operation

The current bus master and MBL 82288 bus controller terminate each bus operation simultaneously to achieve maximum bus operation bandwidth. Both are informed in advance by $\overline{\text{READY}}$ active (open-collector output from MBL 82284) which identifies the last Tc cycle of the current bus operation. The bus master and bus controller must see the same sense of the $\overline{\text{READY}}$ signal, thereby requiring $\overline{\text{READY}}$ be synchronous to the system clock.

Synchronous Ready

The MBL 82284 clock generator provides $\overline{\text{READY}}$ synchronization from both synchronous and asynchronous sources (see Fig. 25). The synchronous ready input ($\overline{\text{SRDY}}$)

Fig. 25 – SYNCHRONOUS AND ASYNCHRONOUS READY



NOTES:
1. $\overline{\text{SRDYEN}}$ is active low.
2. If $\overline{\text{SRDYEN}}$ is high, the state of $\overline{\text{SRDY}}$ will not effect $\overline{\text{READY}}$
3. $\overline{\text{ARDYEN}}$ is active low.

of the clock generator is sampled with the failing edge of CLK at the end of phase 1 of each Tc. The state of $\overline{\text{SRDY}}$ is then broadcast to the bus master and bus controller via the $\overline{\text{READY}}$ output line.

Asynchronous Ready

Many systems have devices or subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the MBL 82284 $\overline{\text{SRDY}}$ setup and hold time requirements. But the MBL 82284 asynchronous ready input ($\overline{\text{ARDY}}$) is designed to accept such signals. The $\overline{\text{ARDY}}$ input is sampled at the beginning of each Tc cycle by MBL 82284 synchronization logic. This provides one system CLK cycle time to resolve its value before broadcasting it to the bus master and bus controller.

$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ must be HIGH at the end of Ts. $\overline{\text{ARDY}}$ cannot be used to terminate bus cycle with no wait states.

Each ready input of the MBL 82284 has an enable pin ($\overline{\text{SRDYEN}}$ and $\overline{\text{ARDYEN}}$) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. Address decode logic usually selects whether the current bus operation should be terminated by $\overline{\text{ARDY}}$ or $\overline{\text{SRDY}}$.

Data Bus Control

Fig. 26, 27, and 28 show how the DT/$\overline{\text{R}}$, DEN, data bus, and address signals operate for different combinations of read, write, and idle bus operations. DT/$\overline{\text{R}}$ goes active (LOW) for a read operation. DT/$\overline{\text{R}}$ remains HIGH before, during, and between write operations.

The data bus is driven with write data during the second phase of Ts. The delay in write data timing allows the read data drivers, from a previous read cycle, sufficient time to enter 3-state OFF before the MBL 80286 CPU begins driving the local data bus for write operations. Write data will always remain valid for one system clock past the last Tc to provide sufficient hold time for Multibus or other similar memory or I/O systems. During write-read or write-idle sequences the data bus enters 3-state OFF during the second phase of the processor cycle after the last Tc. In a write-write sequence the data bus does not enter 3-state OFF between Tc and Ts.

Bus Usage

The MBL 80286 local bus may be used for several functions: instruction data transfers, data transfers by other bus masters, instruction fetching, processor extension data transfers, interrupt acknowledge, and halt/shutdown. This section describes local bus activities which have special signals or requirements.

Fig. 26 – BACK TO BACK READ-WRITE CYCLES

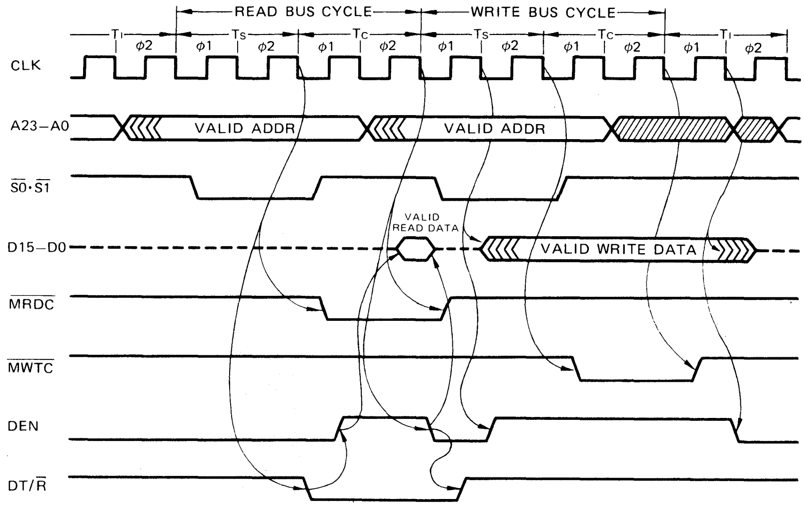


Fig. 27 – BACK TO BACK WRITE-READ CYCLES

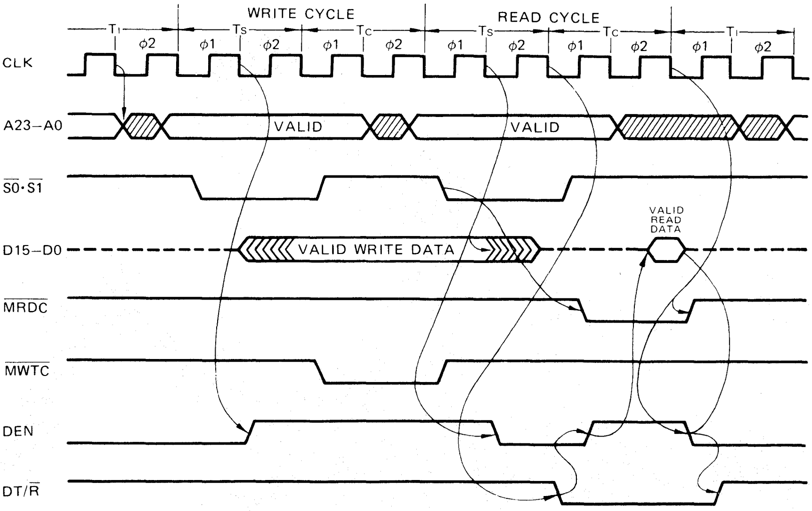
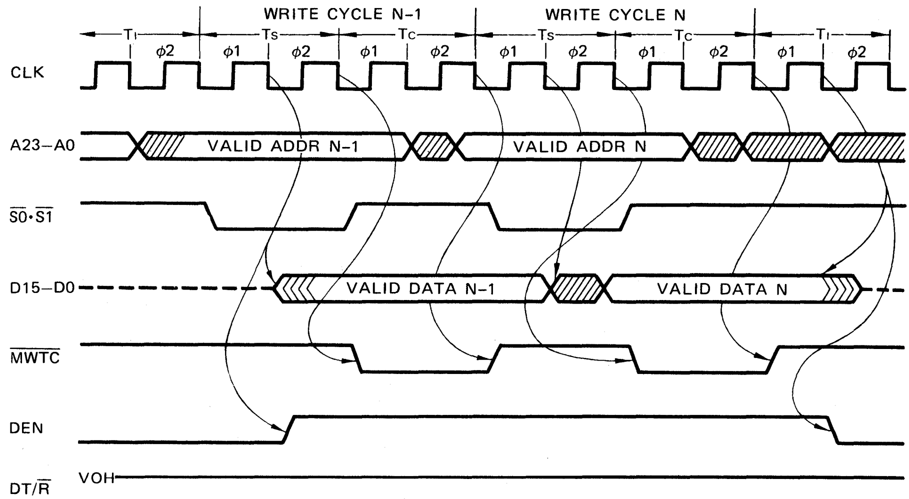


Fig. 28 – BACK TO BACK WRITE-WRITE CYCLES



HOLD and HLDA

HOLD and HLDA allow another bus master to gain control of the local bus by placing the MBL 80286 bus into the Th state. The sequence of events required to pass control between the MBL 80286 and another local bus master are shown in Fig. 29.

In this example, the MBL 80286 is initially in the Th state as signaled by HLDA being active. Upon leaving Th, as signaled by HLDA going inactive, a write operation is started. During the write operation another local bus master requests the local bus from the MBL 80286 as shown by the HOLD signal. After completing the write operation, the MBL 80286 performs one Ti bus cycle, to guarantee write data hold time, then enters Th as signaled by HLDA going active.

The CMDLY signal and ARDY ready are used to start and stop the write bus command, respectively. Note that SRDY must be inactive or disabled by SRDYEN to guarantee ARDY will terminate the cycle.

Instruction Fetching

The MBL 80286 Bus Unit (BU) will fetch instructions ahead of the current instruction being executed. This activity is called prefetching. It occurs when the local bus would otherwise be idle and obeys the following rules:

A prefetch bus operation starts when at least two bytes of the 6-byte prefetch queue are empty.

The prefetcher normally performs word prefetches independent of the byte alignment of the code segment base in physical memory.

The prefetcher will perform only a byte code fetch operation for control transfers to an instruction beginning on a numerically odd physical address.

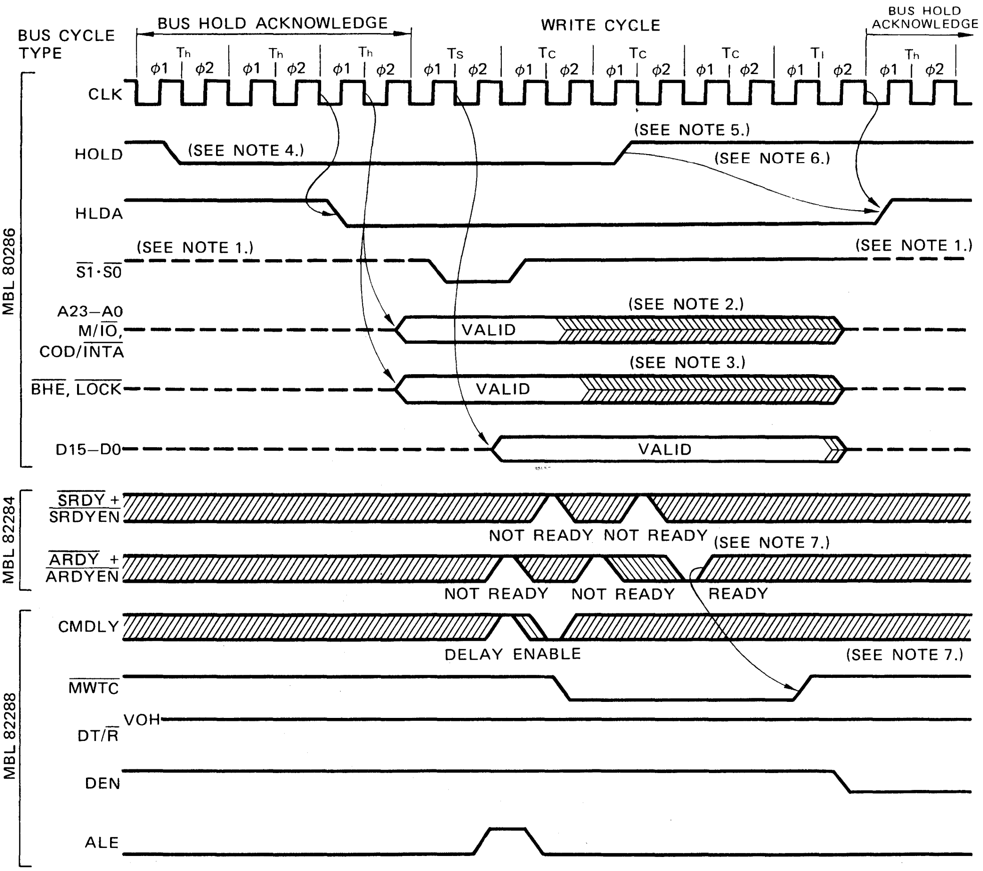
Prefetching stops whenever a control transfer or HLT instruction is decoded by the IU and placed into the instruction queue.

In real address mode, the prefetcher may fetch up to 6 bytes beyond the last control transfer or HLT instruction in a code segment.

In protected mode, the prefetcher will never cause a segment overrun exception. The prefetcher stops at the last physical memory word of the code segment. Exception 13 will occur if the program attempts to execute beyond the last full instruction in the code segment.

If the last byte of a code segment appears on an even physical memory address, the prefetcher will read the next physical byte of memory (perform a word code fetch). The value of this byte is ignored and any attempt to execute if causes exception 13.

Fig. 29 – MULTIBUS WRITE TERMINATED BY ASYNCHRONOUS READ WITH BUS HOLD



Ts = STATUS CYCLE
Tc = COMMAND CYCLE

NOTES:

1. Status lines are not driven by MBL 80286, yet remain high due to pullup resistors in MBL 82288 and Intel 82289 during HOLD state.
2. Address, M/IO and COD/INTA may start floating during any Tc depending on when internal MBL 80286 bus arbiter decides to release bus to external HOLD. The float starts in φ2 of Tc.
3. BHE and LOCK may start floating after the end of any Tc depending on when internal MBL 80286 bus arbiter decides to release bus to external HOLD. The float starts in φ1 of Tc.
4. The minimum HOLD to HLDA times is shown. Maximum is one Th longer.
5. The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending is shown.
6. The minimum HOLD to HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine status (i.e., Interrupts, Waits, Lock, etc.)
7. Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state is ignored after ready is signaled via the asynchronous input.

Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), 00FA(H), and 00FC(H) which are part of the I/O port address range reserved by intel. An ESC instruction with Machine Status Word bits EM = 0 and TS = 0 will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand trarsfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

Interrupt Acknowledge Sequence

Fig. 30 illustrates an interrupt acknowledge sequence performed by the MBL 80286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master MBL 8259A Programmable Interrupt Controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight bit vector is read on D0-D7 of the MBL 80286 during the second INTA bus operation to select an interrupt handler routine from the interrupt table.

The Master Cascade Enable (MCE) signal of the MBL 82288 is used to enable the cascade address drivers, during INTA bus operations (See Fig. 30), onto the local address bus for distribution to slave interrupt controllers via the system address bus. The MBL 80286 emits the $\overline{\text{LOCK}}$ signal (active LOW) during Ts of the first INTA bus operation. A local bus "hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the MBL 80286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the MBL 8259A. The second INTA bus operation must always have at least one extra Tc state added via logic controlling $\overline{\text{READY}}$. A23-A0 are in 3-state OFF until after the first Tc state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra Tc state allows time for the MBL 80286 to resume driving the address lines for subsequent bus operations.

Local Bus Usage Priorities

The MBL 80286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest) Any transfers which assert $\overline{\text{LOCK}}$ either explicitly (via the LOCK instruction prefix) or implicitly (i.e. segment descriptor access, interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd aligned word operand.

The second or third cycle of a processor extension data transfer.

Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

Data transfer performed by EU as part of an instruction.

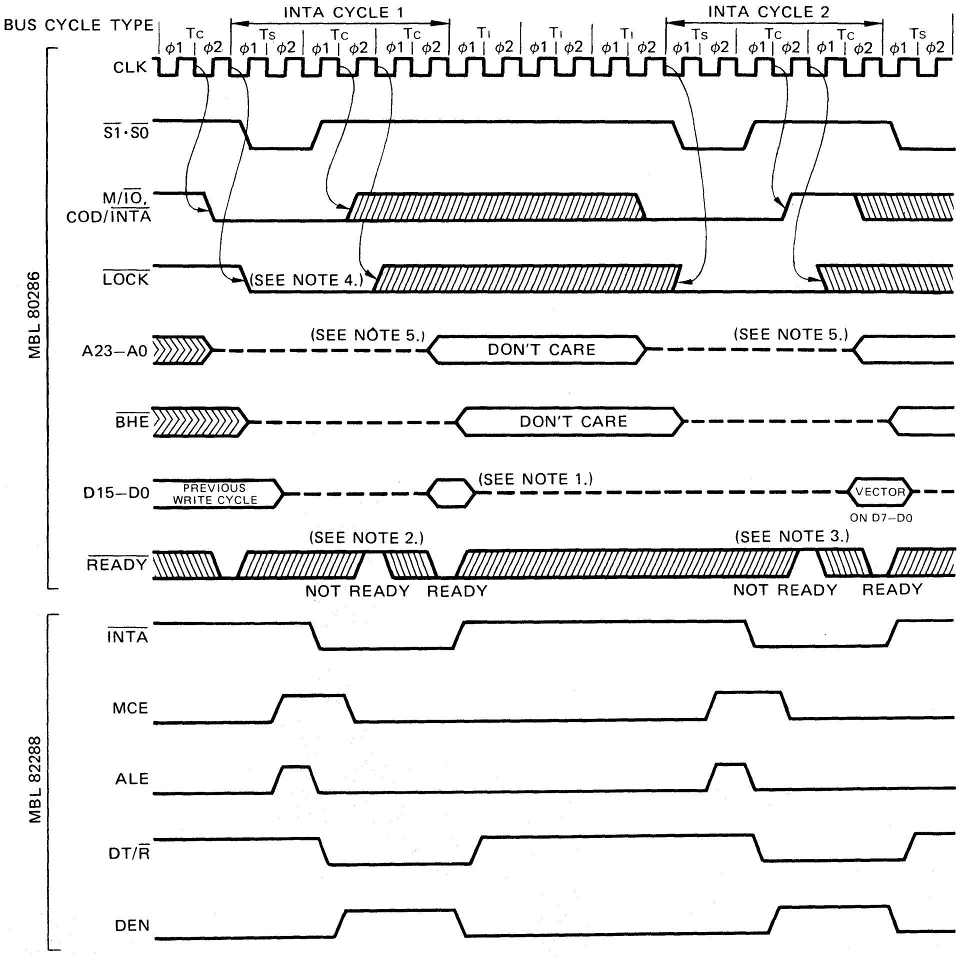
(Lowest) An instruction prefetch request from BU. The EU will inhibit prefetching two processor clocks in advance of any data transfers to minimize waiting by EU for a prefetch to finish.

Halt or Shutdown Cycles

The MBL 80286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to a HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when $\overline{\text{S1}}$, $\overline{\text{S0}}$ and COD/$\overline{\text{INTA}}$ are LOW and M/$\overline{\text{IO}}$ is HIGH. A1 HIGH indicates halt, and A1 LOW indicates shutdown. The MBL 82288 bus controller does not issue ALE, nor is $\overline{\text{READY}}$ required to terminate a halt or shutdown bus operation.

During halt or shutdown, the MBL 80286 may service PEREQ or HOLD requests. A processor extension segment overrrun exception during shutdown will inhibit further service of PEREQ. Either NMI or RESET will force the MBL 80286 out of either halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the MBL 80286 out of halt.

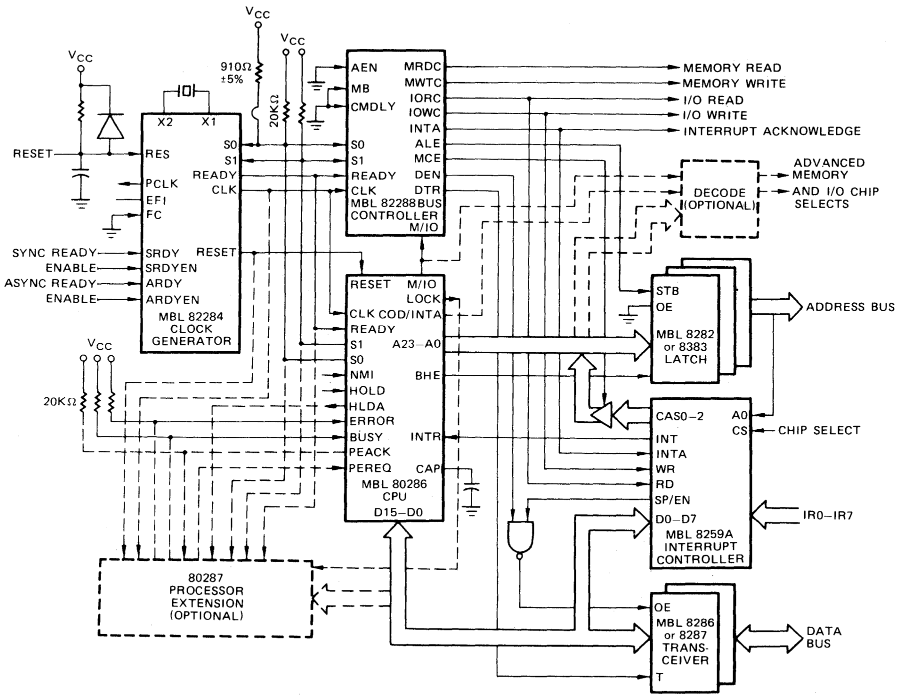
Fig. 30 – INTERRUPT ACKNOWLEDGE SEQUENCE



NOTES:

1. Data is ignored.
2. First INTA cycle should have at least one wait state inserted to meet MBL 8259A minimum INTA pulse width.
3. Second INTA cycle must have at least one wait state inserted since the CPU will not drive A23–A0, BHE, and LOCK until after the first Tc state. The CPU imposed one/clock delay prevents bus contention between cascade address buffer being disabled by MCE ↓ and address outputs. Without the wait state, the MBL 80286 address will not be valid for a memory cycle started immediately after the second INTA cycle. The MBL 8259A also requires one wait state for minimum INTA pulse width.
4. LOCK is active for the first INTA cycle to prevent the Intel 82289 from releasing the bus between INTA cycles in a multi-master system.
5. A23–A0 exits 3-state OFF during φ2 of the second Tc in the INTA cycle.

Fig. 31 – BASIC MBL 80286 SYSTEM CONFIGURATION



SYSTEM CONFIGURATIONS

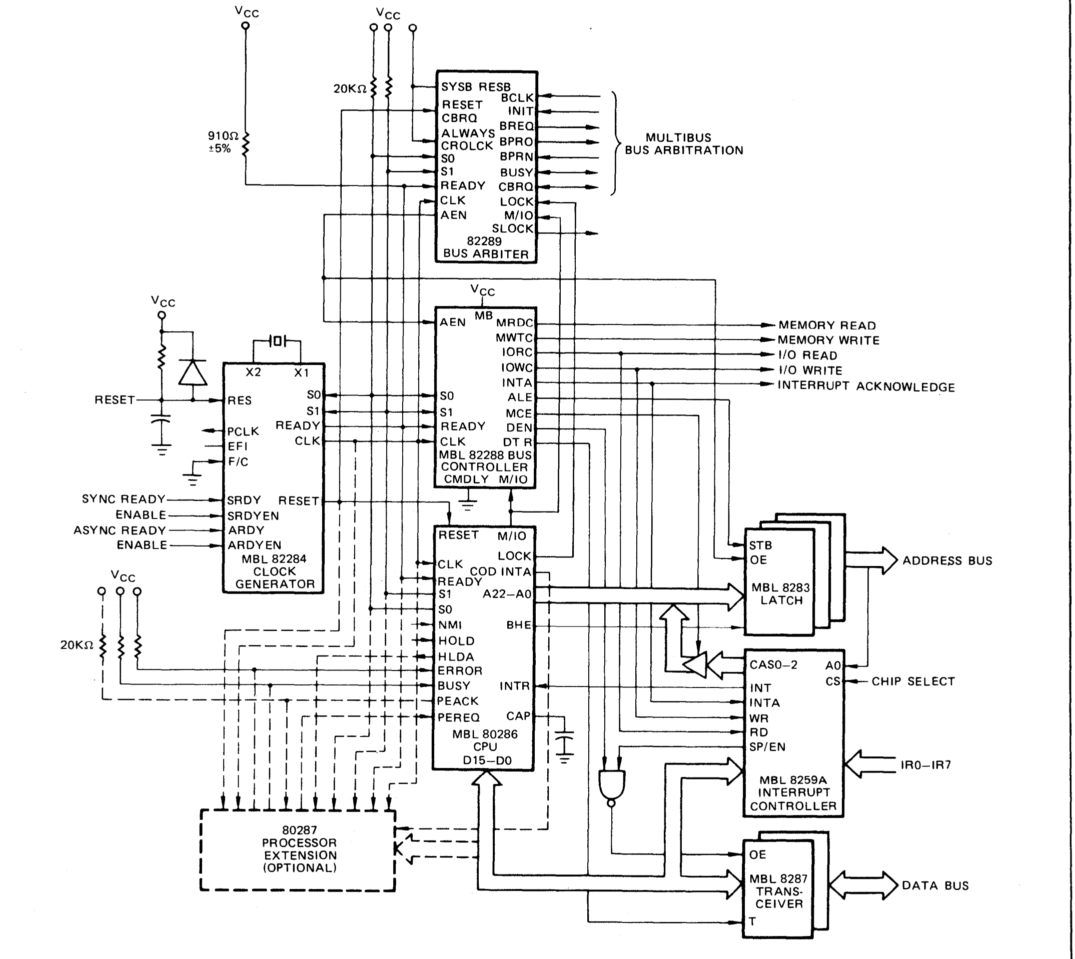
The versatile bus structure of the MBL 80286 microsystem, with a full complement of support chips, allows flexible configuration of a wide range of systems. The basic configuration, shown in Fig. 31, is similar to an MBL 8086 maximum mode system. It includes the CPU plus an MBL 8259A interrupt controller, MBL 82284 clock generator, and the MBL 82288 bus controller. The MBL 8086 latches (MBL 8282 and 8283) and transceivers (MBL 8286 and 8287) may be used in an MBL 80286 microsystem.

As indicated by the dashed lines in Fig. 31, the ability to add processor extensions is an integral feature of MBL 80286 microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrent with CPU execution of other instructions. Full system integrity is maintained because the MBL 80286 supervises all data transfers and instruction execution for the processor extension.

The MBL 80286 and Intel 80287 numeric data processor which includes the 80287 numeric processor extension (NPX) uses this interface. The MBL 80286 and Intel 80287 microsystem has all the instructions and data types of an MBL 8086 and Intel 8087 or MBL 8088 and Intel 8087 system. The 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the MBL 80286 protection mechanism.

The MBL 80286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the MBL 8282/3's by ALE during the middle of a Ts cycle. The latched chip select and address information remains stable during the bus operation while the next cycles address is being decoded and propagated into the system. Decode logic can be implemented with a high speed bipolar PROM.

Fig. 32 – MULTIBUS®* SYSTEM BUS INTERFACE

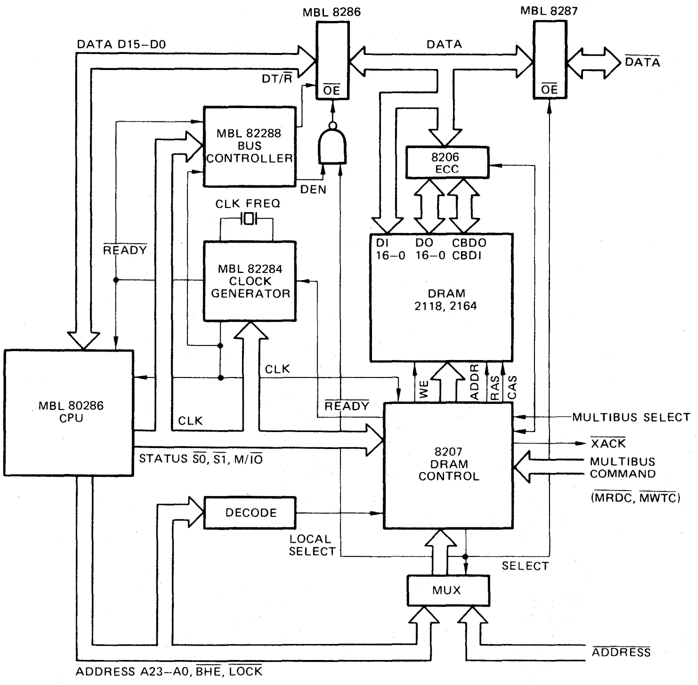


The optional decode logic shown in Fig. 31 takes advantage of the overlap between address and data of the MBL 80286 bus cycle to generate advanced memory and IO-select signals. This minimizes system performance degradation caused by address propagation and decode delays. In addition to selecting memory and I/O, the advanced selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/$\overline{\text{INTA}}$ and M/$\overline{\text{IO}}$ signals are applied to the decode logic to distinguish between interrupt, I/O, code and data bus cycles.

By adding the 82289 bus arbiter chip the MBL 80286 provides a Multibus system bus interface as shown in Fig. 32. The ALE output of the MBL 82288 for the MULTIBUS bus is connected to its CMDLY input to delay the start of commands one system CLK as required to meet MULTIBUS address and write data setup times. This arrangement will add at least one extra Tc state to each bus operation which uses the MULTIBUS.

* MULTIBUS is a patented bus of Intel.

Fig. 33 – MBL 80286 SYSTEM CONFIGURATION WITH DUAL-PORTED MEMORY



A second MBL 82288 bus controller and additional latches and transceivers could be added to the local bus of Fig. 32. This configuration allows the MBL 80286 to support an on-board bus for local memory and peripherals, and the MULTIBUS for system bus interfacing.

Fig. 33 shows the addition of dual ported dynamic memory between the MULTIBUS system bus and the MBL 80286 local bus. The dual port interface is provided by the 8207 Dual Port DRAM Controller. The 8207 runs synchronously with the CPU to maximize throughput for local memory

Table 16 – MBL 80286 SYSTEMS RECOMMENDED PULL UP RESISTOR VALUES

MBL 80286 Pin and Name	Pullup Value	Purpose
4 – $\overline{\text{S1}}$	20kΩ ± 10%	Pull $\overline{\text{S0}}$, $\overline{\text{S1}}$, and $\overline{\text{PEACK}}$ inactive during MBL 80286 hold periods
5 – $\overline{\text{S0}}$		
6 – $\overline{\text{PEACK}}$		
53 – $\overline{\text{ERROR}}$	20kΩ ± 10%	Pull $\overline{\text{ERROR}}$ and $\overline{\text{BUSY}}$ inactive when 80287 not present (or temporarily removed from socket)
54 – $\overline{\text{BUSY}}$		
63 – $\overline{\text{READY}}$	910Ω ± 5%	Pull $\overline{\text{READY}}$ inactive within required minimum time (C_L = 150pF, $I_R \leq$ 7mA)

references. It also arbitrates between requests from the local and system buses and performs functions such as refresh, initialization of RAM, and read/modify/write cycles. The 8207 combined with the 8206 Error Checking and Correction memory controller provide for single bit error correction. The dual-ported memory can be combined with a standard MULTIBUS system bus interface to maximize performance and protection in multiprocessor system configurations.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0 to +7V
Power Dissipation	3.3 Watt

***NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: *Specifications contained within the following tables are subject to change.*

D.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to +55°C, or T_{CASE} = 0°C to +85°C)

Symbol	Parameter	MBL 80286-6 (6 MHz)		MBL 80286-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
V_{IL}	Input LOW Voltage	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V	
V_{ILC}	CLK Input LOW Voltage	-0.5	0.6	-0.5	0.6	V	
V_{IHC}	CLK Input HIGH Voltage	3.8	V_{CC}+0.5	3.8	V_{CC}+0.5	V	
V_{OL}	Output LOW Voltage		0.45		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output HIGH Voltage	2.4		2.4		V	I_{OH} = -400μA
I_{LI}	Input Leakage Current		±10		±10	μA	$0V \leqq V_{IN} \leqq V_{CC}$
I_{IL}	Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ pins	30	500	30	500	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current		±10		±10	μA	$0.45V \leqq V_{OUT} \leqq V_{CC}$
I_{LO}	Output Leakage Current		±1		±1	mA	$0V \leqq V_{OUT} \leqq 0.45V$
I_{CC}	Supply Current (turn on, 0°C)		600		600	mA	Note 1
C_{CLK}	CLK Input Capacitance		20		20	pF	F_C = 1MHz
C_{IN}	Other Input Capacitance		10		10	pF	F_C = 1MHz
C_O	Input/Output Capacitance		20		20	pF	F_C = 1MHz

NOTE 1: Low temperature is worst case.

A.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to + 55°C, or T_{CASE} = 0°C to + 85°C)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

Symbol	Parameter	MBL 80286-6 (6 MHz)		MBL 80286-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
1	System Clock (CLK) Period	83	250	62	250	ns	
2	System Clock (CLK) LOW Time	20	225	15	225	ns	at 1.0V
3	System Clock (CLK) HIGH Time	25	230	25	235	ns	at 3.6V
17	System Clock (CLK) Rise Time		10		10	ns	1.0V to 3.6V
18	System Clock (CLK) Fall Time		10		10	ns	3.6V to 1.0V
4	Asynch. Inputs Setup Time	30		20		ns	Note 1
5	Asynch. Inputs Hold Time	30		20		ns	Note 1
6	RESET Setup Time	33		28		ns	
7	RESET Hold Time	5		5		ns	
8	Read Data Setup Time	20		10		ns	
9	Read Data Hold Time	8		8		ns	
10	$\overline{\text{READY}}$ Setup Time	50		38		ns	
11	$\overline{\text{READY}}$ Hold Time	35		25		ns	
12	Status/$\overline{\text{PEACK}}$ Valid Delay	1	55	1	40	ns	Note 2, Note 3
13	Address Valid Delay	1	80	1	60	ns	Note 2, Note 3
14	Write Data Valid Delay	0	65	0	50	ns	Note 2, Note 3
15	Address/Status/Data Float Delay	0	80	0	50	ns	Note 2, Note 4
16	HLDA Valid Delay	0	80	0	50	ns	Note 2, Note 3
19	Address Valid to Status Valid Setup Time	—		38			Note 3, 5, and 6

NOTE 1: Asychronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.

NOTE 2: Delay from 0.8V on the CLK, to 0.8V or 2.0V or float on the output as appropriate for valid or floating condition.

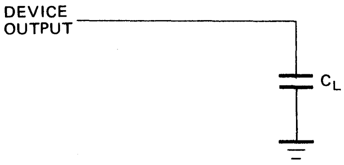
NOTE 3: Output load: C_L = 100pF.

NOTE 4: Float condition occurs when output current is less than I_{LO} in magnitude.

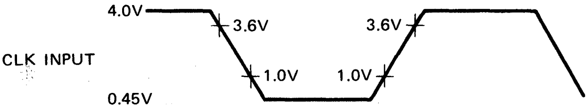
NOTE 5: Delay measured from address either reaching 0.8V or 2.0V (Valid) to status going active reaching 2.0V or status going inactive reaching 0.8V.

NOTE 6: For load capacitance of 10pF on Status/$\overline{\text{PEACK}}$ lines, subtract typically 7ns for 8MHz spec.

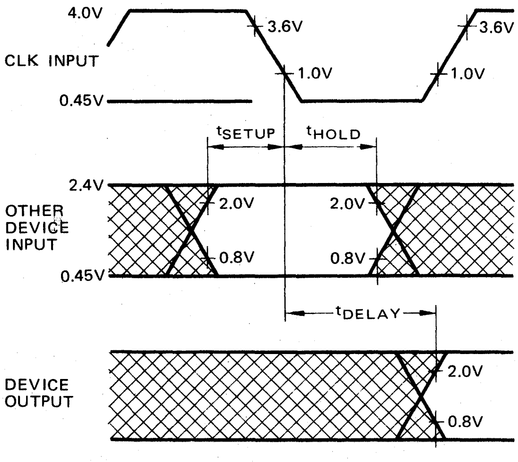
NOTE 7: AC Test Loading on Outputs



NOTE 8: AC Drive and Measurement Points – CLK Input

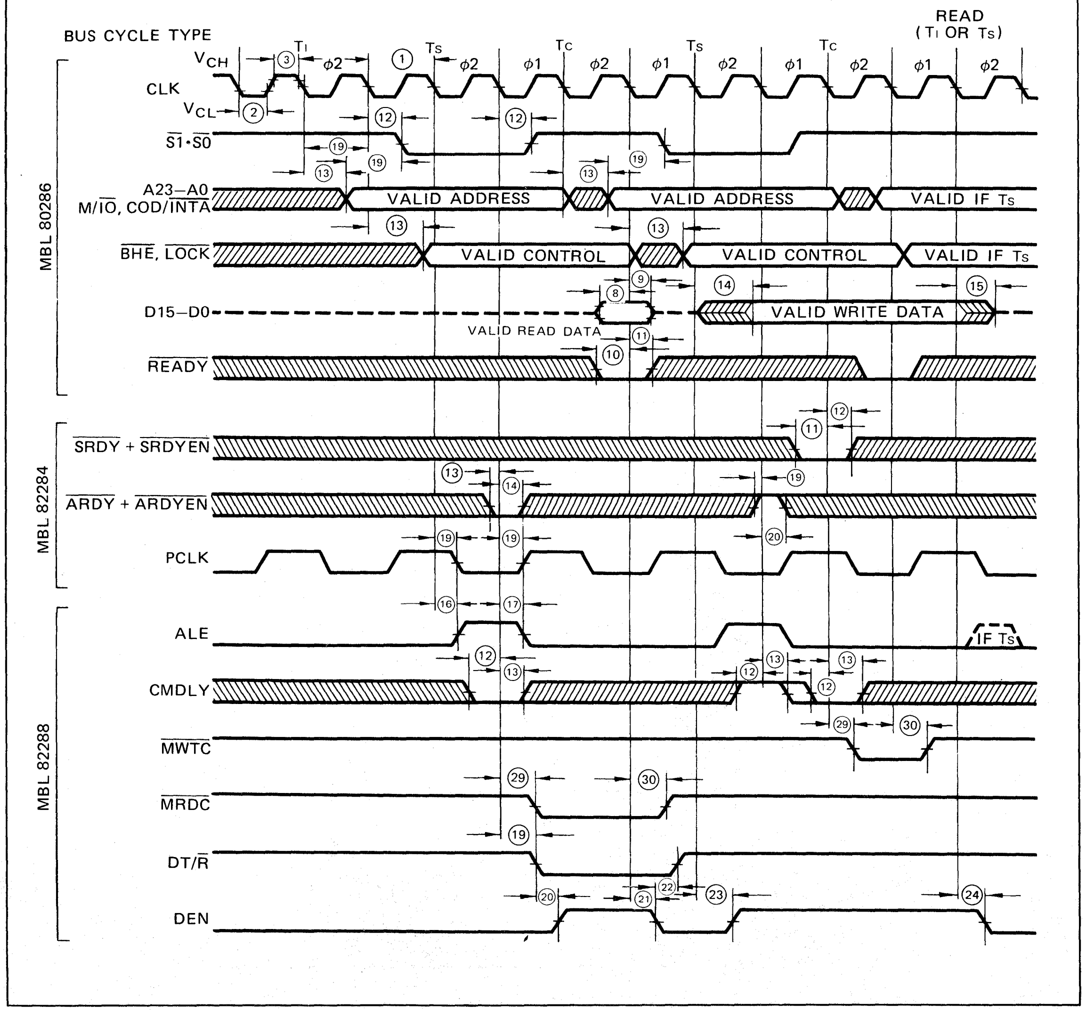


NOTE 9: AC Setup, Hold and Delay Time Measurement – General



WAVEFORMS

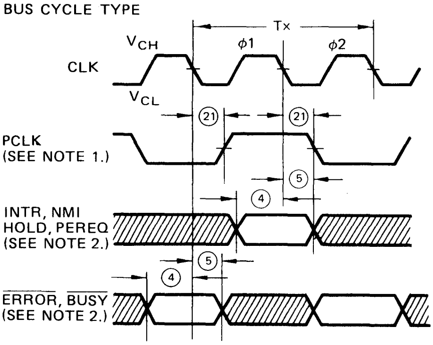
MAJOR CYCLE TIMING



NOTE: For timing requirements of the MBL 82284 and MBL 82288, refer to the data sheets of the MBL 82284 and MBL 82288.

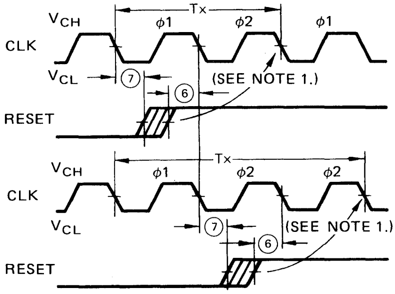
WAVEFORMS (Continued)

MBL 80286 ASYNCHRONOUS INPUT SIGNAL TIMING


BUS CYCLE TYPE
Tx
VCH
φ1
φ2
CLK
VCL
21
21
PCLK (SEE NOTE 1.)
5
4
INTR, NMI HOLD, PEREQ (SEE NOTE 2.)
5
4
ERROR, BUSY (SEE NOTE 2.)

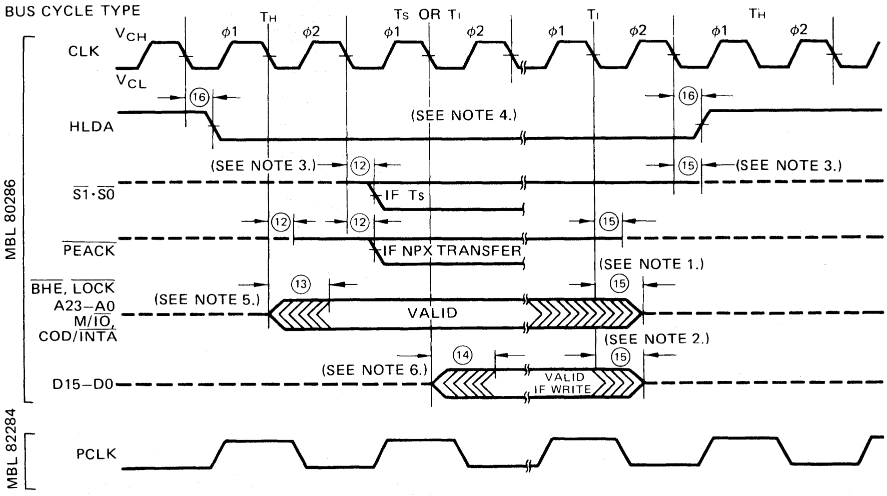
NOTES:
1. PCLK indicates which processor cycle phase will occur on the next CLK, PCLK may not indicate the correct phase until the first bus cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

MBL 80286 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE



NOTE:
When RESET meets the setup time shown, the next CLK will start or repeat φ2 of a processor cycle.

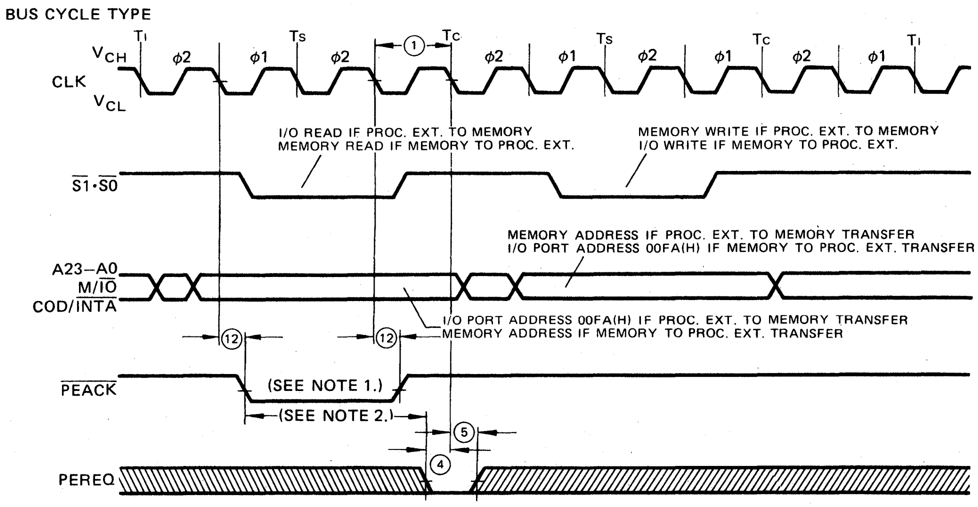
EXITING AND ENTERING HOLD



NOTES:
1. These signals may not be driven by the MBL 80286 during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before TI in the diagram was a write TC.
3. The MBL 80286 floats its status pins during TH. External 20kΩ resistors keep these signals high (see Table 16).
4. For HOLD request set up to HLDA, refer to Fig. 29.
5. BHE and LOCK are driven at this time but will not become valid until TS.
6. The data bus will remain in 3-state OFF if a read cycle is performed.

WAVEFORMS (Continued)

MBL 80286 PEREQ/$\overline{\text{PEACK}}$ TIMING FOR ONE TRANSFER ONLY


BUS CYCLE TYPE
Ti
Ts
Tc
Ts
Tc
Ti
VCH
VCL
CLK
φ2
φ1
φ2
φ2
φ1
φ2
φ1
φ2
φ1
1
I/O READ IF PROC. EXT. TO MEMORY
MEMORY READ IF MEMORY TO PROC. EXT.
MEMORY WRITE IF PROC. EXT. TO MEMORY
I/O WRITE IF MEMORY TO PROC. EXT.
S1·S0
MEMORY ADDRESS IF PROC. EXT. TO MEMORY TRANSFER
I/O PORT ADDRESS 00FA(H) IF MEMORY TO PROC. EXT. TRANSFER
A23–A0
M/IO
COD/INTA
I/O PORT ADDRESS 00FA(H) IF PROC. EXT. TO MEMORY TRANSFER
MEMORY ADDRESS IF MEMORY TO PROC. EXT. TRANSFER
12
12
PEACK
(SEE NOTE 1.)
(SEE NOTE 2.)
5
4
PEREQ

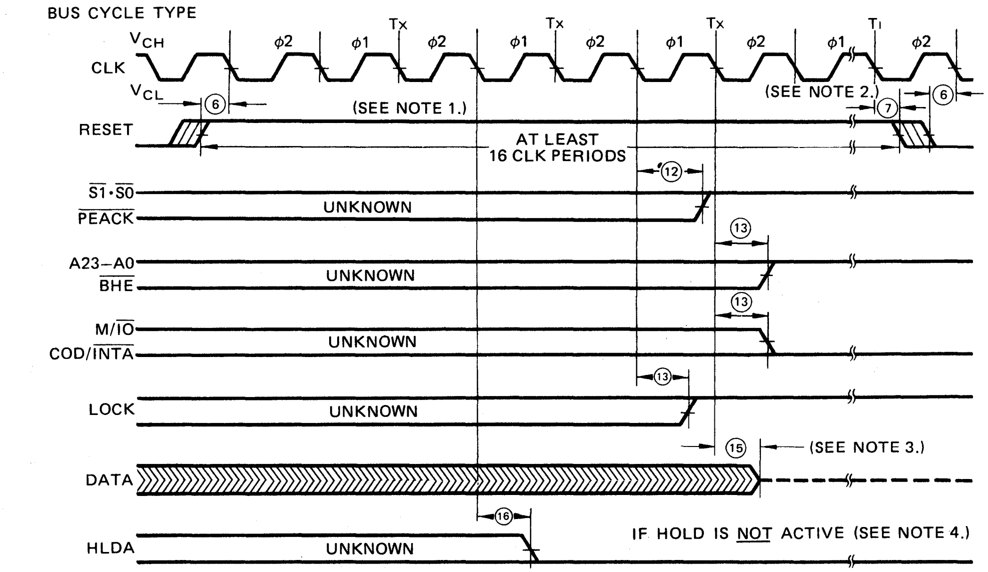
ASSUMING WORD-ALIGNED MEMORY OPERAND. IF ODD ALIGNED, MBL 80286 TRANSFERS TO/FROM MEMORY BYTE-AT-A-TIME WITH MEMORY CYCLES.

NOTES:

1. $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).
2. To prevent a second processor extension data operand transfer, the worst case maximum time (Shown above) is: 3x ① – ⑪ max. – ④ min. The actual, configuration dependent, maximum time is: 3x ① – ⑪ max. – ④ min. + Ax2x ①.
   A is the number of extra Tc states added to either the first or second bus operation of the processor extension data operand transfer sequence.

WAVEFORMS (Continued)

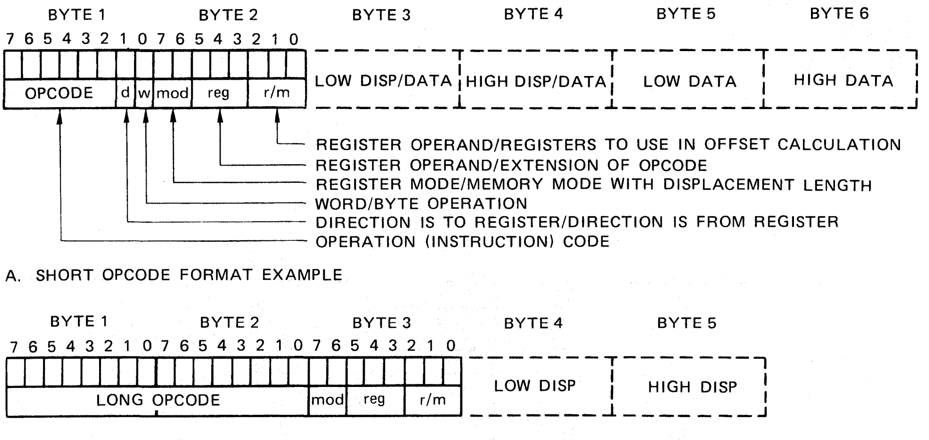
INITIAL MBL 80286 PIN STATE DURING RESET



NOTES:

1. Setup time for RESET ↑ may be violated with the consideration that φ1 of the processor clock may begin one system CLK period later.
2. Setup and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during φ1 or φ2.
3. The data bus is only guaranteed to be in 3-state OFF at the time shown.
4. HOLD is acknowledged during RESET, causing HLDA to go active and the appropriate pins to float. If HOLD remains active while RESET goes inactive, the MBL 80286 remains in HOLD state and will not perform any bus accesses until HOLD is de-activated.

Fig. 35 – MBL 80286 INSTRUCTION FORMAT EXAMPLES



A. SHORT OPCODE FORMAT EXAMPLE

B. LONG OPCODE FORMAT EXAMPLE

MBL 80286 INSTRUCTION SET SUMMARY

Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the MBL 80286. With no delays in bus cycles, the actual clock count of an MBL 80286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

To calculate elapsed times for instruction sequences, multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 8 MHz processor clock has a clock period of 125 nanoseconds and requires a MBL 80286 system clock (CLK input) of 16 MHz.

Instruction Clock Count Assumptions

1. The instruction has been prefetched, decoded, and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
2. Bus cycles do not require wait states.
3. There are no processor extension data transfer or local bus HOLD requests.
4. No exceptions occur during instruction execution.

Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value

Greater refers to positive signed value

Less refers to less positive (more negative) signed values

if d = 1 then to register; if d = 0 then from register

if w = 1 then word instruction; if w = 0 then byte instruction

if s = 0 then 16-bit immediate data form the operand

if s = 1 then an immediate data byte is sign-extended to form the 16-bit operand

x don't care

z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

* = add one clock if offset calculation requires summing 3 elements

n = number of times repeated

m = number by bytes of code in next instruction

Level (L)—Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects, and allowed usage for instructions in both operating modes of the MBL 80286.

REAL ADDRESS MODE ONLY

1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).

2. A segment overrun exception (13) will occur if a word operand reference at offset FFFF(H) is attempted.

3. This instruction may be executed in real address mode to initialize the CPU for protected mode.

4. The IOPL and NT fields will remain 0.

5. Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

EITHER MODE

6. An exception may occur, depending on the value of the operand.

7. $\overline{\text{LOCK}}$ is automatically asserted regardless of the presence or absence of the LOCK instruction prefix.

8. $\overline{\text{LOCK}}$ does not remain active between all operand transfers.

PROTECTED VIRTUAL ADDRESS MODE ONLY

9. A general protection exception (13) will occur if the memory operand can not be used due to either a segment limit or access rights violation. If a stack segment limit is violated, a stack segment overrun exception (12) occurs.

10. For segment load operations, the CPL, RPL, and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the desination, and a segment not-present violation occurs, a stack exception (12) occurs.

11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert $\overline{\text{LOCK}}$ to maintain descriptor integrity in multiprocessor systems.

12. JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.

13. A general protection exception (13) occurs if CPL $\neq 0$.

14. A general protection exception (13) occurs if CPL > IOPL.

15. The IF field of the flag word is not updated if CPL > IOPL. The IOPL field is updated only if CPL = 0.

16. Any violation of privilege rules as applied to the selector operand do not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.

17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer then a processor extension segment overrun exception (9) occurs.

18. The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

MBL 80286 INSTRUCTION SET SUMMARY

					CLOCK COUNT		COMMENTS	
FUNCTION	FORMAT				Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
DATA TRANSFER								
MOV = Move:								
Register to Register/memory	1000100w	mod reg r/m			2,3*	2,3*	2	9
Register/memory to register	1000101w	mod reg r/m			2,5*	2,5*	2	9
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w = 1	2,3*	2,3*	2	9
Immediate to register	1011 w reg	data	data if w = 1		2	2		
Memory to accumulator	1010000w	addr-low	addr-high		5	5	2	9
Accumulator to memory	1010001w	addr-low	addr-high		3	3	2	9
Register/memory to segment register	10001110	mod 0 reg r/m			2,5*	17,19*	2	9,10,11
Segment register to register/memory	10001100	mod 0 reg r/m			2,3*	2,3*	2	9
PUSH = Push:								
Memory	11111111	mod 110 r/m			5*	5*	2	9
Register	01010 reg				3	3	2	9
Segment register	000 reg 110				3	3	2	9
Immediate	011010s0	data	data if s = 0		3	3	2	9
PUSHA = Push All	01100000				17	17	2	9
POP = Pop:								
Memory	10001111	mod 000 r/m			5*	5*	2	9
Register	01011 reg				5	5	2	9
Segment register	000 reg 111	(reg ≠ 01)			5	20	2	9,10,11
POPA = Pop All	01100001					19	2	9
XCHG = Exchange:								
Register/memory with register	1000011w	mod reg r/m			3,5*	3,5*	2,7	7,9
Register with accumulator	10010 reg				3	3		
IN = Input from:								
Fixed port	1110010w	port			5	5		14
Variable port	1110110w				5	5		14
OUT = Output to:								
Fixed port	1110011w	port			3	3		14
Variable port	1110111w				3	3		14
XLAT = Translate byte to AL	11010111				5	5		9
LEA = Load EA to register	10001101	mod reg r/m			3*	3*		
LDS = Load pointer to DS	11000101	mod reg r/m	(mod ≠ 11)		7*	21*	2	9,10,11
LES = Load pointer to ES	11000100	mod reg r/m	(mod ≠ 11)		7*	21*	2	9,10,11
LAHF = Load AH with flags	10011111				2	2		
SAHF = Store AH into flags	10011110				2	2		
PUSHF = Push flags	10011100				3	3	2	9
POPF = Pop flags	10011101				5	5	2,4	9,15

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTURCTION SET SUMMARY (Continued)

					CLOCK COUNT		COMMENTS	
FUNCTION	FORMAT				Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
ARITHMETIC								
ADD = Add:								
Reg/memory with register to either	000000dw	mod reg r/m			2,7*	2,7*	2	9
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	3,7*	3,7*	2	9
Immediate to accumulator	0000010w	data	data if w = 1		3	3		
ADC = Add with carry:								
Reg/memory with register to either	000100dw	mod reg r/m			2,7*	2,7*	2	9
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	3,7*	3,7*	2	9
Immediate to accumulator	0001010w	data	data if w = 1		3	3		
INC = Increment:								
Register/memory	1111111w	mod 000 r/m			2,7*	2,7*	2	9
Register	01000 reg				2	2		
SUB = Subtract:								
Reg/memory and register to either	001010dw	mod reg r/m			2,7	2,7*	2	9
Immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	3,7*	3,7*	2	9
Immediate from accumulator	0010110w	data	data if w = 1		3	3		
SBB = Subtract with borrow:								
Reg/memory and register to either	000110dw	mod reg r/m			2,7*	2,7*	2	9
Immediate from register/memory	100000sw	mod 011 r/m	data	data if sw=01	3,7*	3,7*	2	9
Immediate from accumulator	0001110w	data	data if w = 1		3	3		
DEC = Decrement:								
Register/memory	1111111w	mod 001 r/m			2,7*	2,7*	2	9
Register	01001 reg				2	2		
CMP = Compare:								
Register/memory with register	0011101w	mod reg r/m			2,6*	2,6*	2	9
Register with register/memory	0011100w	mod reg r/m			2,7*	2,7*	2	9
Immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	3,6*	3,6*	2	9
Immediate with accumulator	0011110w	data	data if w = 1		3	3		
NEG = Change sign	1111011w	mod 011 r/m			2	7*	2	7
AAA = ASCII adjust for add	00110111				3	3		
DAA = Decimal adjust for add	00100111				3	3		
AAS = ASCII adjust for subtract	00111111				3	3		
DAS = Decimal adjust for subtract	00101111				3	3		
MUL = Multiply (unsigned):	1111011w	mod 100 r/m						
Register-Byte					13	13		
Register-Word					21	21		
Memory-Byte					16*	16*	2	9
Memory-Word					24*	24*	2	9
IMUL = Integer multiply (signed):	1111011w	mod 101 r/m						
Register-Byte					13	13		
Register-Word					21	21		
Memory-Byte					16*	16*	2	9
Memory-Word					24*	24*	2	9

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTURCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
ARITHEMETIC (Continued)								
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s = 0	21,24*	21,24*	2	9
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 110 r/m						
Register-Byte					14	14	6	6
Register-Word					22	22	6	6
Memory-Byte					17*	17*	2,6	6,9
Memory-Word					25*	25*	2,6	6,9
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 111 r/m						
Register-Byte					17	17	6	6
Register-Word					25	25	6	6
Memory-Byte					20*	20*	2,6	6,9
Memory-Word					28*	28*	2,6	6,9
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			16	16		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			14	14		
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	2		
CWD = Convert word to double word	1 0 0 1 1 0 0 1				2	2		
LOGIC								
Shift/Rotate Instructions:								
Register/Memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2,7*	2,7*	2	9
Register/Memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n,8+n*	5+n,8+n*	2	9
Register/Memory by Count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n,8+n*	5+n,8+n*	2	9
	TTT	**Instruction**						
	0 0 0	ROL						
	0 0 1	ROR						
	0 1 0	RCL						
	0 1 1	RCR						
	1 0 0	SHL/SAL						
	1 0 1	SHR						
	1 1 1	SAR						
AND = **And:**								
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			2,7*	2,7*	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 100 r/m	data	data if w = 1	3,7*	3,7*	2	9
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1		3	3		
TEST = And function to flags, no result:								
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			2,6*	2,6*	2	9
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 000 r/m	data	data if w = 1	3,6*	3,6*	2	9
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1		3	3		
OR = **Or:**								
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			2,7*	2,7*	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 001 r/m	data	data if w = 1	3,7*	3,7*	2	9
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1		3	3		

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTRUCTION SET SUMMARY (Continued)

					CLOCK COUNT		COMMENTS	
FUNCTION	FORMAT				Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
LOGIC (Continued)								
XOR = Exclusive or:								
Reg/memory and register to either	001100dw	mod reg r/m			2,7*	2,7*	2	9
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w = 1	3,7*	3,7*	2	9
Immediate to accumulator	0011010w	data	data if w = 1		3	3		
NOT = Invert register/memory	1111011w	mod 010 r/m			2,7*	2,7*	2	9
STRING MANIPULATION:								
MOVS = Move byte/word	1010010w				5	5	2	9
CMPS = Compare byte/word	1010011w				8	8	2	9
SCAS = Scan byte/word	1010111w				7	7	2	9
LODS = Load byte/wd to AL/AX	1010110w				5	5	2	9
STOS = Stor byte/wd from AL/A	1010101w				3	3	2	9
INS = Input byte/wd from DX port	0110110w				5	5	2	9,14
OUTS = Output byte/wd to DX port	0110111w				5	5	2	9,14
Repeated by count in CX								
MOVS = Move string	11110011	1010010w			5+4n	5+4n	2	9
CMPS = Compare string	1111001z	1010011w			5+9n	5+9n	2,8	8,9
SCAS = Scan string	1111001z	1010111w			5+8n	5+8n	2,8	8,9
LODS = Load string	11110010	1010110w			5+4n	5+4n	2,8	8,9
STOS = Store string	11110010	1010101w			4+3n	4+3n	2,8	8,9
INS = Input string	11110011	0110110w			5+4n	5+4n	2	9,14
OUTS = Output string	11110011	0110111w			5+4n	5+4n	2	9,14
CONTROL TRANSFER								
CALL = Call:								
Direct within segment	11101000	disp-low	disp-high		7+m	7+m	2	18
Register/memory indirect within segment	11111111	mod 010 r/m			7+m, 11+m*	7+m, 11+m*	2,8	8,9,18
Direct intersegment	10011010	segment offset			13+m	26+m	2	11,12,18
		segment selector						
Protected Mode Only (Direct intersegment):								
Via call gate to same privilege level						41+m		8,11,12 18
Via call gate to different privilege level, no parameters						82+m		8,11,12 18
Via call gate to different privilege level, x parameters						86+4x +m		8,11,12 18
Via TSS						177+m		8,11,12 18
Via task gate						182+m		8,11,12 18
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		16+m	29+m*	2	8,9,11 12,18

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTRUCTION SET SUMMARY (Continued)

		CLOCK COUNT		COMMENTS	
FUNCTION	FORMAT	Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
CONTROL TRANSFER (Continued)					
Protected Mode Only (Indirect intersegment):					
Via call gate to same privilege level			44+m*		8,9,11 12,18
Via call gate to different privilege level, no parameters			83+m*		8,9,11 12,18
Via call gate to different privilege level, x parameters			90+4x +m*		8,9,11 12,18
Via TSS			180+m*		8,9,11 12,18
Via task gate			185+m*		8,9,11 12,18
JMP = Unconditional jump:					
Short/long	11101011 disp-low	7+m	7+m		18
Direct within segment	11101001 disp-low disp-high	7+m	7+m		18
Register/memory indirect within segment	11111111 mod 100 r/m	7+m, 11+m*	7+m, 11+m*	2	9,18
Direct intersegment	11101010 segment offset segment selector	11+m	23+m		11,12,18
Protected Mode Only (Direct intersegment):					
Via call gate to same privilege level			38+m		8,11,12 18
Via TSS			175+m		8,11,12 18
Via task gate			180+m		8,11,12 18
Indirect intersegment	11111111 mod 101 r/m (mod ≠ 11)	15+m*	26+m*	2	8,9,11 12,18
Protected Mode Only (Indirect Intersegment):					
Via call gate to same privilege level			41+m*		8,9, 11 12,18
Via TSS			178+m*		8,9,11 12,18
Via task gate			183+m*		8,9,11 12,18
RET = Return from CALL:					
Within segment	11000011	11+m	11+m	2	8,9,18
Within seg adding immed to SP	11000010 data-low data-high	11+m	11+m	2	8,9,18
Intersegment	11001011	15+m	25+m	2	8,9,11 12,18
Intersegment adding immediate to SP	11001010 data-low data-high	15+m		2	8,9,11 12,18
Protected Mode Only (RET):					
To different privilege level			55+m		9,11,12 18

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTURCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
CONTROL TRANSFER (Continued)								
JE/JZ = Jump on equal/zero	01110100	disp			7+m or 3	7+m or 3		18
JL/JNGE = Jump on less/not greater or equal	01111100	disp			7+m or 3	7+m or 3		18
JLE/JNG = Jump on less or equal/ not greater	01111110	disp			7+m or 3	7+m or 3		18
JB/JNAE = Jump on below/not above or equal	01110010	disp			7+m or 3	7+m or 3		18
JBE/JNA = Jump on below or equal/not above	01110110	disp			7+m or 3	7+m or 3		18
JP/JPE = Jump on parity/parity even	01111010	disp			7+m or 3	7+m or 3		18
JO = Jump on overflow	01110000	disp			7+m or 3	7+m or 3		18
JS = Jump on sign	01111000	disp			7+m or 3	7+m or 3		18
JNE/JNZ = Jump on not equal/not zero	01110101	disp			7+m or 3	7+m or 3		18
JNL/JGE = Jump on not less/ greater or euqal	01111101	disp			7+m or 3	7+m or 3		18
JNLE/JG = Jump on not less or equal/greater	01111111	disp			7+m or 3	7+m or 3		18
JNB/JAE = Jump on not below/ above or equal	01110011	disp			7+m or 3	7+m or 3		18
JNBE/JA = Jump on not below or equal/above	01110111	disp			7+m or 3	7+m or 3		18
JNP/JPO = Jump on not par/par odd	01111011	disp			7+m or 3	7+m or 3		18
JNO = Jump on not overflow	01110001	disp			7+m or 3	7+m or 3		18
JNS = Jump on not sign	01111001	disp			7+m or 3	7+m or 3		18
LOOP = Loop CX times	11100010	disp			8+m or 4	8+m or 4		18
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			8+m or 4	8+m or 4		18
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			8+m or 4	8+m or 4		18
JCXZ = Jump on CX zero	11100011	disp			8+m or 4	8+m or 4		18
ENTER = Enter Procedure	11001000	data-low	data-high	L			2,8	8,9
L = 0					11	11	2,8	8,9
L = 1					15	15	2,8	8,9
L > 1					16+4x (L-1)	16+4x (L-1)	2,8	8,9
LEAVE = Leave Procedure	11001001				5	5		
INT = Interrupt:								
Type specified	11001101	type			23+m		2,7,8	
Type 3	11001100				23+m		2,7,8	
INTO = Interrupt on overflow	11001110				24+m or 3 (3 if no interrupt)	(3 if no interrupt)	2,6,8	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
CONTROL TRANSFER (Continued)					
Protected Mode Only:					
Via interrupt or trap gate to same privilege level			40+m		7,8,11 12,18
Via interrupt or trap gate to fit different privilege level			78+m		7,8,11 12,18
Via Task Gate			167+m		7,8,11 12,18
IRET = Interrupt return	1 1 0 0 1 1 1 1	17+m	31+m	2,4	8,9,11 12,15,18
Protected Mode Only:					
To different privilege level			55+m		8,9,11 12,15,18
To different task (NT = 1)			169+m		8,9,11 12,18
SOUND = Detect value out of range	0 1 1 0 0 0 1 0 · mod reg r/m	13*	13* (Use INT clock count if exception 5)	2,6	6,8,9,11 12,18
PROCESSOR CONTROL					
CLC = Clear carry	1 1 1 1 1 0 0 0	2	2		
CMC = Complement carry	1 1 1 1 0 1 0 1	2	2		
STC = Set carry	1 1 1 1 1 0 0 1	2	2		
CLD = Clear direction	1 1 1 1 1 1 0 0	2	2		
STD = Set direction	1 1 1 1 1 1 0 1	2	2		
CLI = Clear interrupt	1 1 1 1 1 0 1 0	3	3		14
STI = Set interrupt	1 1 1 1 1 0 1 1	2	2		14
HLT = Halt	1 1 1 1 0 1 0 0	2	2		13
WAIT = Wait	1 0 0 1 1 0 1 1	3	3		
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	0	0		14
CTS = Clear task switched flag	0 0 0 0 1 1 1 1 · 0 0 0 0 0 1 1 0	2	2	3	13
ESC = Processor Extension Escape	1 1 0 1 1 T T T · mod LLL r/m (TTT LLL are opcode to processor extension)	9-20*	9-20*	5,8	8,17
SEG = Segment Override Prefix	0 0 1 reg 1 1 0	0	0		
PROTECTION CONTROL					
LGDT = Load global descriptor table register	0 0 0 0 1 1 1 1 · 0 0 0 0 0 0 0 1 · mod 010 r/m	11*	11*	2,3	9,13
SGDT = Store global descriptor table register	0 0 0 0 1 1 1 1 · 0 0 0 0 0 0 0 1 · mod 000 r/m	11*	11*	2,3	9
LIDT = Load interrupt descriptor table register	0 0 0 0 1 1 1 1 · 0 0 0 0 0 0 0 1 · mod 011 r/m	12*	12*	2,3	9,13
SIDT = Store interrupt descriptor table register	0 0 0 0 1 1 1 1 · 0 0 0 0 0 0 0 1 · mod 001 r/m	12*	12*	2,3	9
LLDT = Load local descriptor table register from register memory	0 0 0 0 1 1 1 1 · 0 0 0 0 0 0 0 0 · mod 010 r/m		17,19*	1	9,11,13

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

MBL 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT			CLOCK COUNT		COMMENTS	
				Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
PROTECTION CONTROL (Continued)							
SLDT = Store local descriptor table register to register/ memory	00001111	00000000	mod 000 r/m		2,3*	1	9
LTR = Load task register from register/memory	00001111	00000000	mod 011 r/m		17,19*	1	9,11,13
STR = Store task register to register memory	00001111	00000000	mod 001 r/m		2,3*	1	9
LMSW = Load machine status word from register/memory	00001111	00000001	mod 110 r/m	3,6*	3,6*	2,3	9,13
SMSW = Store machine status word	00001111	00000001	mod 100 r/m	2,3*	2,3*	2,3	9
LAR = Load access rights from register/memory	00001111	00000010	mod reg r/m		14,16*	1	9,11,16
LSL = Load segment limit from register/memory	00001111	00000011	mod reg r/m		14,16*	1	9,11,16
ARPL = Adjust register privilege level from register/memory		01100011	mod reg r/m		10*,11*	2	8,9
VERR = Verify read access: register/memory	00001111	00000000	mod 100 r/m		14,16*	1	9,11,16
VERR = Verify write access:	00001111	00000000	mod 101 r/m		14,16*	1	9,11,16

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

Footnotes

The effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 00 then DISP = 0*, disp-low and disp-high are absent
are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

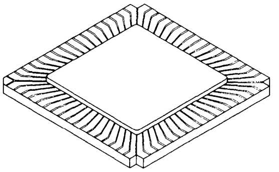
REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

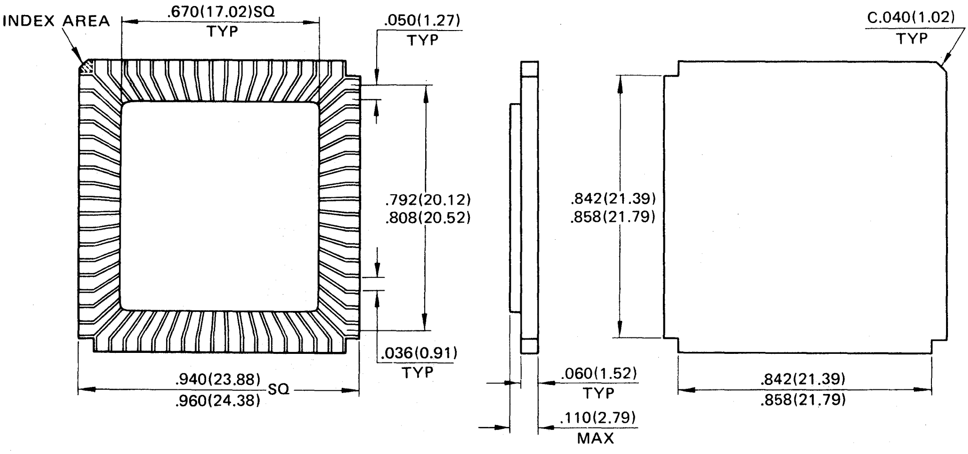
PACKAGE ILLUSTRATION

CERAMIC LCC
(METAL SEAL)



PACKAGE DIMENSIONS (Suffix: -CV)

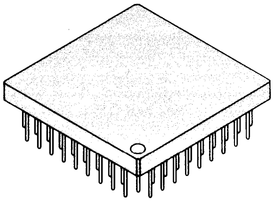
68-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-68C-A01)



Dimension in
inches (millimeters)

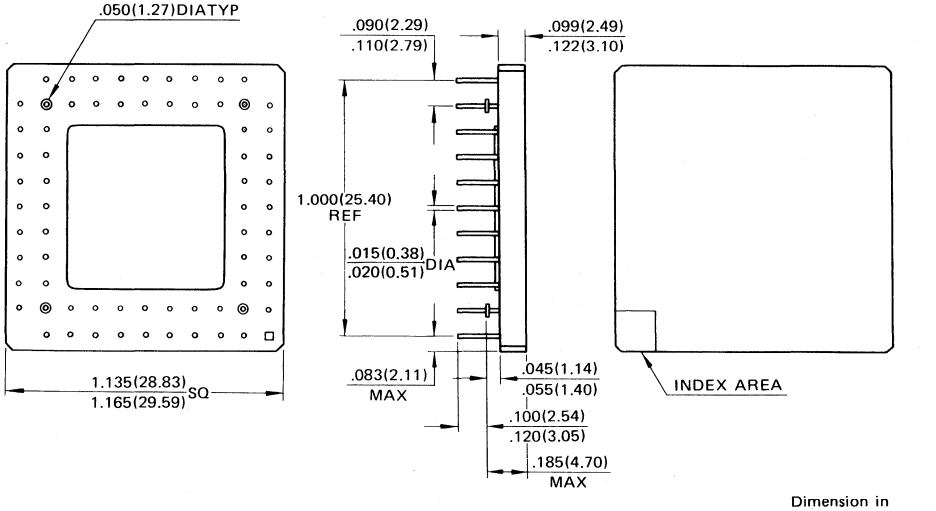
PACKAGE ILLUSTRATION

CERAMIC PGA
(METAL SEAL)



PACKAGE DIMENSIONS (Suffix: -CR)

68-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY
(CASE No.: PGA-68C-A01)



Dimension in
inches(millimeters)

FUJITSU

BIPOLAR CLOCK GENERATOR AND READY INTERFACE FOR MBL 80286 PROCESSORS

MBL 82284-8
MBL 82284-6

December 1985
Edition 1.0

BIPOLAR CLOCK GENERATOR AND READY INTERFACE FOR MBL 80286 PROCESSORS

The Fujitsu MBL 82284 is a clock generator/driver which provides clock signals for MBL 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

- **Generates System Clock for MBL 80286 Processors**
- **Uses Crystal or TTL Signal for Frequency Source**
- **Provides Local READY and Multibus* READY Synchronization**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Single +5V Power Supply**
- **Two Package Options:**
  - **18-pin Cerdip (Suffix: CZ)**
  - **18-pin Plastic DIP (Suffix: P)**

Fig. 1 – BLOCK DIAGRAM

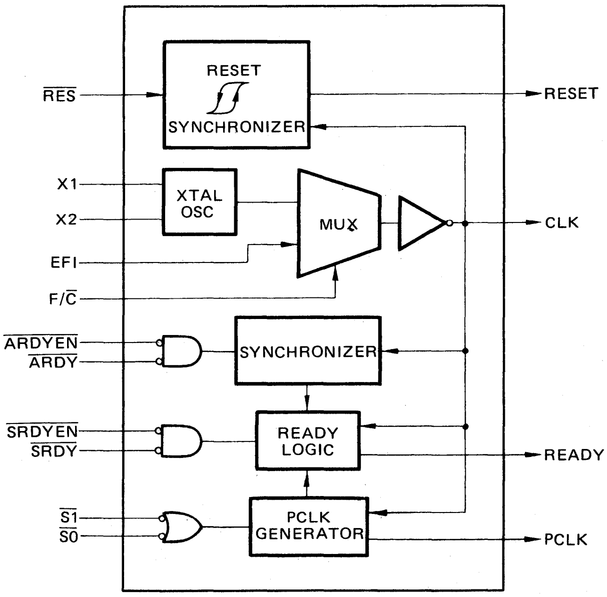
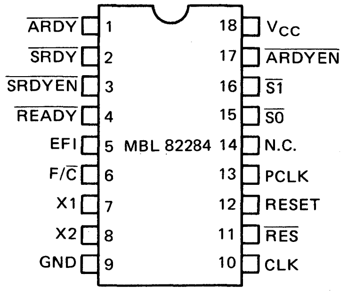


Fig. 2 – PIN CONFIGURATION


$\overline{\text{ARDY}}$ 1
$\overline{\text{SRDY}}$ 2
$\overline{\text{SRDYEN}}$ 3
$\overline{\text{READY}}$ 4
EFI 5
F/$\overline{\text{C}}$ 6
X1 7
X2 8
GND 9
MBL 82284
18 V_{CC}
17 $\overline{\text{ARDYEN}}$
16 $\overline{\text{S1}}$
15 $\overline{\text{S0}}$
14 N.C.
13 PCLK
12 RESET
11 $\overline{\text{RES}}$
10 CLK

* Multibus is a patented bus of Intel.

PIN DESCRIPTION

The following pin function descriptions are for the MBL 82284 clock generator.

Table 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
CLK	O	**System Clock** is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
F/$\overline{\text{C}}$	I	**Frequency/Crystal Select** is a strapping option to select the source for the CLK output. When F/$\overline{\text{C}}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{\text{C}}$ is strapped HIGH, the EFI input drives the CLK output.
X1, X2	I	**Crystall In** are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{\text{C}}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	I	**External Frequency In** drives CLK when the F/$\overline{\text{C}}$ input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	O	**Peripheral Clock** is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{\text{ARDYEN}}$	I	**Asynchronous Ready Enable** is an active LOW input which qualifies the $\overline{\text{ARDY}}$ input. $\overline{\text{ARDYEN}}$ selects $\overline{\text{ARDY}}$ as the source of ready for the current bus cycle. Inputs to $\overline{\text{ARDYEN}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{\text{ARDY}}$	I	**Asynchronous Ready** is an active LOW input used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Inputs to $\overline{\text{ARDY}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{\text{SRDYEN}}$	I	**Synchronous Ready Enable** is an active LOW input which qualifies $\overline{\text{SRDY}}$. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{\text{SRDY}}$	I	**Synchronous Ready** is an active LOW input used to terminate the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{\text{READY}}$	O	**Ready** is an active LOW output which signals the current bus cycle is to be completed. The $\overline{\text{SRDY}}$, $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ and RES inputs control $\overline{\text{READY}}$ as explained later in the $\overline{\text{READY}}$ generator section. $\overline{\text{READY}}$ is an open collector output requiring an external 910Ω pullup resistor.
$\overline{\text{S0}}$, $\overline{\text{S1}}$	I	**Status** inputs prepare the MBL 82284 for a subsequent bus cycle. $\overline{\text{S0}}$ and $\overline{\text{S1}}$ synchronize PCLK to the internal processor clock and control $\overline{\text{READY}}$. These inputs have pullup resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
RESET	O	**Reset** is an active HIGH output which is derived from the $\overline{\text{RES}}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{\text{READY}}$ will be active (LOW).
$\overline{\text{RES}}$	I	**Reset In** is an active LOW input which generates the system reset signal RESET. Signals to $\overline{\text{RES}}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{\text{RES}}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V_{CC}		**System Power:** +5V power supply.
GND		**System Ground:** 0 volts.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MBL 82284 generates the clock, ready, and reset signals required for MBL 80286 processors and support components. The MBL 82284 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic and system reset generation logic.

CLOCK GENERATOR

The CLK output provides the basic timing control for an MBL 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The MBL 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

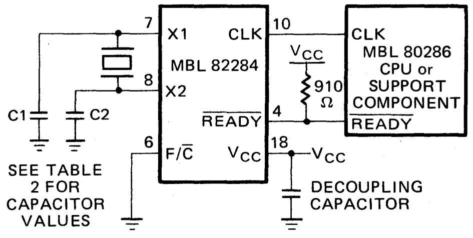
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

OSCILLATOR

The oscillator circuit of the MBL 82284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 2. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pins. Decouple V_{CC} and GND as close to the MBL 82284 as possible.

Fig. 3 – RECOMMENDED CRYSTAL AND $\overline{\text{READY}}$ CONNECTIONS

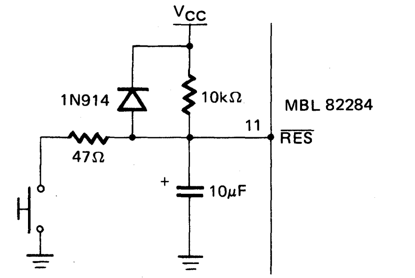


RESET OPERATION

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{\text{RES}}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{\text{RES}}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{\text{RES}}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable V_{CC} and CLK. To prevent spurious activity, $\overline{\text{RES}}$ should be asserted until V_{CC} and CLK stabilize at their operating values. MBL 80286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Fig. 4, will keep $\overline{\text{RES}}$ LOW long enough to satisfy both needs.

Fig. 4 – TYPICAL RC $\overline{\text{RES}}$ TIMING CIRCUIT



A Schmitt trigger input with hysteresis on $\overline{\text{RES}}$ assures a single transition of RESET with an RC circuit on $\overline{\text{RES}}$. The hysteresis separates the input voltage level at which the circuit output switches between HIGH to LOW from the input voltage level at which the circuit output switches between LOW to HIGH. The $\overline{\text{RES}}$ HIGH to LOW input transition voltage is lower than the $\overline{\text{RES}}$ LOW to HIGH input transition voltage. As long as the slope of the $\overline{\text{RES}}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{\text{RES}}$ input transition voltage, the RESET output will make a single transition.

READY OPERATION

The MBL 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{\text{SRDY}}$) or asynchronous ready ($\overline{\text{ARDY}}$) source may be used. Each ready input has an enable ($\overline{\text{SRDYEN}}$ and $\overline{\text{ARDYEN}}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{\text{READY}}$ is enabled (LOW), if either $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ = 0 or $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ = 0 when sampled by the MBL 82284 $\overline{\text{READY}}$ generation logic. $\overline{\text{READY}}$ will remain active for at least two CLK cycles.

The $\overline{\text{READY}}$ output has an open-collector driver allowing other ready circuits to be wire or'ed with it, as shown in Fig. 3. The $\overline{\text{READY}}$ signal of an MBL 80286 system requires an external 910 Ω ±5% pull-up resistor. To force the $\overline{\text{READY}}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{\text{READY}}$ output floats when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{\text{READY}}$ signal to V_{IH}. When RESET is active, $\overline{\text{READY}}$ is forced active one CLK later (see waveforms).

Fig. 5 illustrates the operation of $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$. These inputs are sampled on the falling edge of CLK when $\overline{\text{S1}}$ and $\overline{\text{S0}}$ are inactive and PCLK is HIGH. $\overline{\text{READY}}$ is forced active when both $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$ are sampled as LOW.

Fig. 6 shows the operation of $\overline{\text{ARDY}}$ and $\overline{\text{ARDYEN}}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{\text{ARDY}}$ and $\overline{\text{ARDYEN}}$ have been resolved as active, the $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$ inputs are ignored. Either $\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ must be HIGH at end of TS (see Fig. 6).

$\overline{\text{READY}}$ remains active until either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ are sampled LOW, or the ready inputs are sampled as inactive.

Table 2 – MBL 82284 CRYSTAL LOADING CAPACITANCE VALUES

Crystal Frequency	C1 Capacitance (pin 7)	C2 Capacitance (pin 8)
1 to 8 MHz 8 to 16 MHz	60 pF 25 pF	40 pF 15 pF

NOTE: Capacitance values must include stray board capacitance.

Fig. 5 – SYNCHRONOUS READY OPERATION

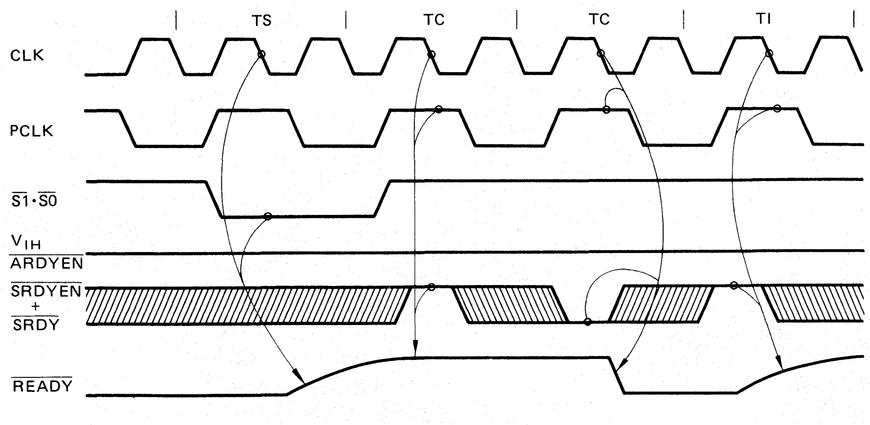
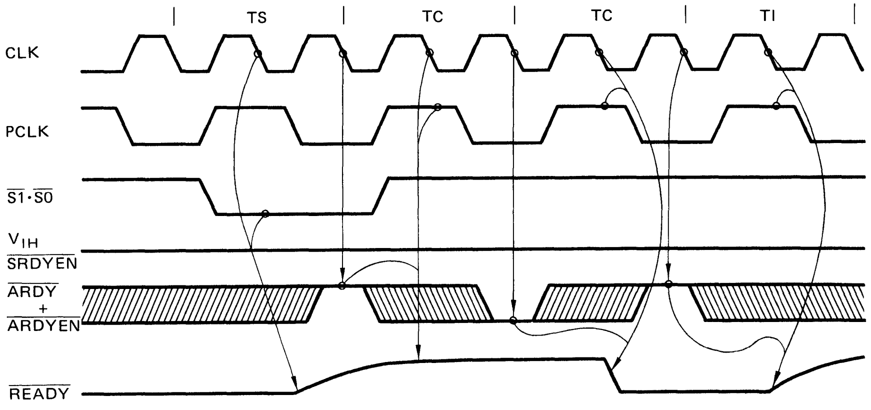

TS
TC
TC
TI
CLK
PCLK
$\overline{\text{S1}}\cdot\overline{\text{S0}}$
V_{IH}
$\overline{\text{ARDYEN}}$
$\overline{\text{SRDYEN}}$ + $\overline{\text{SRDY}}$
$\overline{\text{READY}}$

Fig. 6 – ASYNCHRONOUS READY OPERATION



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . –65°C to +150°C
All Output and Supply Voltages . . . . –0.5V to +7V
All Input Voltages . . . . –1.0V to +5.5V
Power Dissipation . . . . 1 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V±5%, T_A = 0°C to 70°C)

Symbol	Parameter	MBL 82284-6 (6 MHz)		MBL 82284-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
V_{IL}	Input LOW Voltage		0.8		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		2.0		V	
V_{IHR}	$\overline{RES}$ and EFI Input HIGH Voltage	2.6		2.6		V	
V_{HYS}	$\overline{RES}$ Input Hysteresis	0.25		0.25		V	
V_{OL}	RESET, PCLK Output LOW Voltage		0.45		0.45	V	I_{OL} = 5mA
V_{OH}	RESET, PCLK Output HIGH Voltage	2.4		2.4		V	I_{OH} = –1mA
V_{OLR}	$\overline{READY}$ Output LOW Voltage		0.45		0.45	V	I_{OL} = 7mA
V_{OLC}	CLK Output LOW Voltage		0.45		0.45	V	I_{OL} = 5mA
V_{OHC}	CLK Output HIGH Voltage	4.0		4.0		V	I_{OH} = –800μA
V_C	Input Forward Clamp Voltage		–1.0		–1.0	V	I_C = –5mA
I_F	Forward Input Current		–0.5		–0.5	mA	V_F = 0.45V
I_R	Reverse Input Current		50		50	μA	V_R = V_{CC}
I_{CC}	Power Supply Current		145		145	mA	
C_I	Input Capacitance		10		10	pF	F_C = 1MHz

A.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to 70°C)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

Symbol	Parameter	MBL 82284-6 (6 MHz)		MBL 82284-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
1	EFI to CLK Delay		35		30	ns	at 1.5V Note 1
2	EFI LOW Time	40		25		ns	at 1.5V Note 1, Note 7
3	EFI HIGH Time	35		25		ns	at 1.5V Note 1, Note 7
4	CLK Period	83	500	62	500	ns	
5	CLK LOW Time	20		15		ns	at 1.0V Note 1, Note 2, 8
6	CLK HIGH Time	25		25		ns	at 3.6V Note 1, Note 2, 8
7	CLK Rise Time		10		10	ns	1.0V to 3.6V Note 1
8	CLK Fall Time		10		10	ns	3.6V to 1.0V Note 1
9	Status Setup Time	28		22		ns	Note 1
10	Status Hold Time	1		1		ns	Note 1
11	$\overline{\text{SRDY}}$ or $\overline{\text{SRDYEN}}$ Setup Time	25		15		ns	Note 1
12	$\overline{\text{SRDY}}$ or $\overline{\text{SRDYEN}}$ Hold Time	0		0		ns	Note 1
13	$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ Setup Time	5		0		ns	Note 1, Note 3
14	$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ Hold Time	30		30		ns	Note 1, Note 3
15	$\overline{\text{RES}}$ Setup Time	25		20		ns	Note 1, Note 3
16	$\overline{\text{RES}}$ Hold Time	10		10		ns	Note 1, Note 3
17	$\overline{\text{READY}}$ Inactive Delay	5		5		ns	at 0.8V Note 4
18	$\overline{\text{READY}}$ Active Delay	0	33	0	24	ns	at 0.8V Note 4
19	PCLK Delay	0	45	0	45	ns	Note 5
20	RESET Delay	5	50	5	34	ns	Note 5
21	PCLK LOW Time	t4-20		t4-20		ns	Note 5, Note 6
22	PCLK HIGH Time	t4-20		t4-20		ns	Note 5, Note 6

NOTE 1: CLK loading: C_L = 150pF.

NOTE 2: With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t2, and t3. Use a parallel-resonant, fundamental mode crystal. The recommended crystal loaidng for CLK frequencies of 8–16MHz are 25pF from pin X1 to ground, and 15pF from pin X2 to ground. These recommended values are ±5pF and include all stray capacitance, Decouple V_{CC} and GND as close to the MBL 82284 as possible.

NOTE 3: This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

NOTE 4: $\overline{\text{READY}}$ loading: I_{OL} = 7mA, C_L = 150pF. In system application, use 910 Ω ±5% pullup resistor to meet MBL 80286-8 and 80286-6 timing requirements.

NOTE 5: PCLK and RESET loading: C_L = 75pF. PCLK also has 750 Ω pullup.

NOTE 6: t4 refers to any allowable CLK period.

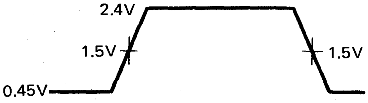
NOTE 7: When driving the MBL 82284 with EFI, provide minimum EFI HIGH and LOW times as follows:

CLK Output Frequency:	8MHz CLK	12MHz CLK	16MHz CLK*
Min. required EFI HIGH time	52ns	35ns	25ns
Min. required EFI LOW time	52ns	40ns	25ns

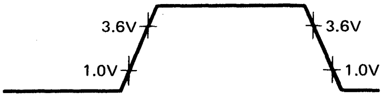
*At CLK frequencies above 12MHz, CLK output HIGH and LOW times are guaranteed only when using crystal with recommended capacitive loading per Table 2, *not* when driving component from EFI. All features of the MBL 82284 remain functional whether EFI or crystal is used to drive the MBL 82284.

NOTE 8: When using crystal (with recommended capacitive loading per Table 2) appropriate for speed of MBL 80286, CLK output HIGH and LOW times guaranteed to meet MBL 80286 requirements.

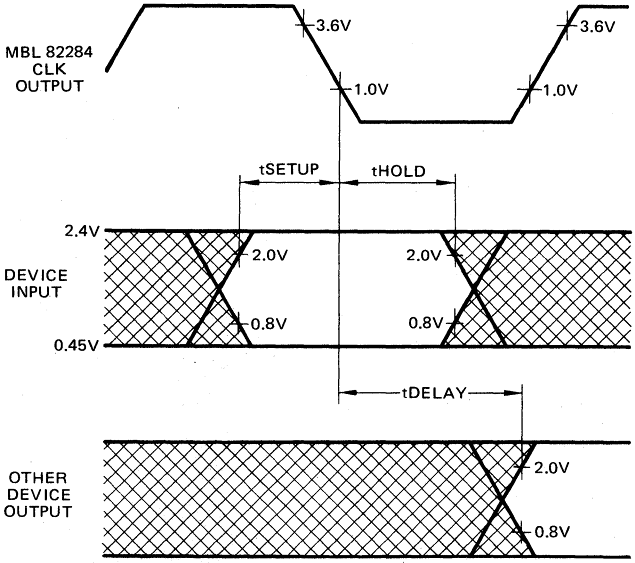
NOTE 9: EFI Drive and Measurement Points



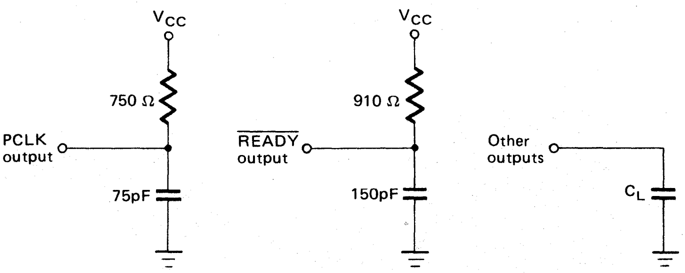
NOTE 10: CLK Output Measurement Points



NOTE 11: AC Setup, Hold and Delay Time Measurement — General

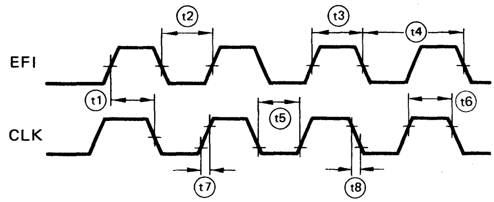


NOTE 12: AC Test Loading on Outputs



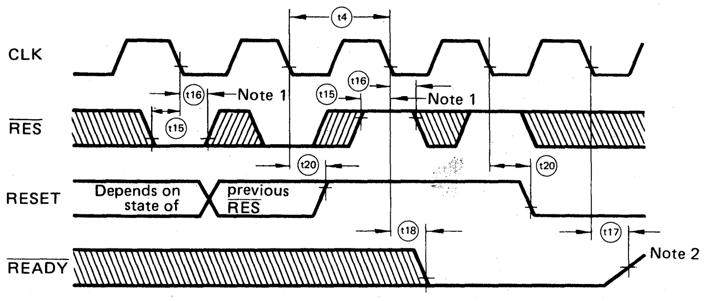
WAVEFORMS

CLK AS A FUNCTION OF EFI



NOTE: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

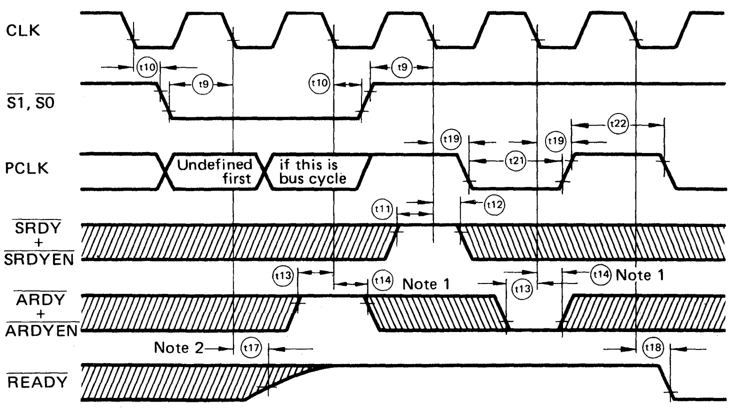
RESET AND $\overline{\text{READY}}$ TIMING AS A FUNCTION OF $\overline{\text{RES}}$ WITH $\overline{\text{S1}}$ AND $\overline{\text{S0}}$ HIGH



NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

NOTE 2: Tie 910 Ω ±5% pullup resistor to the $\overline{\text{READY}}$ output.

READY AND PCLK TIMING WITH RES HIGH

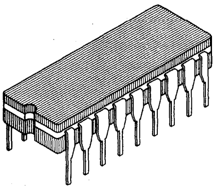


NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

NOTE 2: Tie 910 Ω ±5% pullup resistor to the READY output.

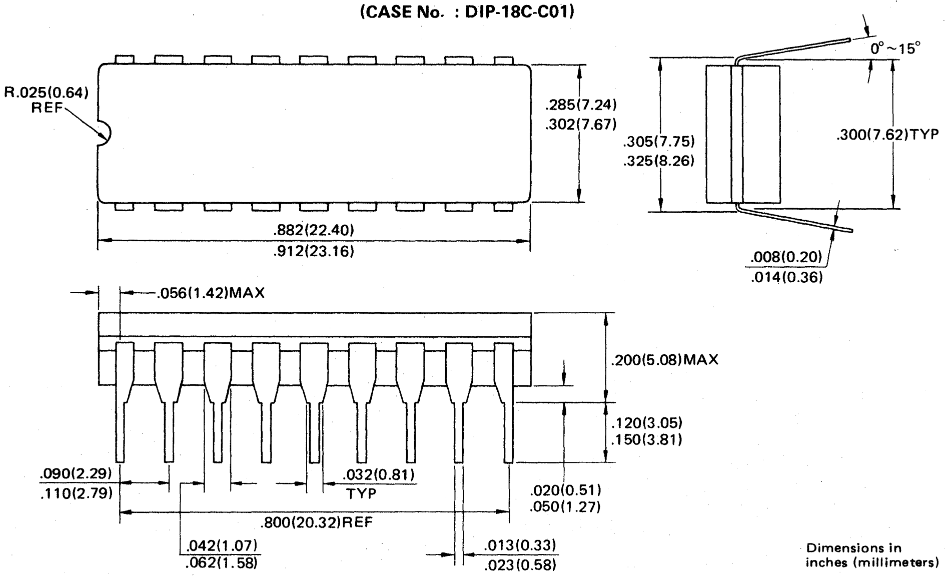
PACKAGE ILLUSTRATION

CERAMIC PACKAGE
(CERDIP)



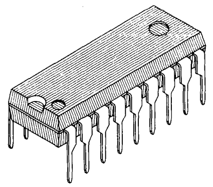
PACKAGE DIMENSIONS (Suffix: CZ)

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



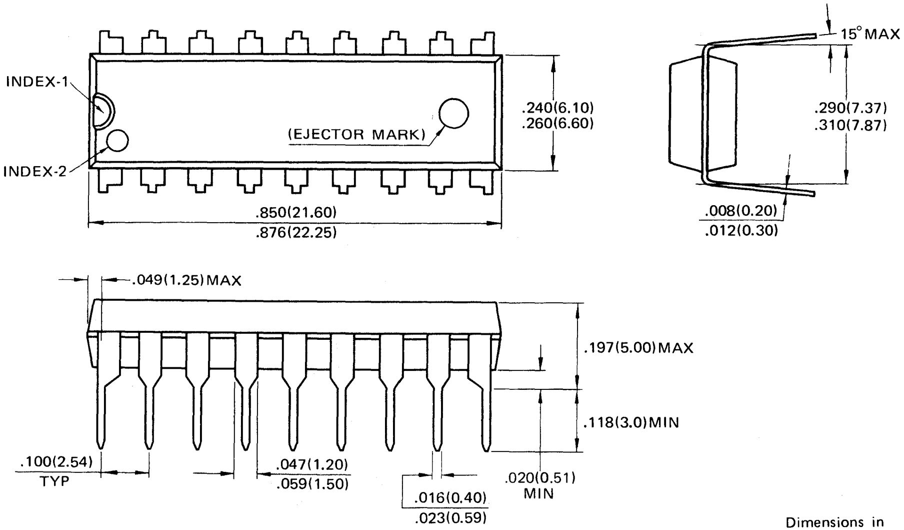
PACKAGE ILLUSTRATION

PLASTIC PACKAGE



PACKAGE DIMENSIONS (Suffix: P)

18-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



Dimensions in
inches (millimeters)

FUJITSU

NMOS BUS CONTROLLER FOR MBL 80286 PROCESSORS

MBL 82288-8
MBL 82288-6

December 1985
Edition 1.0

NMOS BUS CONTROLLER FOR MBL 80286 PROCESSORS

The Fujitsu MBL 82288 Bus Controller is a 20-pin NMOS component for use in MBL 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

Two modes of operation are possible via a strapping option: Multibus compatible bus cycles, and high speed bus cycles.

- **Provides Commands and Control for Local and System Bus**
- **Offers Wide Flexibility in System Configurations**
- **Flexible Command Timing**
- **Optional Multibus* Compatible Timing**
- **Control Drivers with 16 mA I_{OL} and 3-State Command Drivers with 32 mA I_{OL}**
- **Single +5V Supply**
- **Two Package Options:**
  –20-Pin Cerdip (Suffix: -CZ)
  –20-Pin Plastic DIP (Suffix: -P)

Fig. 1 – BLOCK DIAGRAM

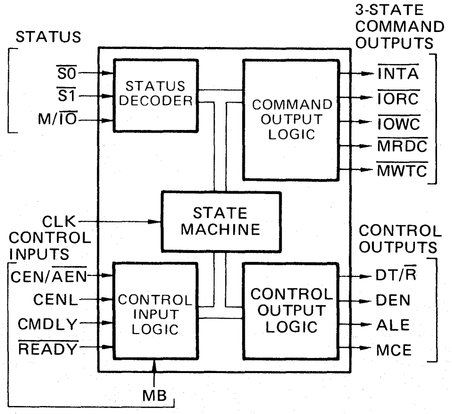
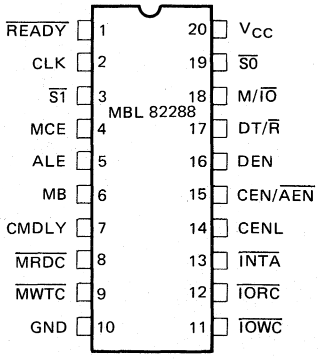


Fig. 2 – PIN CONFIGURATION



*Multibus is a patented bus of Intel.

PIN DESCRIPTION

The following pin function descriptions are for the MBL 82288 bus controller.

Table 1 – PIN DESCRIPTION

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>CLK</td><td>I</td><td><b>System Clock</b> provides the basic timing control for the MBL 82288 in an MBL 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.</td></tr>
<tr><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$</td><td>I</td><td><b>Bus Cycle Status</b> starts a bus cycle and, along with M/$\overline{\text{IO}}$, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ is sampled LOW at the falling edge of CLK. Setup and hold times must be met for proper operation.
<table>
<tr><th colspan="4">MBL 80286 Bus Cycle Status Definition</th></tr>
<tr><th>M/$\overline{\text{IO}}$</th><th>$\overline{\text{S1}}$</th><th>$\overline{\text{S0}}$</th><th>Type of Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; Idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; Idle</td></tr>
</table></td></tr>
<tr><td>M/$\overline{\text{IO}}$</td><td>I</td><td><b>Memory or I/O Select</b> determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>MB</td><td>I</td><td><b>Multibus Mode Select</b> determines timing of the command and control outputs. When HIGH, the bus controller operates with Multibus-compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{\text{AEN}}$ input pin is selected by this signal. This input is typically a strapping option and not dynamically changed.</td></tr>
<tr><td>CENL</td><td>I</td><td><b>Command Enable Latched</b> is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the end of each TS cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this MBL 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>CMDLY</td><td>I</td><td><b>Command Delay</b> allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If $\overline{\text{READY}}$ is detected LOW before the command output is activated, the MBL 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command. This input has no effect on MBL 82288 control outputs.</td></tr>
<tr><td>$\overline{\text{READY}}$</td><td>I</td><td><b>Ready</b> indicates the end of the current bus cycle. $\overline{\text{READY}}$ is an active LOW input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{\text{READY}}$ must be LOW during reset, to force the MBL 82288 into the idle state. Setup and hold times must be met for proper operation. The MBL 82284 drives $\overline{\text{READY}}$ LOW during RESET.</td></tr>
</table>

Table 1 – PIN DESCRIPTION (Continued)

Symbol	Type	Name and Function
CEN/$\overline{\text{AEN}}$	I	**Command Enable/Address Enable** controls the command and DEN outputs of the bus controller. CEN/$\overline{\text{AEN}}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is HIGH, this pin has the $\overline{\text{AEN}}$ function. $\overline{\text{AEN}}$ is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). $\overline{\text{AEN}}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). $\overline{\text{AEN}}$ would normally be controlled by an 82289 bus arbiter which activates $\overline{\text{AEN}}$ when that arbiter owns the bus to which the bus controller is attached. When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not tristate them.
ALE	O	**Address Latch Enable** controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	**Master Cascade Enable** signals that a cascade address from a master MBL 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	**Data Enable** controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{\text{R}}$	O	**Data Transmit/Receive** establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/$\overline{\text{R}}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{\text{R}}$ is not affected by any of the control inputs.
$\overline{\text{IOWC}}$	O	**I/O Write Command** instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IORC}}$	O	**I/O Read Command** instructs an I/O device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{MWTC}}$	O	**Memory Write Command** instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{MRDC}}$	O	**Memory Read Command** instructs the memory device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{INTA}}$	O	**Interrupt Acknowledge** tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
V_{CC}		**System Power:** +5V power supply.
GND		**System Ground:** 0 volts.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MBL 82288 bus controller is used in MBL 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to satisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a $\overline{\text{CMDLY}}$ input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.

Connection to multiple buses are supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the MBL 80286 local bus.

Bus shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the 82289.

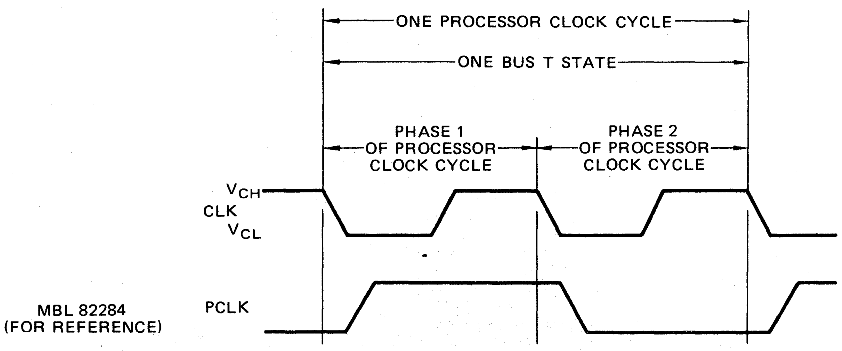
Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for tristate bus drivers to enter 3-state OFF before enabling other drivers onto the same bus.

The term CPU refers to any MBL 80286 processor or MBL 80286 support component which may become an MBL 80286 local bus master and thereby drive the MBL 82288 status inputs.

PROCESSOR CYCLE DEFINITION

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see Fig. 3). Knowledge of the phase of the local bus master internal clock is required for proper operation of the MBL 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted beginning in Phase 1 of the local bus master's internal clock.

Fig. 3 — CLK RELATIONSHIP TO THE PROCESSOR CLOCK AND BUS T-STATES

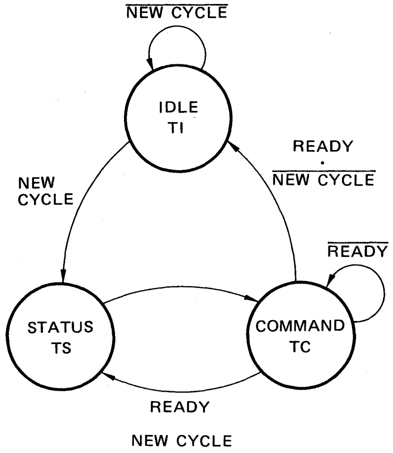

ONE PROCESSOR CLOCK CYCLE
ONE BUS T STATE
PHASE 1 OF PROCESSOR CLOCK CYCLE
PHASE 2 OF PROCESSOR CLOCK CYCLE
V_{CH}
CLK
V_{CL}
MBL 82284 (FOR REFERENCE)
PCLK

BUS STATE DEFINITION

The MBL 82288 bus controller has three bus states (see Fig. 4): Idle (TI), Status (TS) and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The TI bus state occurs when no bus cycle is currently active on the MBL 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.

Fig. 4 – MBL 82288 BUS STATES



BUS CYCLE DEFINITION

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes LOW, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ are active (see Fig. 5). These inputs are sampled by the MBL 82288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The $\overline{\text{READY}}$ input determines whether the current TC bus state is to be repeated. The $\overline{\text{READY}}$ input has the same timing and effect for all bus cycles. $\overline{\text{READY}}$ is sampled at the end of each TC bus state to see if it is active. If sampled HIGH, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.

When $\overline{\text{READY}}$ is sampled LOW, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

Fig. 5 – BUS CYCLE DEFINITION

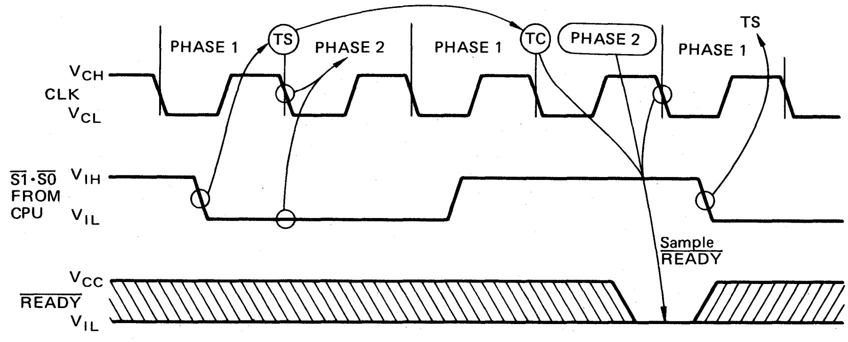


Table 2 – COMMAND AND CONTROL OUTPUTS FOR EACH TYPE OF BUS CYCLE

Type of Bus Cycle	M/$\overline{\text{IO}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$	Command Activated	DT/$\overline{\text{R}}$ State	ALE, DEN Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	$\overline{\text{INTA}}$	LOW	YES	YES
I/O Read	0	0	1	$\overline{\text{IORC}}$	LOW	YES	NO
I/O Write	0	1	0	$\overline{\text{IOWC}}$	HIGH	YES	NO
None; Idle	0	1	1	None	HIGH	NO	NO
Halt/Shutdown	1	0	0	None	HIGH	NO	NO
Memory Read	1	0	1	$\overline{\text{MRDC}}$	LOW	YES	NO
Memory Write	1	1	0	$\overline{\text{MWTC}}$	HIGH	YES	NO
None; Idle	1	1	1	None	HIGH	NO	NO

OPERATING MODES

Two types of buses are supported by the MBL 82288: Multibus and non-Multibus. When the MB input is strapped HIGH, Multibus timing is used. In Multibus mode, the MBL 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

COMMAND AND CONTROL OUTPUTS

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{\text{IO}}$, $\overline{\text{S1}}$, and $\overline{\text{S0}}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decode done by the MBL 82288 and the effect on command, DT/$\overline{\text{R}}$, ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{\text{MRDC}}$, $\overline{\text{IORC}}$, and $\overline{\text{INTA}}$), control outputs (ALE, DEN, DT/$\overline{\text{R}}$) and control inputs (CEN/$\overline{\text{AEN}}$, CENL, CMDLY, MB, and $\overline{\text{READY}}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{\text{MWTC}}$ and $\overline{\text{IOWC}}$), control outputs (ALE, DEN, DT/$\overline{\text{R}}$) and control inputs (CEN/$\overline{\text{AEN}}$, CENL, CMDLY, MB, and $\overline{\text{READY}}$) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{\text{S1}}$ and $\overline{\text{S0}}$.

Fig. 6-10 show the basic command and control output timing for read and write bus cycles. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label CMD represents the appropriate command output for the bus cycle. For Fig. 6–10, the CMDLY input is connected to GND and CENL to V_{CC}. The effects of CENL and CMDLY are described later in the section on control inputs.

Fig. 6, 7 and 8 show non-Multibus cycles. MB is connected to GND while CEN is connected to V_{CC}. Fig. 6 shows a read cycle with no wait states while Fig. 7 shows a write cycle with one wait state. The $\overline{\text{READY}}$ input is shown to illustrate how wait states are added.

Fig. 6 – IDEL-READ-IDEL BUS CYCLES WITH MB = 0

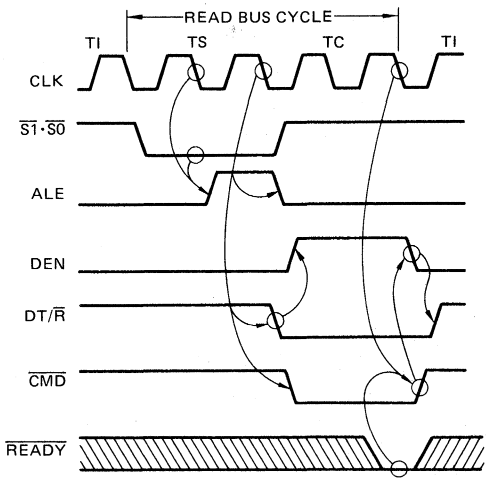
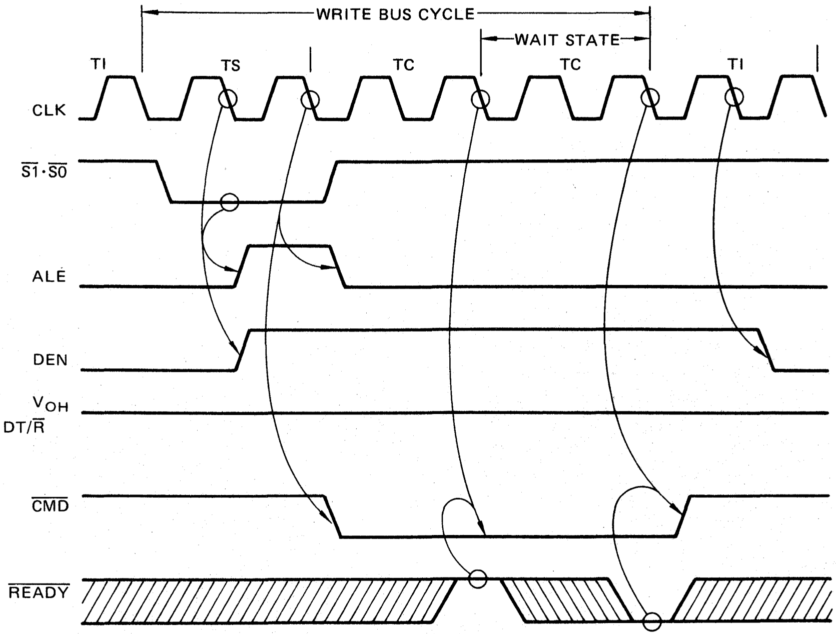


Fig. 7 – IDLE-WRITE-IDLE BUS CYCLES WITH MB = 0



Bus cycles can occur back to back with no TI bus states between TC and TS. Back to back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle.

A special case in control timing occurs for back to back write cycles with MB = 0. In this case, DT/$\overline{R}$ and DEN remain HIGH between the bus cycles (see Fig. 8). The command and ALE output timing does not change.

Fig. 9 and 10 show a Multibus cycle with MB = 1. $\overline{AEN}$ and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described later in the section on control inputs. Fig. 9 shows a read cycle with one wait state and Fig. 10 shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The $\overline{READY}$ input is shown to illustrate how wait states are added.

Fig. 8 – WRITE-WRITE BUS CYCLES WITH MB = 0

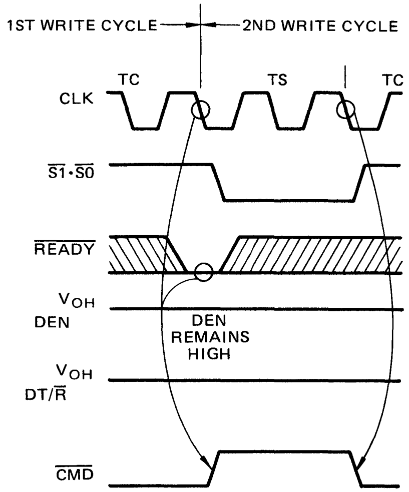
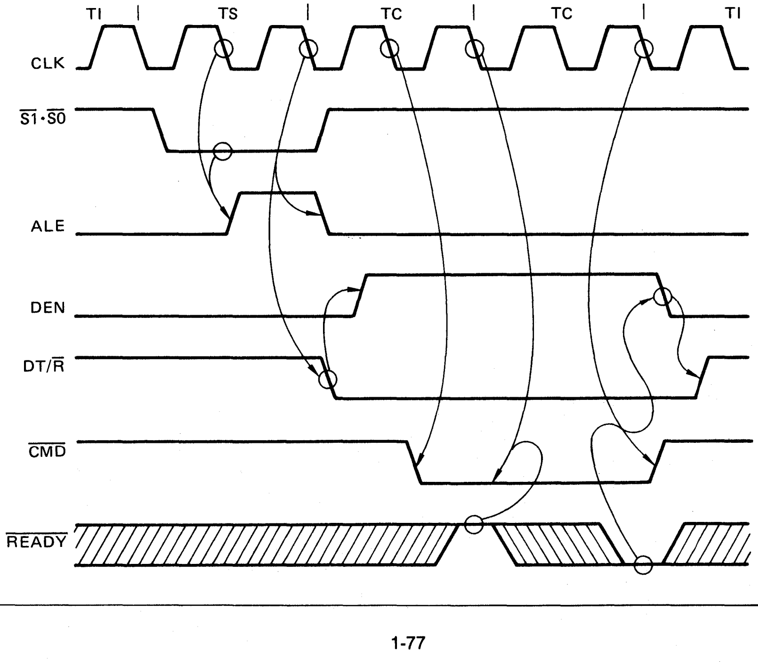
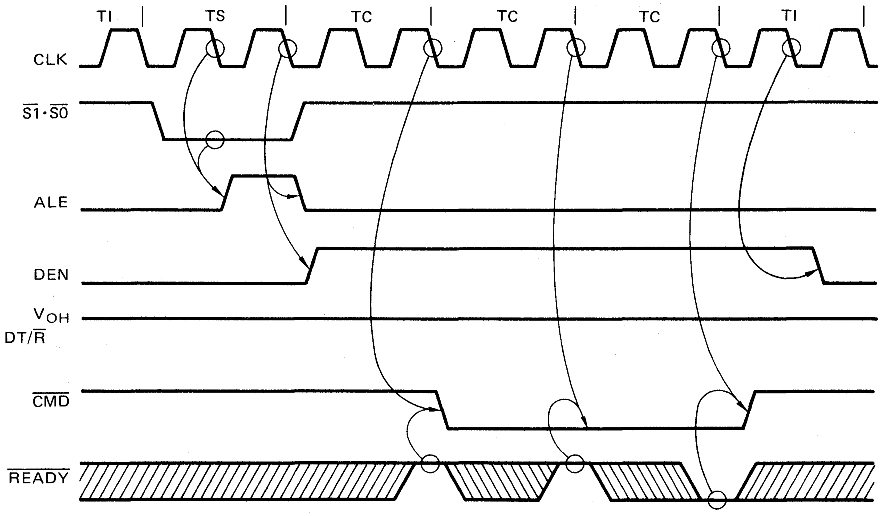


Fig. 9 – IDLE-READ-IDLE BUS CYCLES WITH MB = 1



1

Fig. 10 – IDEL-WRITE-IDLE BUS CYCLES WITH MB = 1



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active.

2) 50 ns minimum setup time for valid write data before any write command output becomes active.

3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach 3-state OFF.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

1) The HIGH to LOW transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) are delayed one CLK cycle.

2) The HIGH to LOW transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) are delayed two CLK cycles.

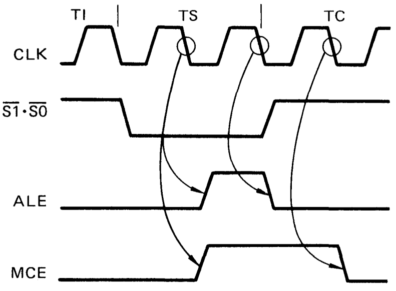
3) The LOW to HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back to back bus cycles with MB = 1 do not change the timing of any of the command of control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during Phase 2 of any TC bus state. ALE is not affected by any control input.

Fig. 11 shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master MBL 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing to a read bus cycle. MCE is not affected by any control input.

Fig. 11 – MCE OPERATION FOR AN INTA BUS CYCLE



CONTROL INPUTS

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many MBL 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the MBL 82288 bus controller, CENL and $\overline{\text{AEN}}$ (see Fig. 12). CENL enables the bus controller to control the current bus cycle. The $\overline{\text{AEN}}$ input prevents a bus controller from driving its command outputs. $\overline{\text{AEN}}$ HIGH means that another bus controller may be driving the shared bus.

In Fig. 12, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The MBL 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{\text{AEN}}$ before it will begin a Multibus operation.

CENL must be sampled HIGH at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled LOW the commands and DEN will not go active and DT/$\overline{\text{R}}$ will remain HIGH. The bus controller will ignore the CMDLY, CEN, and $\overline{\text{READY}}$ inputs until another bus cycle is started via $\overline{\text{S1}}$ and $\overline{\text{S0}}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during Phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, the DEN output will be forced LOW during TC as shown in the timing waveforms.

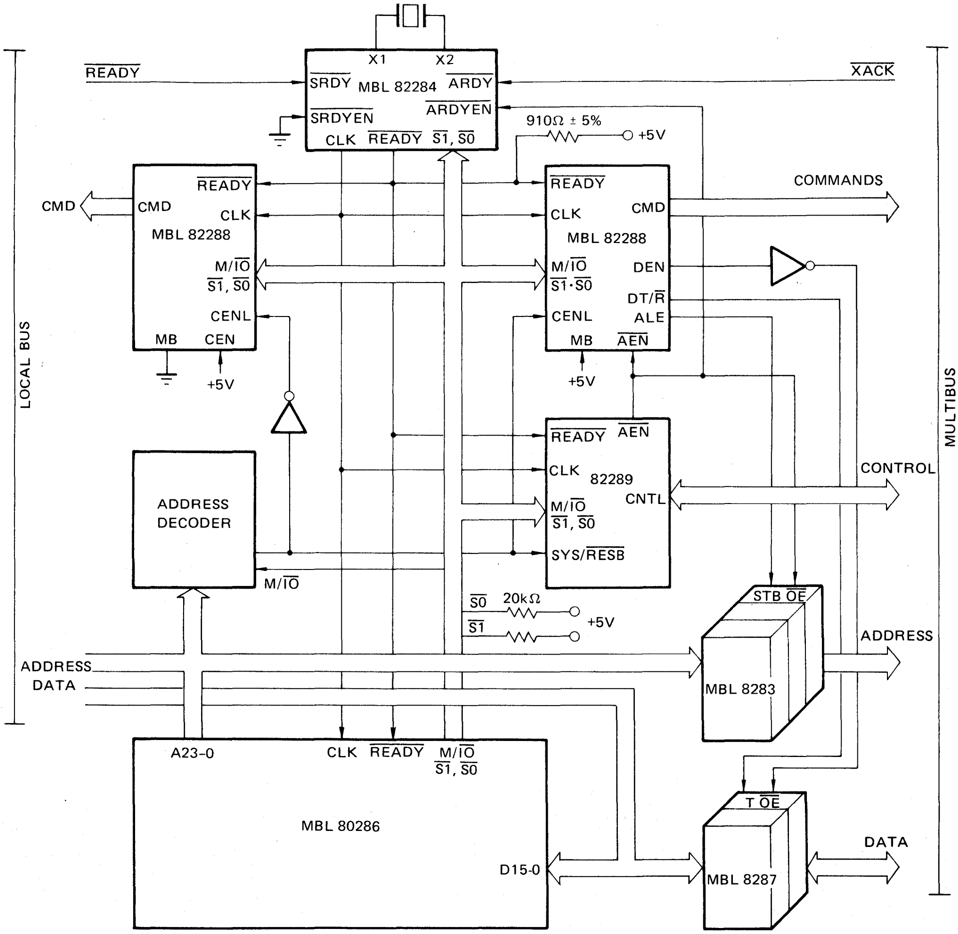
When MB = 1, CEN/$\overline{\text{AEN}}$ becomes $\overline{\text{AEN}}$. $\overline{\text{AEN}}$ controls when the bus controller command outputs enter and exit 3-state OFF. $\overline{\text{AEN}}$ is intended to be driven by a bus arbiter, like the 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{\text{AEN}}$ makes a LOW to HIGH transition, the command outputs immediately enter 3-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into 3-state OFF (see Fig. 12). The LOW to HIGH transition of $\overline{\text{AEN}}$ should only occur during TI or TS bus states.

The HIGH to LOW transition of $\overline{\text{AEN}}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{\text{AEN}}$ can become active during any T-state. $\overline{\text{AEN}}$ LOW immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB=0, CEN/$\overline{\text{AEN}}$ becomes CEN. CEN is an synchronous input which immediately affects the command and DEN outputs. When CEN makes a HIGH to LOW transition, the commands and DEN are immediately forced inactive. When CEN makes a LOW to HIGH transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

Fig. 12 – SYSTEM USE OF $\overline{\text{AEN}}$ AND CENL



CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in Fig. 9 and 10.

$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

WAVEFORMS DISCUSSION

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the MBL 82288; however, most functional descriptions are provided in Fig. 5 through 11.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . −0.5V to +7V
Power Dissipation . . . . 1 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to 70°C)

Symbol	Parameter	MBL 82288-6 (6 MHz)		MBL 82288-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
V_{IL}	Input LOW Voltage	−0.5	0.8	−0.5	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V	
V_{ILC}	CLK Input LOW Voltage	−0.5	0.6	−0.5	0.6	V	
V_{IHC}	CLK Input HIGH Voltage	3.8	V_{CC}+0.5	3.8	V_{CC}+0.5	V	
V_{OL}	Output LOW Voltage: Command Outputs Control Outputs		 0.45 0.45		 0.45 0.45	 V V	 I_{OL} = 32mA, Note 1 I_{OL} = 16mA, Note 2
V_{OH}	Output HIGH Voltage: Command Outputs Control Outputs	 2.4 2.4		 2.4 2.4		 V V	 I_{OH} = −5mA, Note 1 I_{OH} = −1mA, Note 2
I_F	Input Current ($\overline{\text{S0}}$ and $\overline{\text{S1}}$ inputs)		−0.5		−0.5	mA	V_f = 0.45V
I_{IL}	Input Leakage current (all other inputs)		±10		±10	μA	$0V \leqq V_{IN} \leqq V_{CC}$
I_{LO}	Output Leakage Current		±10		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	Power Supply Current		120		120	mA	
C_{CLK}	CLK Input Capacitance		12		12	pF	F_C = 1MHz
C_I	Input Capacitance		10		10	pF	F_C = 1MHz
C_O	Input/Output Capacitance		20		20	pF	F_C = 1MHz

NOTE: 1. Command Outputs are $\overline{\text{INTA}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{MRDC}}$, and $\overline{\text{MWRC}}$.
2. Control Outputs are DT/$\overline{\text{R}}$, DEN, ALE and MCE.

A.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to 70°C)

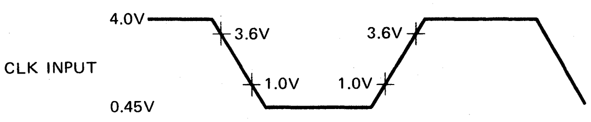
AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	MBL 82288-6 (6 MHz)		MBL 82288-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
1	CLK Period	83	250	62	250	ns	
2	CLK HIGH Time	25	230	20	235	ns	at 3.6V
3	CLK LOW Time	20	225	15	230	ns	at 1.0V
4	CLK Rise Time		10		10	ns	1.0V to 3.6V
5	CLK Fall Time		10		10	ns	3.6V to 1.0V
6	M/$\overline{\text{IO}}$ and Status Setup Time	28		22		ns	
7	M/$\overline{\text{IO}}$ and Status Hold Time	1		1		ns	
8	CENL Setup Time	30		20		ns	
9	CENL Hold Time	1		1		ns	
10	$\overline{\text{READY}}$ Setup Time	50		38		ns	
11	$\overline{\text{READY}}$ Hold Time	35		25		ns	
12	CMDLY Setup Time	25		20		ns	
13	CMDLY Hold Time	1		1		ns	
14	$\overline{\text{AEN}}$ Setup Time	25		20		ns	Note 3
15	$\overline{\text{AEN}}$ Hold Time	0		0		ns	Note 3
16	ALE, MCE Active Delay from CLK	3	25	3	20	ns	Note 4
17	ALE, MCE Inactive Delay from CLK		35		25	ns	Note 4
18	DEN (Write) Inactive from CENL		35		35	ns	Note 4
19	DT/$\overline{\text{R}}$ LOW from CLK		40		25	ns	Note 4
20	DEN (Read) Active from DT/$\overline{\text{R}}$	5	50	5	35	ns	Note 4
21	DEN (Read) Inactive Delay from CLK	3	40	3	35	ns	Note 4
22	DT/$\overline{\text{R}}$ HIGH from DEN Inactive	5	45	5	35	ns	Note 4
23	DEN (Write) Active Delay from CLK		35		30	ns	Note 4
24	DEN (Write) Inactive Delay from CLK	3	35	3	30	ns	Note 4
25	DEN Inactive from CEN		40		30	ns	Note 4
26	DEN Active from CEN		35		30	ns	Note 4
27	DT/$\overline{\text{R}}$ HIGH from CLK (when CEN = LOW)		50		35	ns	Note 4
28	DEN Active from $\overline{\text{AEN}}$		35		30	ns	Note 4
29	$\overline{\text{CMD}}$ Active Delay from CLK	3	40	3	25	ns	Note 5
30	$\overline{\text{CMD}}$ Inactive Delay from CLK	3	30	3	25	ns	Note 5
31	$\overline{\text{CMD}}$ Inactive from CEN		35		25	ns	Note 5
32	$\overline{\text{CMD}}$ Active from CEN		45		25	ns	Note 5
33	$\overline{\text{CMD}}$ Inactive Enable from $\overline{\text{AEN}}$		40		40	ns	Note 5
34	$\overline{\text{CMD}}$ Float Delay from $\overline{\text{AEN}}$		40		40	ns	Note 6
35	MB Setup Time	25		20		ns	
36	MB Hold Time	0		0		ns	
37	Command Inactive Enable from MB↓		40		40	ns	Note 5
38	Command Float Time from MB↑		40		40	ns	Note 6
39	DEN Inactive from MB↑		40		30	ns	Note 4
40	DEN Active from MB↓		35		30	ns	Note 4

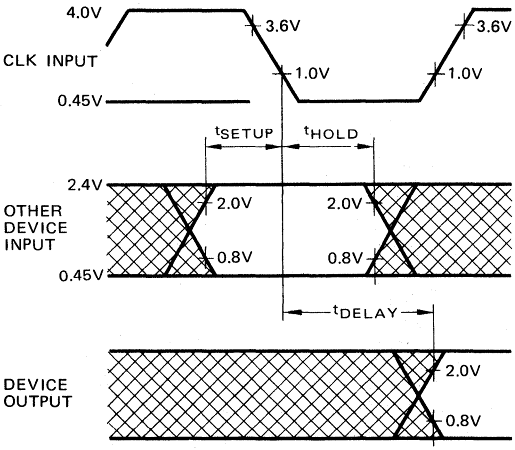
NOTE: 3. $\overline{\text{AEN}}$ is an asynchronous input. This specification is for testing purposes only, to assure recognition at a specific CLK edge.

4. Control output load: C_L= 150pF.
5. Command output load: C_L= 300pF.
6. Float condition occurs when output current is less than I_{LO} in magnitude.

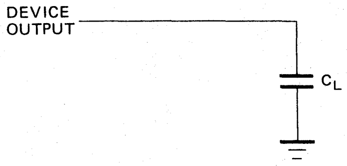
NOTE 7: AC Drive and Measurement Points — CLK Input



NOTE 8: AC Setup, Hold and Delay Time Measurement — General

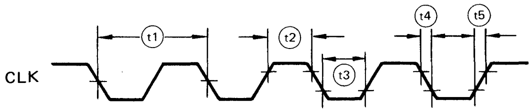


NOTE 9: AC Test Loading on Outputs

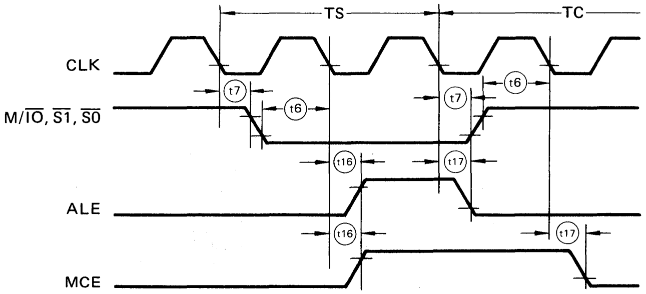


WAVEFORMS

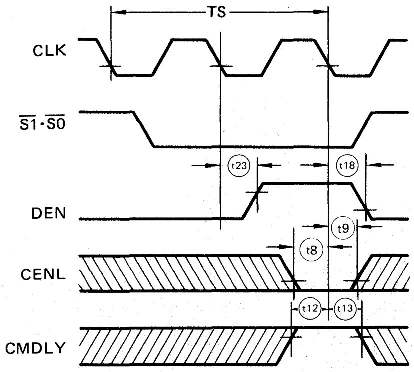
CLK CHARACTERISTICS



STATUS, ALE, MCE, CHARACTERISTICS

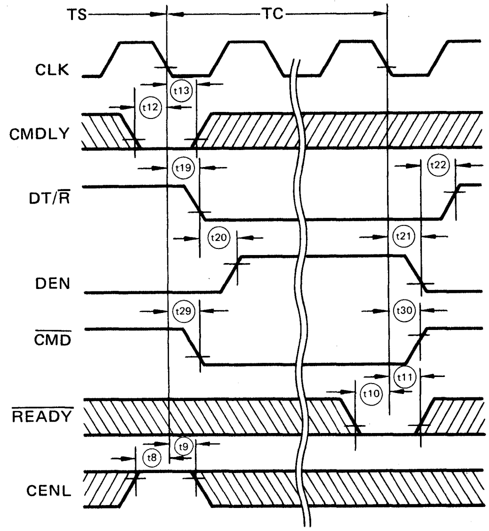


CENL, CMDLY, DEN CHARACTERISTICS WITH MB = 0 AND CEN = 1 DURING WRITE CYCLE

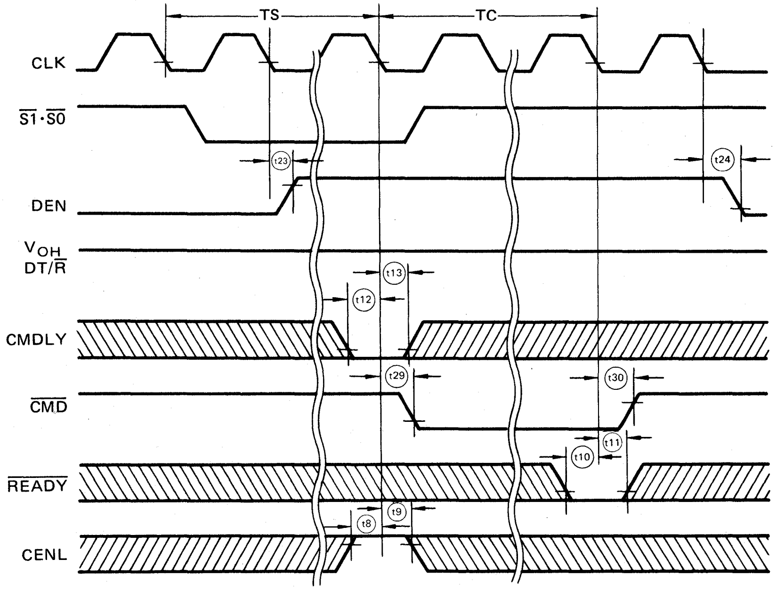


WAVEFORMS (Continued)

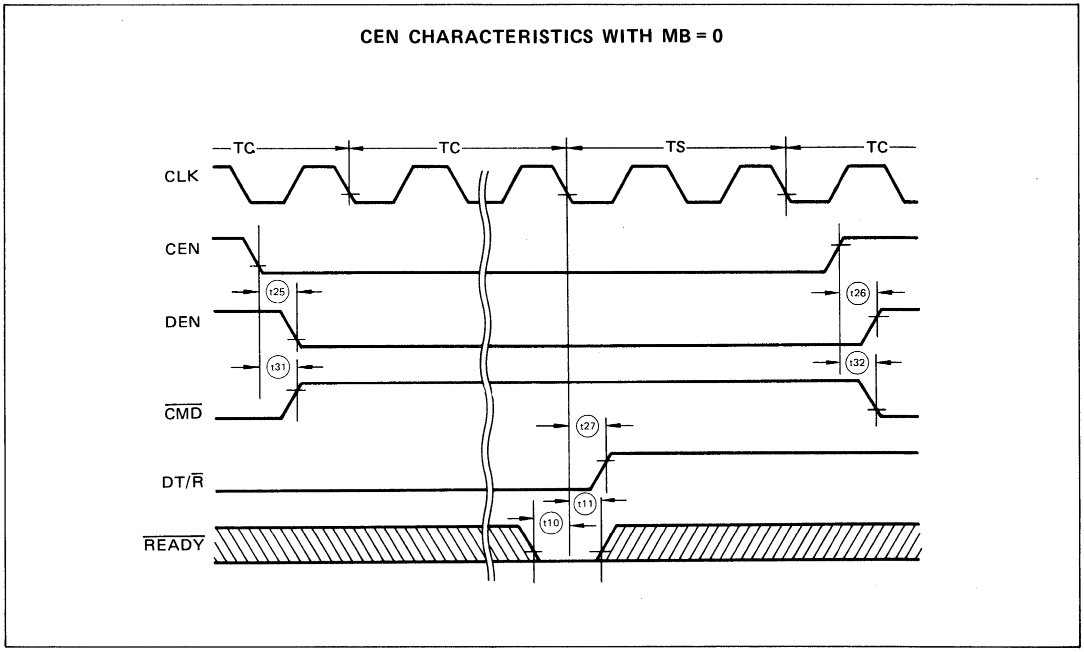
READ CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1



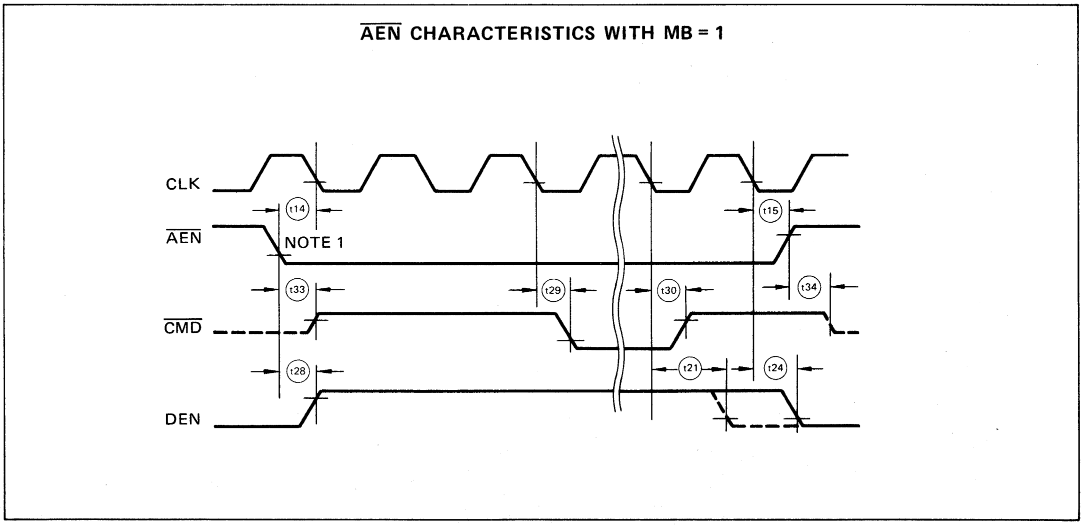
WRITE CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1



WAVEFORMS (Continued)



CEN CHARACTERISTICS WITH MB = 0

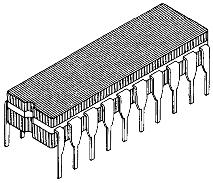


$\overline{\text{AEN}}$ CHARACTERISTICS WITH MB = 1

NOTE 1: $\overline{\text{AEN}}$ is an asynchronous input. $\overline{\text{AEN}}$ setup and hold times are specified to guarantee the response shown in the waveforms.

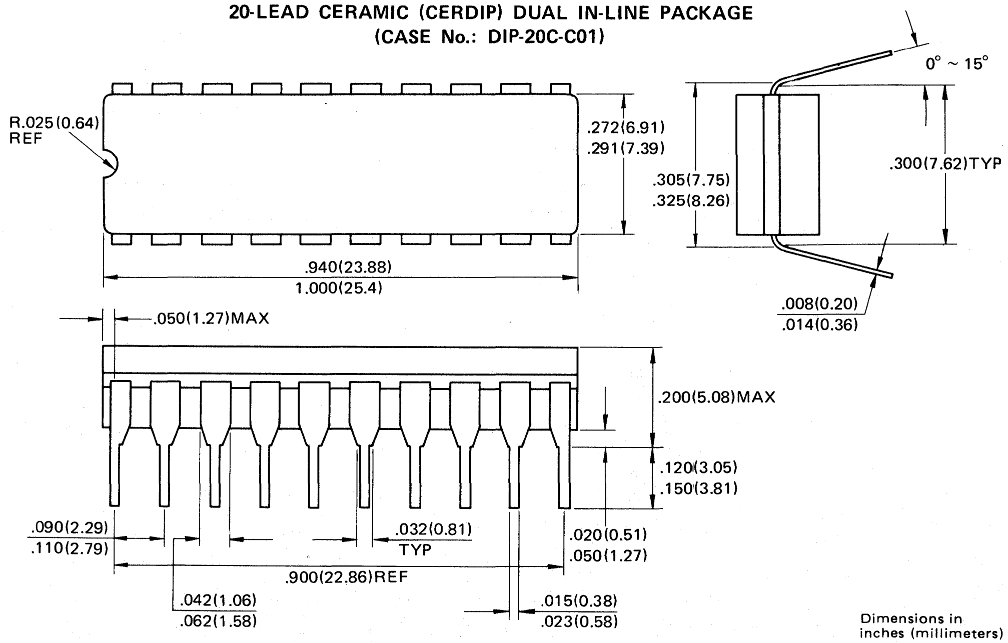
PACKAGE ILLUSTRATION

CERAMIC PACKAGE
(CERDIP)



PACKAGE DIMENSIONS (Suffix -CZ)

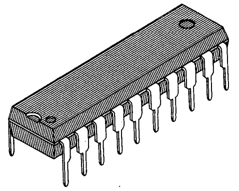
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



Dimensions in
inches (millimeters)

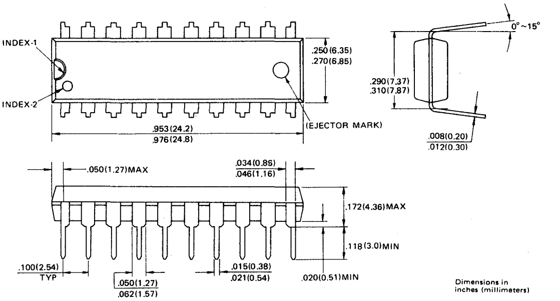
PACKAGE ILLUSTRATION

PLASTIC PACKAGE



PACKAGE DIMENSIONS (Suffix: -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



Dimensions in inches (millimeters)

FUJITSU

NMOS HIGH-INTEGRATION 16-BIT MICROPROCESSOR

MBL 80186
MBL 80186-6

February 1986
Edition 1.0

NMOS HIGH-INTEGRATION 16-BIT MICROPROCESSOR

The Fujitsu MBL 80186 is a highly integrated 16-bit microprocessor. The MBL 80186 effectively combines 15–20 of the most common MBL 8086 system components onto one. The MBL 80186 provides two times greater throughput than the standard 5MHz MBL 8086. The MBL 80186 is upward compatible with MBL 8086 and 88 software and adds 10 new instruction types to the existing set. It is housed in a 68-pad ceramic LCC (Leadless Chip Carrier: JEDEC Type A) or 68-pin Ceramic PGA (Pin Grid Array) package.

- **Integrated Feature Set:**
  - **Enhanced MBL 8086-2 CPU**
  - **Clock Generator**
  - **2 Independent, High-Speed DMA Channels**
  - **Programmable Interrupt Controller**
  - **3 Programmable 16-bit Timers**
  - **Programmable Memory and Peripheral Chip-Select Logic**
  - **Programmable Wait State Generator**
  - **Local Bus Controller**
- **Available in 8MHz (MBL 80186) and cost effective 6MHz (MBL 80186-6) versions.**
- **High-performance Processor**
  - **2 Times the Performance of the Standard MBL 8086**
  - **4 MByte/Sec Bus Bandwidth Interface**
- **Direct Addressing Capability to 1 MByte of Memory**
- **Completely Object Code Compatible with All Existing MBL 8086, 88 Software**
  - **10 New Instruction Types**
- **High Performance Numerical Coprocessing Capability Through Intel 8087 Interface**
- **Two Package Options:**
  - **68-Pad Ceramic LCC (Suffix -CV) (JEDEC Type A)**
  - **68-Pin Ceramic PGA (Suffix -CR)**

Fig. 1 — BLOCK DIAGRAM

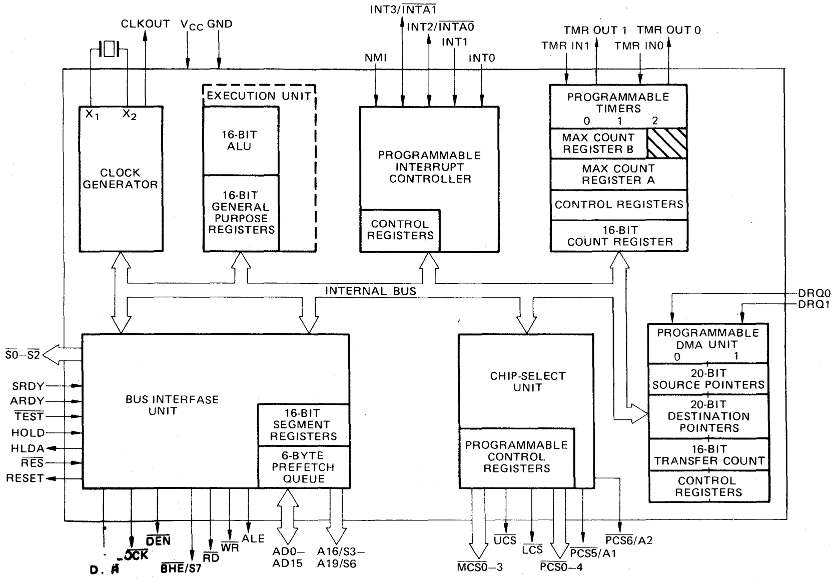


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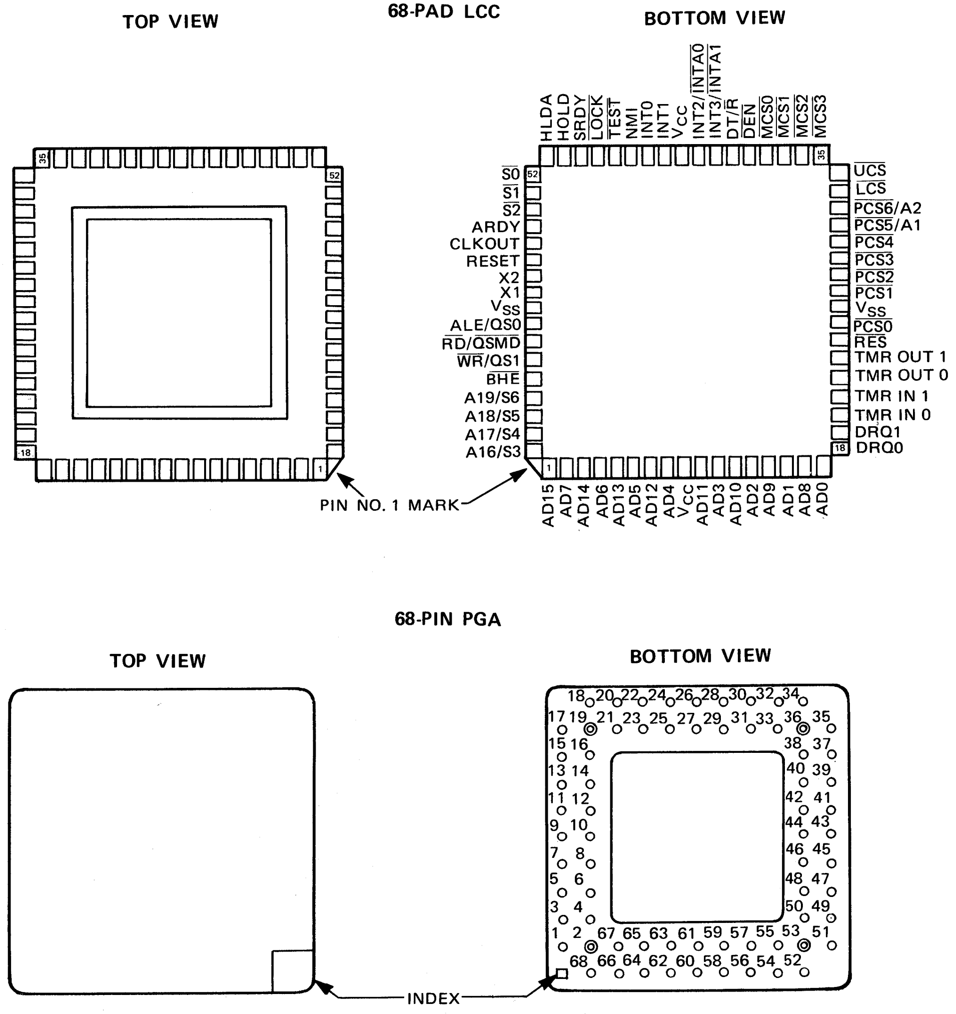
Fig. 2 — PIN CONFIGURATIONS



PIN DESCRIPTION

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
V_{CC}, V_{CC}	9, 43	I	**System Power:** +5 V power supply.
V_{SS}, V_{SS}	26, 60	I	**System Ground.**
RESET	57	O	**Reset Output** indicates that the MBL 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{\text{RES}}$ signal.
X1, X2	59, 58	I	**Crystal Inputs,** X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	**Clock Output** provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLOKOUT. CLKOUT has sufficient MOS drive capabilities for the 8087 Numeric Processor Extension.
$\overline{\text{RES}}$	24	I	**System Reset** causes the MBL 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the MBL 80186 clock. The MBL 80186 begins fetching instructions approximately 7 clock cycels after $\overline{\text{RES}}$ is returned HIGH. $\overline{\text{RES}}$ is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to HIGH transition of $\overline{\text{RES}}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{\text{RES}}$ generation via an RC network. When $\overline{\text{RES}}$ occurs, the MBL 80186 will drive the status lines to an inactive level for one clock, and then tri-state them.
$\overline{\text{TEST}}$	47	I	**$\overline{\text{TEST}}$** is examined by the WAIT instruction. If the $\overline{\text{TEST}}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{\text{TEST}}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the MBL 80186 is waiting for $\overline{\text{TEST}}$, interrupts will be serviced. This input is synchronized internally.
TMR IN 0, TMR IN 1	20 21	I I	**Timer Inputs** are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	**Timer Outputs** are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0, DRQ1	18 19	I I	**DMA Request** is driven HIGH by an external device when it desires that a DMA channel (Channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized.
NMI	46	I	**Non-Maskable Interrupt** is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0, INT1, INT2/$\overline{\text{INTA0}}$, INT3/$\overline{\text{INTA1}}$	45, 44 42 41	I I/O I/O	**Maskable Interrupt Requests** can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

PIN DESCRIPTION (Continued)

Table 1 – PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>A19/S6,
A18/S5,
A17/S4,
A16/S3</td><td>65
66
67
68</td><td>O
O
O
O</td><td><b>Address Bus Outputs (16–19)</b> and <b>Bus Cycle Status (3–6)</b> reflect the four most significant address bits during T1. These signals are active HIGH. During T2, T3, Tw and T4, status information is available on these lines as encoded below:
<table>
<tr><th></th><th>Low</th><th>High</th></tr>
<tr><td>S6</td><td>Processor Cycle</td><td>DMA Cycle</td></tr>
</table>
S3, S4, and S5 are defined as LOW during T2–T4.</td></tr>
<tr><td>AD15–AD0</td><td>10–17,
1–8</td><td>I/O</td><td><b>Address/Data Bus (0–15)</b> signals constitute the time mutiplexed memory or I/O address (T1) and data (T2, T3, Tw, and T4) bus. The bus is active HIGH. A0 is analogous to $\overline{\mathrm{BHE}}$ for the lower byte of the data bus, pins D7 through D0. It is LOW during T1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.</td></tr>
<tr><td>$\overline{\mathrm{BHE}}$/S7</td><td>64</td><td>O</td><td>During T1 the <b>Bus High Enable</b> signal should be used to determine if data is to be enabled onto the most significant half of the data bus, pin D15–D8. $\overline{\mathrm{BHE}}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S7 status information is available during T2, T3, and T4. S7 is logically equivalent to $\overline{\mathrm{BHE}}$. The signal is active LOW, and is tristated OFF during bus HOLD.
<table>
<tr><th colspan="3">$\overline{\mathrm{BHE}}$ and A0 Encodings</th></tr>
<tr><th>$\overline{\mathrm{BHE}}$ Value</th><th>A0 Value</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Byte Transfer on upper half of data bus (D15–D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte Transfer on lower half of data bus (D7–D0)</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>ALE/QS0</td><td>61</td><td>O</td><td><b>Address Latch Enable/Queue Status 0</b> is provided by the MBL 80186 to latch the address into the MBL 8282/8283 address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T1 of the associated bus cycle, effectively one-half clock cycle earlier than in the standard MBL 8086. The trailing edge is generated off the CLKOUT rising edge in T1 as in the MBL 8086. Note that ALE is never floated.</td></tr>
<tr><td>$\overline{\mathrm{WR}}$/QS1</td><td>63</td><td>O</td><td><b>Write Strobe/Queue Status 1</b> indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{\mathrm{WR}}$ is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during Reset, and then floated. When the MBL 80186 is in queue status mode, the ALE/QS0 and $\overline{\mathrm{WR}}$/QS1 pins provide information about processor/instruction queue interaction.
<table>
<tr><th>QS1</th><th>QS0</th><th>Queue Operation</th></tr>
<tr><td>0</td><td>0</td><td>No queue operation</td></tr>
<tr><td>0</td><td>1</td><td>First opcode byte fetched from the queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent byte fetched from the queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the queue</td></tr>
</table></td></tr>
<tr><td>$\overline{\mathrm{RD}}$/$\overline{\mathrm{QSMD}}$</td><td>62</td><td>O</td><td><b>Read Strobe</b> indicates that the MBL 80186 is performing a memory or I/O read cycle. $\overline{\mathrm{RD}}$ is active LOW for T2, T3, and Tw of any read cycle. It is guaranteed not to go LOW in T2 until after the Address Bus is floated. $\overline{\mathrm{RD}}$ is active LOW, and floats during "HOLD." $\overline{\mathrm{RD}}$ is driven HIGH for one clock during Reset, and then the output driver is floated. A weak internal pull-up mechanism on the $\overline{\mathrm{RD}}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the MBL 80186 should provide ALE, $\overline{\mathrm{WR}}$ and $\overline{\mathrm{RD}}$, or if the Queue-Status should be provided. $\overline{\mathrm{RD}}$ should be connected to GND to provide Queue-Status data.</td></tr>
</table>

PIN DESCRIPTION (Continued)

Table 1 – PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>ARDY</td><td>55</td><td>I</td><td><b>Asynchronous Ready</b> informs the MBL 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the MBL 80186. This means that the falling edge of ARDY must be synchronized to the MBL 80186 clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied LOW.</td></tr>
<tr><td>SRDY</td><td>49</td><td>I</td><td><b>Synchronous Ready</b> must be synchronized externally to the MBL 80186. The use of SRDY provides a relaxed system-timing specification on the Ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW.</td></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>48</td><td>O</td><td><b>$\overline{\text{LOCK}}$</b> output indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active LOW. The $\overline{\text{LOCK}}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{\text{LOCK}}$ is asserted. $\overline{\text{LOCK}}$ is active LOW, is driven HIGH for one clock during RESET, and then floated.</td></tr>
<tr><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{S2}}$</td><td>52–54</td><td>O</td><td><b>Bus Cycle Status</b> $\overline{\text{S0}}$–$\overline{\text{S2}}$ are encoded to provide bus-transaction information:
<table>
<tr><th colspan="4">MBL 80186 Bus Cycle Status Information</th></tr>
<tr><th>$\overline{\text{S2}}$</th><th>$\overline{\text{S1}}$</th><th>$\overline{\text{S0}}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Data from Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Data to Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (no bus cycle)</td></tr>
</table>
The status pins float during "HOLD."
$\overline{\text{S2}}$ may be used as a logical M/$\overline{\text{IO}}$ indicator, and $\overline{\text{S1}}$ as a DT/$\overline{\text{R}}$ indicator. The status lines are driven HIGH for one clock during Reset, and then floated until a bus cycle begins.</td></tr>
<tr><td>HOLD,
HLDA</td><td>50
51</td><td>I
O</td><td><b>HOLD</b> indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the MBL 80186 clock. The MBL 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T4 or T1. Simultaneous with the issuance of HLDA, the MBL 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the MBL 80186 will lower HLDA. When the MBL 80186 needs to run another bus cycle, it will again drive the local bus and control lines.</td></tr>
<tr><td>$\overline{\text{UCS}}$</td><td>34</td><td>O</td><td><b>Upper Memory Chip Select</b> is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{\text{UCS}}$ is software programmable.</td></tr>
</table>

PIN DESCRIPTION (Continued)

Table 1 – PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{\text{LCS}}$	33	O	**Lower Memory Chip Select** is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{\text{LCS}}$ is software programmable.
$\overline{\text{MCS0}}$–3	38–35	O	**Mid-Range Memory Chip Select** signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{\text{MCS0}}$–3 are software programmable.
$\overline{\text{PCS0}}$-4	25, 27–30	O	**Peripheral Chip Select Signals 0–4** are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{\text{PCS0}}$–4 are software programmable.
$\overline{\text{PCS5}}$/A1	31	O	**Peripheral Chip Select 5 or Latched A1** may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{\text{PCS5}}$ is software programmable. When programmed to provide latched A1, rather than $\overline{\text{PCS5}}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active HIGH.
$\overline{\text{PCS6}}$/A2	32	O	**Peripheral Chip Select 6 or Latched A2** may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{\text{PCS6}}$ is software programmable. When programmed to provide latched A2, rather than $\overline{\text{PCS6}}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active HIGH.
DT/$\overline{\text{R}}$	40	O	**Data Transmit/Receive** controls the direction of data flow through the external MBL 8286/8287 data bus transceiver. When LOW, data is transferred to the MBL 80186. When HIGH, the MBL 80186 places write data on the data bus.
$\overline{\text{DEN}}$	39	O	**Data Enable** is provided as an MBL 8286/8287 data bus transceiver output enable. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access. $\overline{\text{DEN}}$ is HIGH whenever DT/$\overline{\text{R}}$ changes state.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The following Functional Description describes the base architecture of the MBL 80186. This architecture is common to the MBL 8086, 88, and 286 microprocessor families as well. The MBL 80186 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard MBL 8086. The MBL 80186 is object code compatible with the MBL 8086, 88 microprocessors and adds 10 new instruction types to the existing MBL 8086, 88 instruction set.

MBL 80186 BASE ARCHITECTURE

The MBL 8086, 88, 186, and 286 family all contain the same basic set of registers, instructions, and addressing modes. The MBL 80186 processor is upward compatible with the MBL 8086, 8088, and 80286 CPUs.

Register Set

The MBL 80186 base architecture has fourteen registers as shown in Fig. 3a and 3b. These registers are grouped into the following categories.

- **General Registers**

Eight 16-bit general purpose registers may be used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

- **Segment Registers**

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization).

- **Base and Index Registers**

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

- **Status and Control Registers**

Two 16-bit special purpose registers record or alter certain aspects of the MBL 80186 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Fig. 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the MBL 80186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

Fig. 3a – MBL 80186 GENERAL PURPOSE REGISTER SET

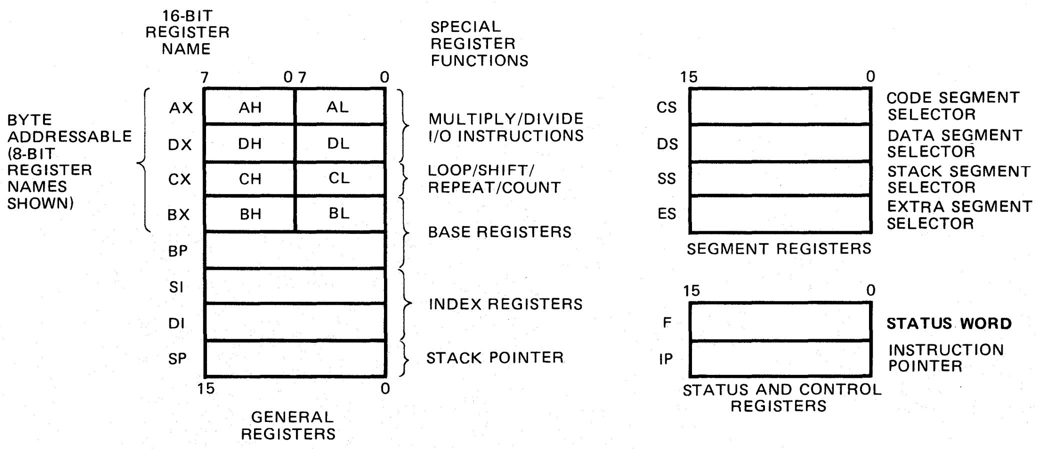


Fig. 3b – STATUS WORD FORMAT

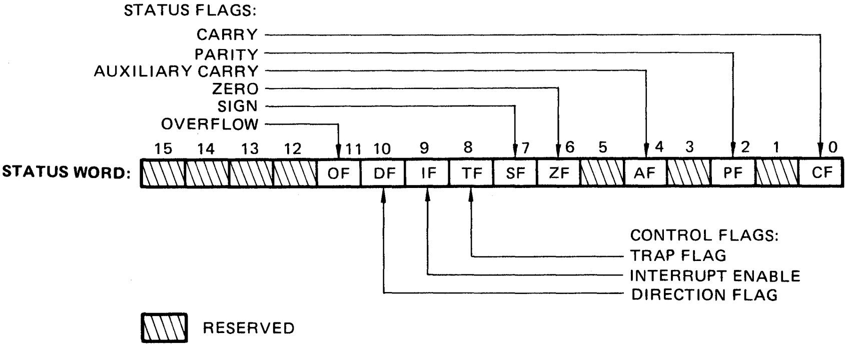


Table 2 – STATUS WORD BIT FUNCTIONS

Bit Position	Name	Function
0	CF	Carry Flag – Set on high-order bit carry or borrow; cleared otherwise.
2	PF	Parity Flag – Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise.
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise.
6	ZF	Zero Flag – Set if result is zero; cleared otherwise.
7	SF	Sign Flag – Set equal to high-order bit or result (0 if positive, 1 if negative).
8	TF	Single Step Flag – Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-Enable Flag – When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag – Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag – Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Fig. 4.

An MBL 80186 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Fig. 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Fig. 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

Fig.4 – MBL 80186 INSTRUCTION SET

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Fig. 4 — MBL 80186 INSTRUCTION SET (Continued)

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign
JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign

UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

Fig. 5 — TWO COMPONENT ADDRESS

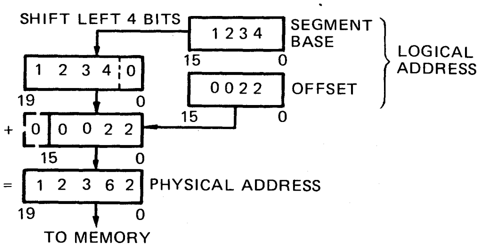
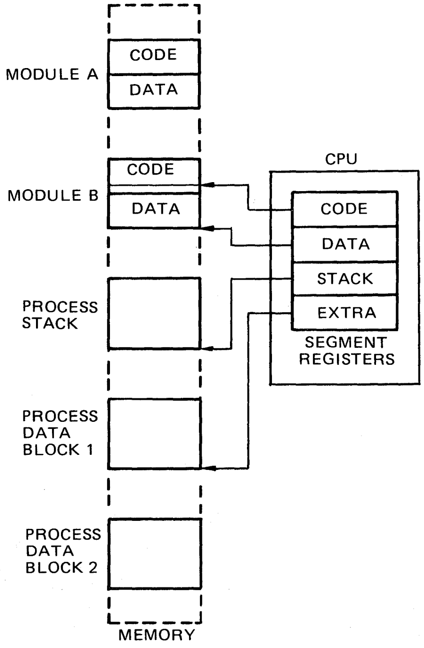


Table 3 — SEGMENT REGISTER SELECTION RULES

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

Fig. 6 — SEGMENTED MEMORY HELPS STRUCTURE SOFTWARE



Addressing Modes

The MBL 80186 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The MBL 80186 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using the MBL 80186 and Intel 8087 Numeric Data Processor.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using the MBL 80186 and Intel 8087 Numeric Data Processor configuration.)

In general, individual data elements must fit within defined segment limits. Fig. 7 graphically represents the data types supported by the MBL 80186.

I/O Space

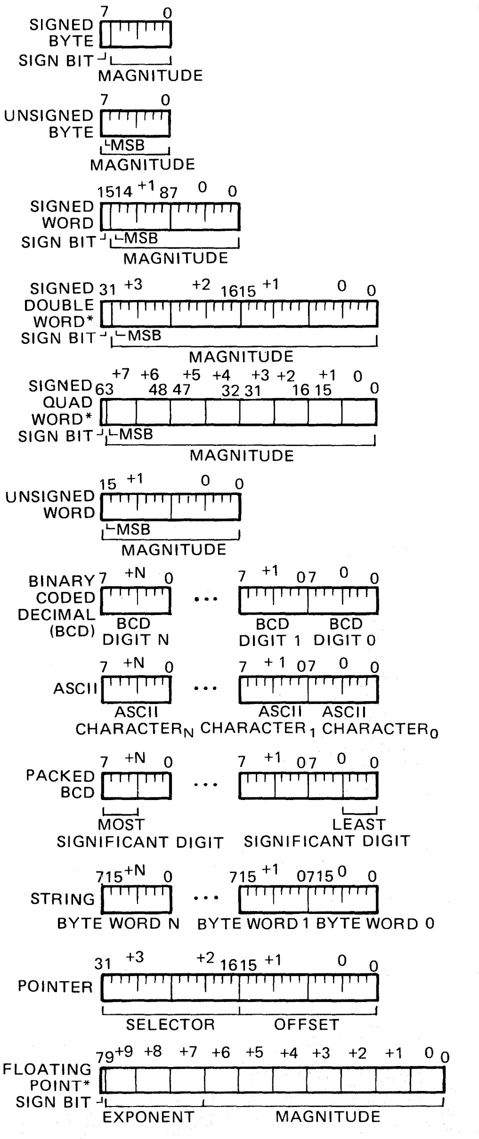
The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A15–A8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the

Fig. 7 — MBL 80186 SUPPORTED DATA TYPES



NOTE:
*SUPPORTED BY MBL 80188 AND INTEL 8087 NUMERIC DATA PROCESSOR CONFIGURATION.

exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0-31, some of which are used for instruction exceptions, are reserved. Table 4 shows the MBL 80186 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the MBL 80186 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and non-cascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The MBL 80186 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INTO, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

The software generated MBL 80186 interrupts are described below.

- **Divide Error Exception (Type 0)**

Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

- **Single-Step Interrupt (Type 1)**

Generated after most instructions if the TF flag is set. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction.

Table 4 – MBL 80186 INTERRUPT VECTORS

Interrupt Name	Vector Type	Default Priority	Related Instructions
Divide Error Exception	0	*1	DIV, IDIV
Single Step Interrupt	1	12**2	All
NMI	2	1	All
Breakpoint Interrupt	3	*1	INT
INTO Detected Overflow Exception	4	*1	INTO
Array Bounds Exception	5	*1	BOUND
Unused-Opcode Exception	6	*1	Undefined Opcodes
ESC Opcode Exception	7	*1***	ESC Opcodes
Timer 0 Interrupt	8	2A****	
Timer 1 Interrupt	18	2B****	
Timer 2 Interrupt	19	2C****	
Reserved	9	3	
DMA 0 Interrupt	10	4	
DMA 1 Interrupt	11	5	
INTO Interrupt	12	6	
INT1 Interrupt	13	7	
INT2 Interrupt	14	8	
INT3 Interrupt	15	9	

NOTES:

*1. These are generated as the result of an instruction execution.

**2. This is handled as in the MBL 8086.

****3. All three timers constitute one source of request to the interrupt controller. The Timer interrupts all have the same default priority level with respect to all other interrupt sources. However, they have a defined priority ordering amongst themselves. (Priority 2A is higher priority than 2B.) Each Timer interrupt has a separate vector type number.

4. Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.

***5. An escape opcode will cause a trap only if the proper bit is set in the peripheral control block relocation register.

- **Non-Maskable Interrupt—NMI (Type 2)**

An external interrupt source which cannot be masked.

- **Breakpoint Interrupt (Type 3)**

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

- **INTO Detected Overflow Exception (Type 4)**

Generated during an INTO instruction if the OF bit is set.

- **Array Bounds Exception (Type 5)**

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

- **Unused Opcode Exception (Type 6)**

Generated if execution is attempted on undefined opcodes.

- **Escape Opcode Exception (Type 7)**

Generated if execution is attempted of ESC opcodes (D8H-DFH). This exception will only be generated if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The MBL 80186 provides maskable hardware interrupt request pins INTO–INT3. In addition, maskable interrupts may be generated by the MBL 80186 integrated DMA controller and the integrated timer unit. The vector types for these interrupts is shown in Table 4. Software enables these inputs by setting the interrupt flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the MBL 80186 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt (NMI) is also provided. This interrupt is serviced regardless of the state of the IF bit. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced.

Single-Step Interrupt

The MBL 80186 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single-step interrupt and is controlled by the single-step flag bit (TF) in the Status Word. Once this bit is set, an internal single-step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{\text{RES}}$ input pin LOW. $\overline{\text{RES}}$ forces the MBL 80186 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{\text{RES}}$ is active. After $\overline{\text{RES}}$ becomes inactive and an internal processing interval elapses, the MBL 80186 begins execution with the instruction at physical location FFFF0(H). $\overline{\text{RES}}$ also sets some registers to predefined values as shown in Table 5.

Table 5 – MBL 80186 INITIAL REGISTER STATE AFTER RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

MBL 80186 CLOCK GENERATOR

The MBL 80186 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

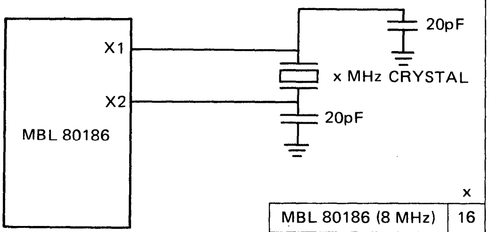
Oscillator

The oscillator circuit of the MBL 80186 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the MBL 80186. The crystal frequency selected will be double the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the MBL 80186. The recommended crystal configuration is shown in Fig. 8.

The following parameters may be used for choosing a crystal:

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	30Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C1 (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max

Fig. 8 – RECOMMENDED MBL 80186 CRYSTAL CONFIGURATION



	x
MBL 80186 (8 MHz)	16
MBL 80186 (6 MHz)	12

Clock Generator

The MBL 80186 clock generator provides the 50% duty cycle processor clock for the MBL 80186. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the MBL 80186. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The MBL 80186 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T2, T3 and again in the middle of each TW until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used. Full synchronization is performed only on the rising edge of ARDY, i.e., the falling edge of ARDY must be synchronized to the CLKOUT signal if it will occur during T2, T3 or TW. High-to-LOW transitions of ARDY must be performed synchronously to the CPU clock.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T2, T3 and again at the end of each TW until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated.

This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the MBL 80186, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The MBL 80186 provides both a $\overline{\text{RES}}$ input pin and a synchronized RESET pin for use with other system components. The $\overline{\text{RES}}$ input pin on the MBL 80186 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET is guaranteed to remain active for at least five clocks given a $\overline{\text{RES}}$ input of at least six clocks. RESET may be delayed up to two and one-half clocks behind $\overline{\text{RES}}$.

Multiple MBL 80186 processors may be synchronized through the $\overline{\text{RES}}$ input pin, since this input resets both the processor and divide-by-two internal counter in the clock generator. In order to insure that the divide-by-two counters all begin counting at the same time, the active going edge of $\overline{\text{RES}}$ must satisfy a 25 ns setup time before the falling edge of the MBL 80186 clock input. In addition, in order to insure that all CPUs begin executing in the same clock cycle, the reset must satisfy a 25 ns setup time before the rising edge of the CLKOUT signal of all the processors.

LOCAL BUS CONTROLLER

The MBL 80186 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides control lines that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The MBL 80186 provides ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ bus control signals. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are used to strobe data from memory to the MBL 80186 or to strobe data from the MBL 80186 to memory. The ALE line provides a strobe to address latches for the multiplexed address/data bus. The MBL 80186 local bus controller does not provide a memory/$\overline{\text{I/O}}$ signal. If this is required, the user will have to use the $\overline{\text{S2}}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The MBL 80186 generates two control signals to be connected to MBL 8286/8287 transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{\text{R}}$ and $\overline{\text{DEN}}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6 – TRANSCEIVER CONTROL SIGNALS DESCRIPTION

Pin Name	Function
$\overline{\text{DEN}}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{\text{R}}$ (Data Transmit/ Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The MBL 80186 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The MBL 80186 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. This requires external circuitry to arbitrate which external device will gain control of the bus from the MBL 80186 when there is more than one alternate local bus master. When the MBL 80186 relinquishes control of the local bus, it floats $\overline{\text{DEN}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{S0}}$-$\overline{\text{S2}}$, $\overline{\text{LOCK}}$, AD0-AD15, A16-A19, $\overline{\text{BHE}}$, and DT/$\overline{\text{R}}$ to allow another master to drive these lines directly.

The MBL 80186 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is the highest-priority activity request which the processor may receive: higher than instruction fetching or internal DMA cycles. However, if a DMA cycle is in progress, the MBL 80186 will complete the transfer before relinquishing the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency time can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clocks or more, if WAIT states are required. In addition, it locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

Local Bus Controller and Reset

Upon receipt of a RESET pulse from the $\overline{\text{RES}}$ input, the local bus controller will perform the following actions:

- Drive $\overline{\text{DEN}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ HIGH for one clock cycle, then float.

> **NOTE:** $\overline{\text{RD}}$ is also provided with an internal pull-up device to prevent the processor from inadvertently entering Queue Status mode during reset.

- Drive $\overline{S0}$–$\overline{S2}$ to the passive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Tristate AD0–15, A16–19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE LOW (ALE is never floated).
- Drive HLDA LOW.

INTERNAL PERIPHERAL INTERFACE

All the MBL 80186 integrated peripherals are controlled via 16-bit registers contained within an internal 256-byte control block. This control block may be mapped into either memory or I/O space. Internal logic will recognize the address and respond to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D15-0, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the MBL 80186 CPU at any time. The location of any register contained within the 256-byte control block is determined by the current base address of the control block.

The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Fig. 9). It provides the upper 12 bits of the base address of the control block. Note that mapping the control register block into an address range corresponding to a chip-select range is not recommended (the chip select circuitry is discussed later in this data sheet). In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space, whereas if the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).
In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into iRMX mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register is set to 20FFH. This causes the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Fig. 10.

The integrated MBL 80186 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data locations in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks. The overall interaction and function of the peripheral blocks has not substantially changed.

CHIP-SELECT/READY GENERATION LOGIC

The MBL 80186 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The MBL 80186 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

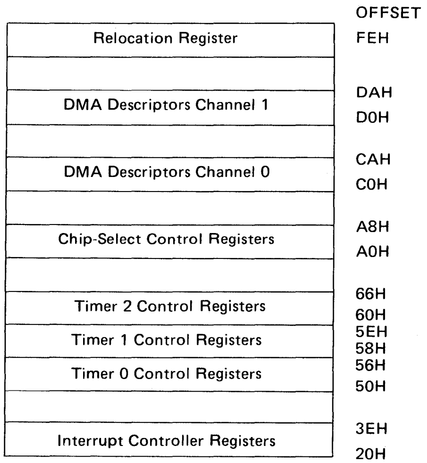
The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes, whereas MBL 80186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

Fig. 9 – RELOCATION REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: FEH	ET	RMX	X	M/IO	Relocation Address Bits R19–R8											

ET = ESC Trap / No ESC Trap (1/0)
M/IO = Register block located in Memory / I/O Space (1/0)
RMX = Master Interrupt Controller mode / iRMX compatible Interrupt Controller mode (0/1)

Fig. 10 – INTERNAL REGISTER MAP


OFFSET
Relocation Register
FEH
DAH
DMA Descriptors Channel 1
D0H
CAH
DMA Descriptors Channel 0
C0H
A8H
Chip-Select Control Registers
A0H
66H
Timer 2 Control Registers
60H
5EH
Timer 1 Control Registers
58H
56H
Timer 0 Control Registers
50H
3EH
Interrupt Controller Registers
20H

- **Upper Memory $\overline{\text{CS}}$**

The MBL 80186 provides a chip select, called $\overline{\text{UCS}}$, for the top of memory. The top of memory is usually used as the system memory because after reset the MBL 80186 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

The lower limit of this memory block is defined in the UMCS register (see Fig. 11). This register is at offset A0H in the internal control block. The legal values for bits 6-13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6-13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

Any internally generated 20-bit address whose upper 16 bits are greater than or equal to UMCS (with bits 0-5 "0") will cause UCS to be activated. UMCS bits R2-R0 are used to specify READY mode for the area or memory defined by this chip-select register, as explained below.

Table 7 – UMCS PROGRAMMING VALUES

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0 = R1 = R2 = 0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

- **Lower Memory $\overline{\text{CS}}$**

The MBL 80186 provides a chip select for low memory called $\overline{\text{LCS}}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is also defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

The upper limit of this memory block is defined in the LMCS register (see Fig. 12). This register is at offset A2H in the internal control block. The legal values for bits 6-15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6-15 not shown in Table 8 will result in undefined operation. After reset, the LMCS register value is undefined. However, the $\overline{\text{LCS}}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0-5 "1") will cause $\overline{\text{LCS}}$ to be active. LMCS register bits R2-R0 are used to specify the READY mode for the area of memory defined by this chip-select register.

Table 8 – LMCS PROGRAMMING VALUES

Upper Address	Memory Block Size	LMCS Value (Assuming R0 = R1 = R2 = 0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

- **Mid-Range Memory $\overline{\text{CS}}$**

The MBL 80186 provides four $\overline{\text{MCS}}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the MBL 80186 1M byte memory address space exclusive of the areas defined by $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8-14 of the MPCS register (see Fig. 13). This register is at location A8H in the internal control block. One and only one of bits 8-14 must be set at a time. Unpredictable operation of the $\overline{\text{MCS}}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. Thus, if the total block size is 32K, each chip select is active for 8K of memory with $\overline{\text{MCS0}}$ being active for the first range and $\overline{\text{MCS3}}$ being active for last range.

The EX and MS in MPCS relate to peripheral functionally as described in a later section.

Table 9 – MPCS PROGRAMMING VALUES

Total Block Size	Individual Select Size	MPCS Bits 14-8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15-9 of the MMCS register (see Fig. 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19-A13 of the 20-bit memory address. Bits A12-A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{\text{MCS}}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After reset, the contents of both of these registers are undefined. However, none of the $\overline{\text{MCS}}$ lines will be active until both the MMCS and MPCS registers are accessed.

MMCS bits R2-R0 specify READY mode of operation for all mid-range chip selects. All devices in mid-range memory must use the same number of WAIT states.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{\text{LCS}}$ line was programmed, there would be an internal conflict between the $\overline{\text{LCS}}$ ready generation logic and the $\overline{\text{MCS}}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{\text{UCS}}$ ready generation logic. Since the $\overline{\text{LCS}}$ chip-select line does not become active until programmed, while the $\overline{\text{UCS}}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{\text{LCS}}$ range must not be programmed.

Peripheral Chip Selects

The MBL 80186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Fig. 11 – UMCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A0H	1	1	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
	A19								A11							

Fig. 12 – LMCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A2H	0	0	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
	A19								A11							

Fig. 13 – MPCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A8H	1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0

Fig. 14 – MMCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A6H	U	U	U	U	U	U	U	1	1	1	1	1	1	R2	R1	R0
	A19						A13									

Seven $\overline{\text{CS}}$ lines called $\overline{\text{PCS0}}$-6 are generated by the MBL 80186. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{\text{PCS5}}$ and $\overline{\text{PCS6}}$ can also be programmed to provide latched address bits A1, A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0, A1 pins used for selecting internal registers of 8-bit peripheral chips. This scheme simplifies the hardware interface because the 8-bit registers of peripherals are simply treated as 16-bit registers located on even boundaries in I/O space or memory space where only the lower 8-bits of the register are significant: the upper 8-bits are "don't cares."

The starting address of the peripheral chip-select block is defined by the PACS register (see Fig. 15). This register is located at offset A4H in the internal control block. Bits 15-6 of this register correspond to bits 19-10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9-0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12-15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

The user should program bits 15-6 to correspond to the desired peripheral base location. PACS bits 0-2 are used to specify READY mode for $\overline{\text{PCS0}}$-$\overline{\text{PCS3}}$.

Table 10 – PCS ADDRESS RANGES

PCS Line	Active between Locations
PCS0	PBA – PBA + 127
PCS1	PBA + 128 – PBA + 255
PCS2	PBA + 256 – PBA + 383
PCS3	PBA + 384 – PBA + 511
PCS4	PBA + 512 – PBA + 639
PCS5	PBA + 640 – PBA + 767
PCS6	PBA + 768 – PBA + 895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Fig. 16). This register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{\text{PCS5}}$ and $\overline{\text{PCS6}}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After reset, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

MPCS bits 0-2 are used to specify READY mode for $\overline{\text{PCS4}}$-$\overline{\text{PCS6}}$ as outlined below.

Fig. 15 – PACS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A4H	U	U	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
	A19									A10						

Table 11 – MS, EX PROGRAMMING VALUES

Bit	Description
MS	1 = Peripherals mapped into memory space. 0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided. 1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

READY Generation Logic

The MBL 80186 can generate a "READY" signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the MBL 80186 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the MBL 80186. The interpretation of the ready bits is shown in Table 12.

Table 12 – READY BITS PROGRAMMING

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). This means, for example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$-3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$-6 READY mode.

Chip Select/Ready Logic and Reset

Upon reset, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to allow the maximum number of internal wait states in conjunction with external Ready consideration (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA CHANNELS

The MBL 80186 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of one Mword/sec or 2 MBytes/sec.

DMA Operation

Each channel has six registers in the control block which define each channel's specific operation. The control registers consist of a 20-bit Source Pointer (2 words), a 20-bit Destination Pointer (2 words), a 16-bit Transfer

Fig. 16 – MPCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A8H	1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0

Counter, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Fig. 18). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13 – DMA CONTROL BLOCK FORMAT

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Counter	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	COH	DOH

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular MBL 80186 DMA channel. This register specifies:

- the mode of synchronization;
- whether bytes or words will be transferred;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer, and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

$\overline{\text{B}}$/W: Byte/Word (0/1) Transfers.

ST/$\overline{\text{STOP}}$: Start/Stop (1/0) Channel.

CHG/$\overline{\text{NOCHG}}$: Change/Do not change (1/0) ST/$\overline{\text{STOP}}$ bit. If this bit is set when writing to the control word, the ST/$\overline{\text{STOP}}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{\text{STOP}}$ bit will

Fig. 17 – DMA UNIT BLOCK DIAGRAM

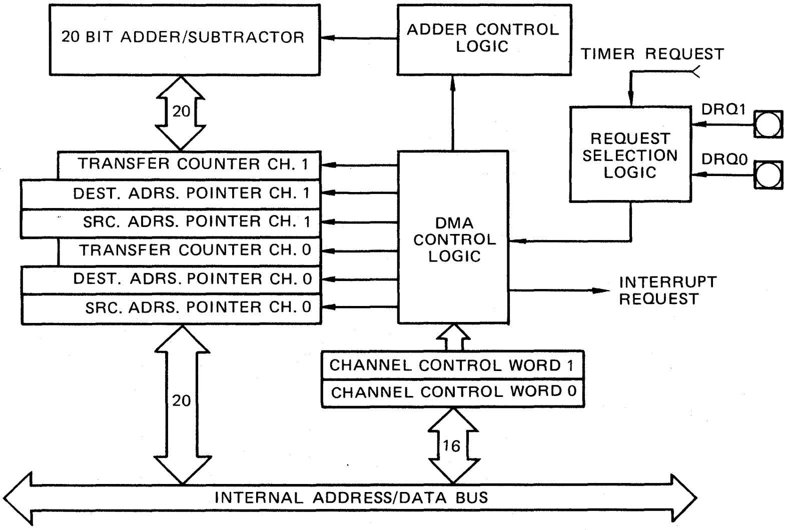


Fig. 18 – DMA CONTROL REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M/$\overline{\text{IO}}$	DESTINATION DEC	INC	M/$\overline{\text{IO}}$	SOURCE DEC	INC	TC	INT	SYN		P	TDRQ	X	CHG/$\overline{\text{NOCHG}}$	ST/$\overline{\text{STOP}}$	$\overline{\text{B}}$/W

X = DON'T CARE.

not be altered. This bit is not stored; it will always be a 0 on read.

INT: Enable Interrupts to CPU on Transfer Count termination.

TC: If set, DMA will terminate when the contents of the Transfer Count register reach zero. The ST/$\overline{\text{STOP}}$ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN: (2 bits)
00 No synchronization.
NOTE: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.
01 Source synchronization.
10 Destination synchronization.
11 Unused.

SOURCE: INC Increment source pointer by 1 or 2 (depends on $\overline{\text{B}}$/W) after each transfer.

M/$\overline{\text{IO}}$ Source pointer is in M/IO space (1/0).

DEC Decrement source pointer by 1 or 2 (depends on $\overline{\text{B}}$/W) after each transfer.

DEST: INC Increment destination pointer by 1 or 2 ($\overline{\text{B}}$/W) after each transfer.

M/$\overline{\text{IO}}$ Destination pointer is in M/IO space (1/0).

DEC Decrement destination pointer by 1 or 2 (depending on $\overline{\text{B}}$/W) after each transfer.

P: Channel priority – relative to other channel.
0 low priority.
1 high priority.
Channels will alternate cycles if both set at same priority level.

TDRQ: 0: Disable DMA requests from timer 2.
1: Enable DMA requests from timer 2.

Bit 3: Bit 3 is not used.

If both INC and DEC are specified for the same pointer, the pointer will remain constant after each cycle.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Fig. 18a). These pointers may be individually incremented or decremented

Fig. 18a – DMA MEMORY POINTER REGISTER FORMAT

HIGHER REGISTER ADDRESS	XXX	XXX	XXX	A19–A16
LOWER REGISTER ADDRESS	A15–A12	A11–A8	A7–A4	A3–A0
	15			

XXX = DON'T CARE

after each transfer. If word transfers are performed, the pointer is incremented or decremented by two. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers. Higher transfer rates can be obtained if all word transfers are performed to even addresses, since this will allow data to be accessed in a single memory access.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or unsynchronized transfers are programmed, however, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). No prefetching occurs when destination synchronization is performed, however. Data will not be fetched from the source address until the destination device signals that it is ready to receive it. When destination synchronized transfers are requested, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another DMA cycle will begin after two processor clocks. This is done to allow the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. These lead to the maximum DMA transfer rates shown in Table 14.

Table 14 – MAXIMUM DMA TRANSFER RATES

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	2MBytes/sec	2MBytes/sec
Source Synch	2MBytes/sec	2MBytes/sec
Destination Synch	1.3MBytes/sec	1.5MBytes/sec

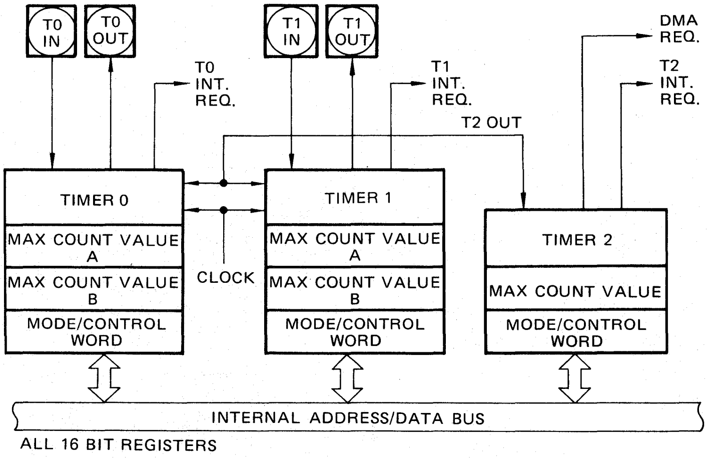
DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed such that one

Fig. 19 – TIMER BLOCK DIAGRAM



channel is always given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses the odd memory locations; however, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/$\overline{\text{STOP}}$ bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also have been generated. Therefore, the source and destination transfer pointers, and the transfer count register (if used) must be programmed before this bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/$\overline{\text{NOCHG}}$ bit is cleared when the control register is written, the ST/$\overline{\text{STOP}}$ bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- The Start/Stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

TIMERS

The MBL 80186 provides three internal 16-bit programmable timers (see Fig. 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

Timer Operation

The timers are controlled by 11 16-bit registers in the internal peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values programmed by the user. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 1 clock after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input. Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

Fig. 20 – TIMER MODE/CONTROL REGISTER

15	14	13	12	11		5	4	3	2	1	0
EN	$\overline{\text{INH}}$	INT	RIU	0	.....	MC	RTG	P	EXT	ALT	CONT

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Fig. 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15 – TIMER CONTROL BLOCK FORMAT

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

ALT:

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT:

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

EXT:

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the MBL 80186 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

P:

The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG:

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the MBL 80186 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN:

The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH:

The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:
When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller.)

MC:
The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts. Programmer intervention is required to clear this bit.

RIU:
The Register in Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. The condition which causes a timer to reset is equivalent between the current count value and the max count being used. This means that if the count is changed to be above the max count value, or if the max count value is changed to be below the current value, the timer will not reset to zero, but rather will count to its maximum value, "wrap around" to zero, then count until the max count is reached.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- All SEL (Select) bits are reset to zero. This selects MAX COUNT register A, resulting in the Timer Out pins going HIGH upon RESET.

INTERRUPT CONTROLLER

The MBL 80186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The MBL 80186 interrupt controller has its own control registers that set the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Fig. 21.

The interrupt controller has a special iRMX 86 compatibility mode that allows the use of the MBL 80186 within the iRMX 86 operating system interrupt structure. The controller is set in this mode by setting bit 14 in the peripheral control block relocation register (see iRMX 86 Compatibility Mode section). In this mode, the internal MBL 80186 interrupt controller functions as a "slave" controller to an external "master" controller. Special initialization software must be included to properly set up the MBL 80186 interrupt controller in iRMX 86 mode.

MASTER MODE OPERATION

Interrupt Controller External Interface

For external interrupt sources, five dedicated pins are provided. One of these pins is dedicated to NMI, non-maskable interrupt. This is typically used for power-fail interrupts, etc. The other four pins may function either as four interrupt input lines with internally generated interrupt vectors, as an interrupt line and an interrupt acknowledge line (called the "cascade mode") along with two other input lines with internally generated interrupt vectors, or as two interrupt input lines and two dedicated interrupt acknowledge output lines. When the interrupt lines are configured in cascade mode, the MBL 80186 interrupt controller will not generate internal interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the MBL 80186 on the second cycle. The capability to interface to external MBL 8259A programmable interrupt controllers is thus provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the MBL 8259A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

- **Fully Nested Mode**

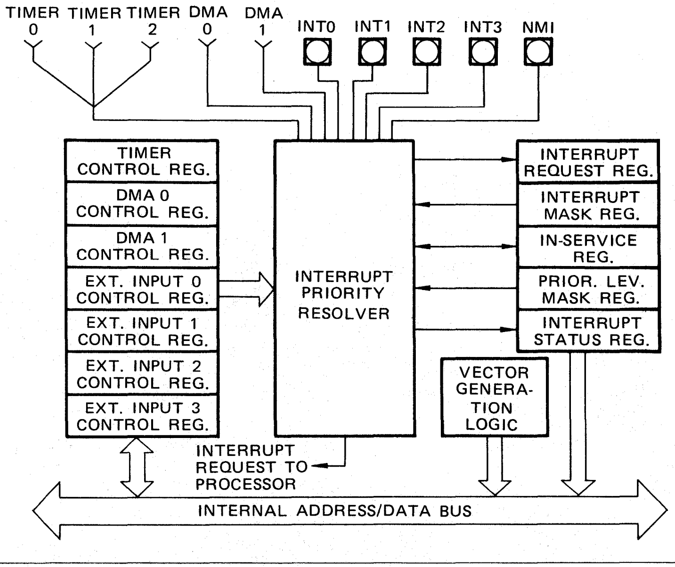
When in the fully nested mode four pins are used as direct interrupt requests. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled without being themselves interrupted by lower-priority interrupts. Since interrupts are enabled, higher-priority interrupts will be serviced.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is issued at the end of the service routine just before the issuance of the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

- **Cascade Mode**

The MBL 80186 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding

Fig. 21 – INTERRUPT CONTROLLER BLOCK DIAGRAM



vectors are generated internally. In the cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Fig. 22. INT0 is an interrupt input interfaced to a MBL 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave MBL 8259As. Three levels of priority are created, requiring priority resolution in the MBL 80186 interrupt controller, the master MBL 8259As, and the slave MBL 8259As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

- **Special Fully Nested Mode**

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external MBL 8259A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same MBL 80186 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the MBL 80186 controller until the MBL 80186 in-service bit is reset. In special fully nested mode, the MBL 80186 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority MBL 80186 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines: Software polling of the external master's IS register is required to determine if there is more than one bit set. If so, the IS bit in the MBL 80186 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Fig. 31). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest-priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The MBL 80186 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

Master Mode Features

- **Programmable Priority**

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine re-enables interrupts, it allows other requests to be serviced.

- **End-of-Interrupt Command**

The end-of-interrupt (EOI) command is used by the programmer to reset the in-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

- **Trigger Mode**

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the MBL 80186 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to reenable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

- **Interrupt Vectoring**

The MBL 80186 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Mode. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Fig. 23. It contains 15 registers. All registers can both be read or written unless specified otherwise.

- **In-Service Register**

This register can be read from or written into. The format is shown in Fig. 24. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0-I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command issued by the CPU.

- **Interrupt Request Register**

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Fig. 24. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits show exactly when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

- **Mask Register**

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Fig. 24. A one in a bit position corresponding to a particular sources serves to mask the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.
shown in Fig. 25. The code in the lower three bits of this

Fig. 22 – CASCADE MODE INTERRUPT CONNECTION

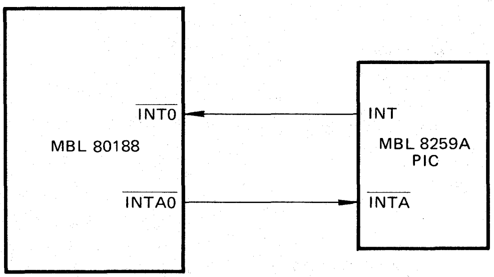


Fig. 23 – INTERRUPT CONTROLLER REGISTERS (NON-iRMX 86 MODE)

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA1 CONTROL REGISTER	36H
DMA0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

- **Priority Mask Register**

This register is used to mask all interrupts below particular interrupt priority levels. The format of this register is register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so all interrupts are unmasked.

- **Interrupt Status Register**

This register contains general interrupt controller status information. The format of this register is shown in Fig. 26. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. The purpose of this bit is to allow prompt service of all non-maskable interrupts. This bit may also be set by the CPU.

IRTx: These three bits represent the individual timer interrupt request bits. These bits are used to differentiate the timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

Fig. 24 – IN-SERVICE, INTERRUPT REQUEST, AND MASK REGISTER FORMATS

15	14		10	9	8	7	6	5	4	3	2	1	0
0	0	· · ·	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Fig. 25 – PRIORITY MASK REGISTER FORMAT

15	14		3	2	1	0
0	0	· · · · · · · · · ·	0	PRM2	PRM1	PRM0

Fig. 26 – INTERRUPT STATUS REGISTER FORMAT

15	14		7	6	5	4	3	2	1	0
DHLT	0	· · · · · ·	0	0	0	0	0	IRT2	IRT1	IRT0

- **Timer, DMA 0, 1 Control Registers**

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Fig. 27. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

- **INT0–INT3 Control Registers**

These registers are the control words for the four external input pins. Fig. 28 shows the format of the INT0 and INT1 Control registers; Fig. 29 shows the format of the INT2 and INT3 Control registers. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PR0-2: Priority programming information. Highest Priority = 000, Lowest Priority = 111

LTM: Level-trigger mode bit, 1 = level-triggered; 0 = edge-triggered. Interrupt input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = nonmask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special fully nested mode bit, 1 = SFNM

- **EOI Register**

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Fig. 30. It initiates an EOI command when written to by the MBL 80186 CPU.

The bits in the EOI register are encoded as follows:

Sx: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10. Note that to reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

Fig. 27 – TIMER/DMA CONTROL REGISTER FORMATS

15	14		4	3	2	1	0
0	0	· · · · · · · · ·	0	MSK	PR2	PR1	PR0

Fig. 28 – INT0/INT1 CONTROL REGISTER FORMATS

15	14		7	6	5	4	3	2	1	0
0	0	· · · · · ·	0	SFNM	C	LTM	MSK	PR2	PR1	PR0

Fig. 29 – INT2/INT3 CONTROL REGISTER FORMATS

15	14		5	4	3	2	1	0
0	0	· · · · · · · ·	0	LTM	MSK	PR2	PR1	PR0

NSPEC/ SPEC: A bit that determineds the type of EOI command. Nonspecific = 1, Specific = 0.

- **Poll and Poll Status Registers**

These registers contain polling information. The format of these registers is shown in Fig. 31. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

Sx. Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

iRMX 86 COMPATIBILITY MODE

This mode allows iRMX 86-80186 compatibility. The interrupt model of iRMX 86 requires one master and multiple slave MBL 8259As in cascaded fashion. When iRMX mode is used, the internal MBL 80186 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal MBL 80186 resources will be monitored through the internal interrupt controller, while the external controller functions as the system master interrupt controller.

Upon reset, the MBL 80186 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX 86 mode, bit 14 of the Relocation Register should be set.

Because of pin limitations caused by the need to interface to an external MBL 8259A master, the internal interrupt controller will no longer accept external inputs. There are however, enough MBL 80186 interrupt controller inptus (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the MBL 80186 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source. The required priority levels for the internal interrupt sources in iRMX mode are shown in Table 16.

Table 16 – INTERNAL SOURCE PRIORITY LEVEL

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA 1
4	Timer 1
5	Timer 2

These level assignments must remain fixed in the iRMX 86 mode of operation.

iRMX 86 Mode External Interface

The configuration of the MBL 80186 with respect to an external MBL 8259A master is shown in Fig. 32. The INT0 input is used as the MBL 80186 CPU interrupt input. INT3 functions as an output to send the MBL 80186 slave-interrupt-request to one of the 8 master-PIC-inputs.

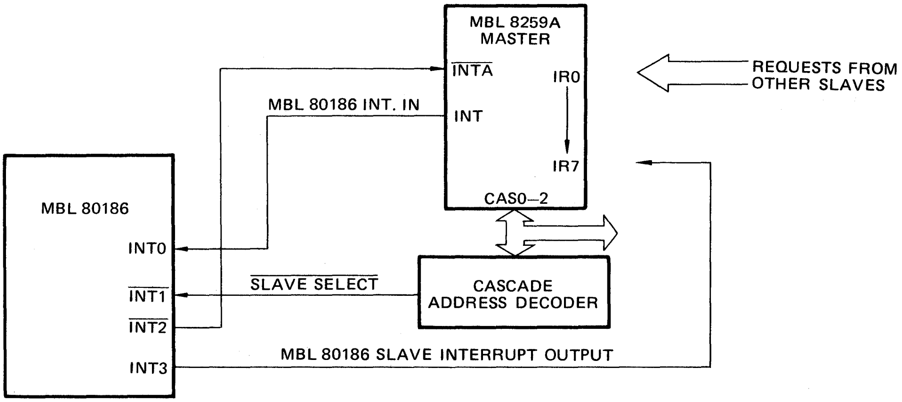
Fig. 30 – EOI REGISTER FORMAT

15	14	13		5	4	3	2	1	0
SPEC/ NSPEC	0	0	· · · · ·	0	S4	S3	S2	S1	S0

Fig. 31 – POLL REGISTER FORMAT

15	14	13		5	4	3	2	1	0
INT REQ	0	0	· · · · ·	0	S4	S3	S2	S1	S0

Fig. 32 – iRMX 86 INTERRUPT CONTROLLER INTERCONNECTION



Correct master-slave interface requires decoding of the slave addresses (CAS0-2). Slave MBL 8259As do this internally. Because of pin limitations, the MBL 80186 slave address will have to be decoded externally. $\overline{\text{INT1}}$ is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{\text{INT2}}$ is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an MBL 8259A.

Interrupt Nesting

iRMX 86 mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the iRMX 86 Mode

Vector generation in iRMX mode is exactly like that of a MBL 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic. These bits represent the encoding of the priority level requesting service. The significant five bits of the vector are programmed by writing to the interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset.The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interruput Controller Registers in the iRMX 86 Mode

All control and command registers are located inside the internal peripheral control block. Fig. 33 shows the offsets of these registers.

- **End-of-Interrupt Register**

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Fig. 34. It initiates an EOI command when written by the MBL 80186 CPU.

The bits in the EOI register are encoded as follows:

Lx: Encoded value indicating the priority of the IS bit to be reset.

- **In-Service Register**

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources.

The format for this register is shown in Fig. 35. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

● Interrupt Request Register

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Fig. 35. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

● Mask Register

This register contains a mask bit for each interrupt source. The format for this register is shown in Fig. 35. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

● Control Registers

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Fig. 36. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

PRx: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

MSK: Mask bit for the priority level indicated by PRx bits.

Fig. 33 – INTERRUPT CONTROLLER REGISTERS (iRMX MODE)

	OFFSET
LEVEL 5 CONTROL REGISTER (TIMER 2)	3AH
LEVEL 4 CONTROL REGISTER (TIMER 1)	38H
LEVEL 3 CONTROL REGISTER (DMA 1)	36H
LEVEL 2 CONTROL REGISTER (DMA 0)	34H
LEVEL 0 CONTROL REGISTER (TIMER 0)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

● Interrupt Vector Register

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Fig. 37. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

tx: 5-bit field indicating the upper five bits of the vector address.

Fig. 34 – SPECIFIC EOI REGISTER FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · · ·	0	0	0	0	0	0	L2	L1	L0

Fig. 35 – IN-SERVICE, INTERRUPT REQUEST, AND MASK REGISTER FORMATS

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · · ·	0	0	0	TMR2	TMR1	D1	D0	0	TMR0

- **Priority-Level Mask Register**

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

mx: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

- **Interrupt Status Register**

This register is defined exactly as in Non-iRMX Mode. (See Fig. 26.)

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

Fig. 36 – CONTROL WORD FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · · ·	0	0	0	0	0	MSK	PR2	PR1	PR0

Fig. 37 – INTERRUPT VECTOR REGISTER FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · · ·	0	t4	t3	t2	t1	t0	0	0	0

Fig. 38 – PRIORITY LEVEL MASK REGISTER FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · · ·	0	0	0	0	0	0	m2	m1	m0

Fig. 39 – TYPICAL MBL 80186 COMPUTER

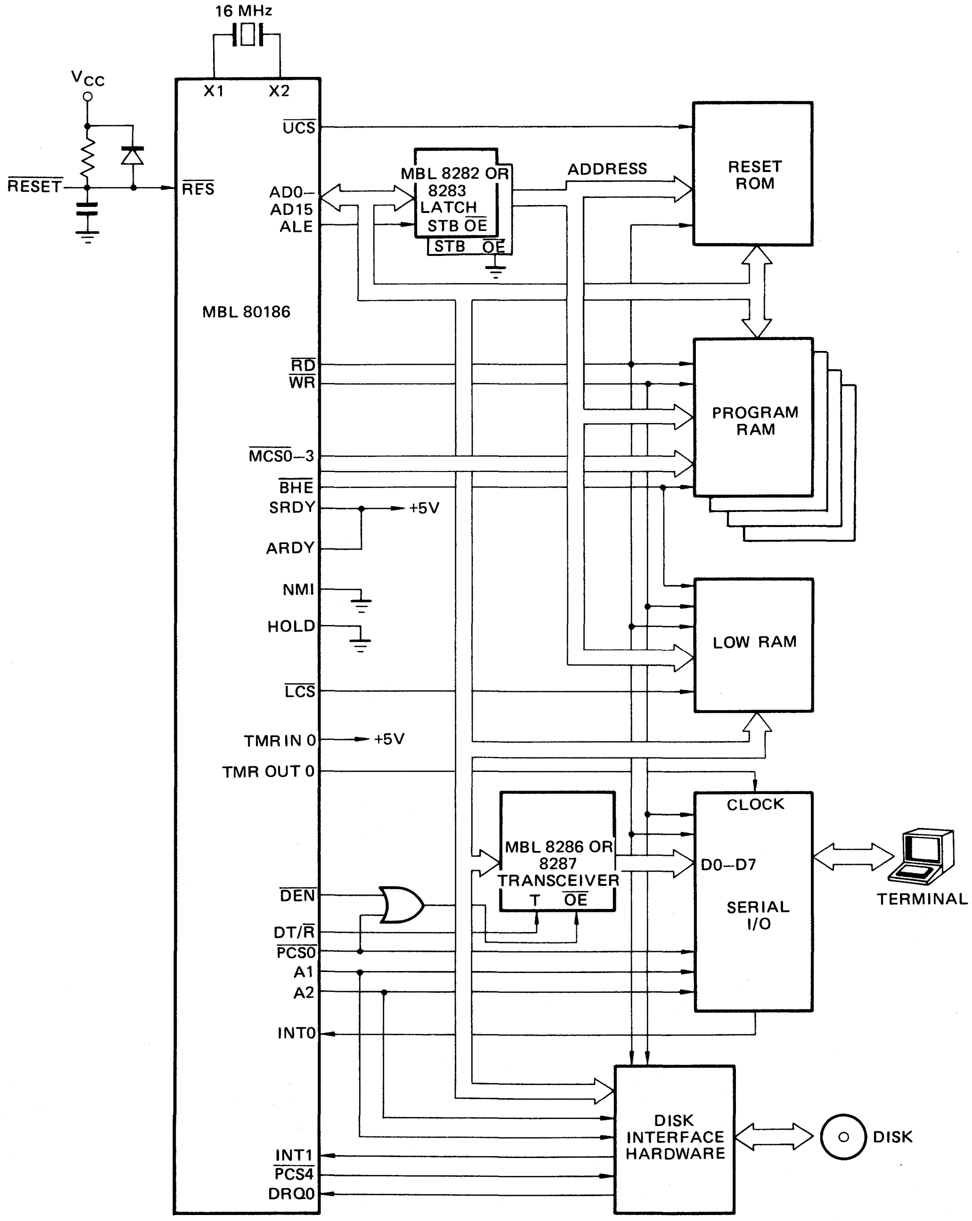
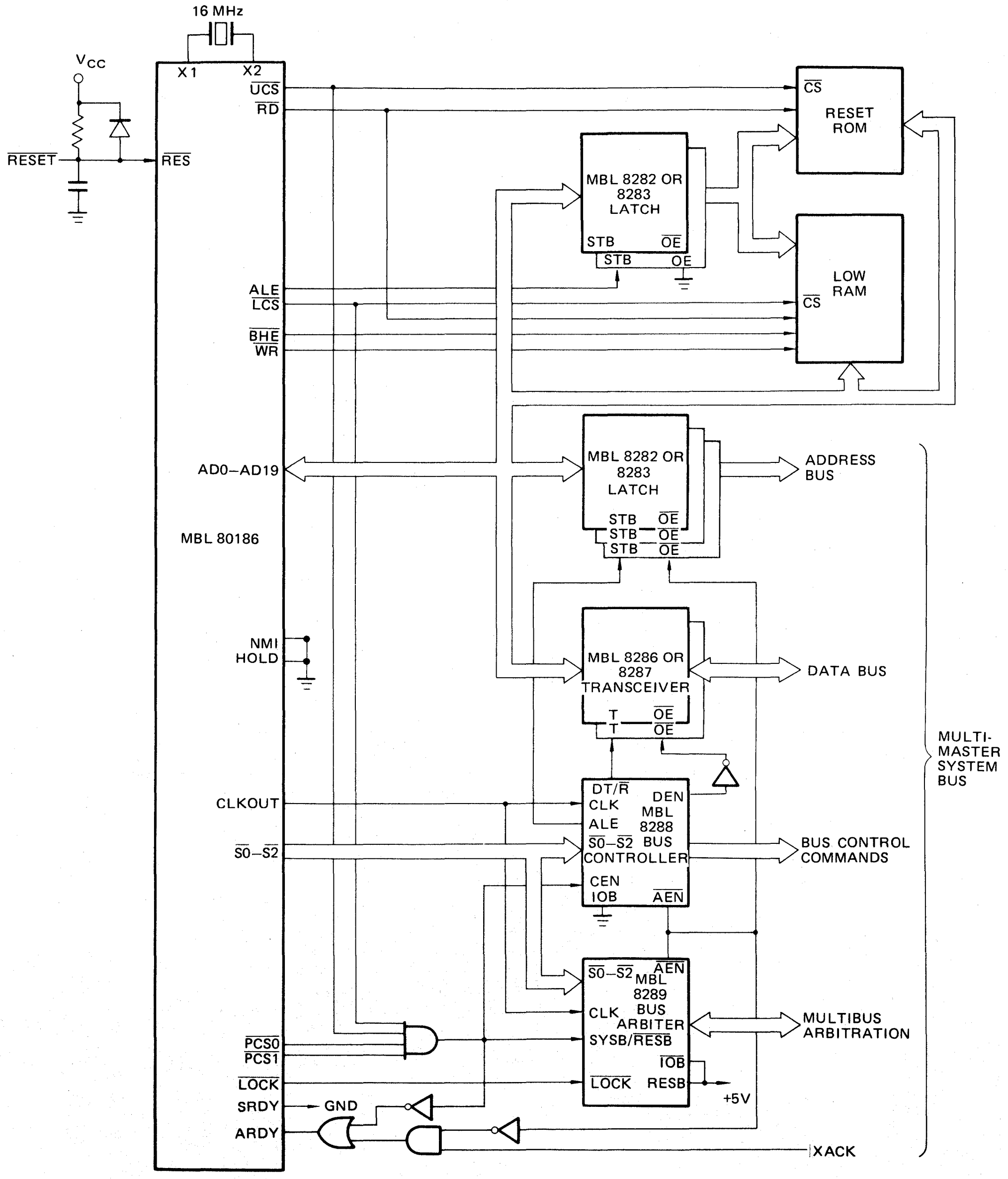


Fig. 40 – TYPICAL MBL 80186 MULTI-MASTER BUS INTERFACE



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias . . . . 0°C to 70°C
Storage Temperature . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . −1.0V to +7V
Power Dissipation . . . . 3 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0° to 70°C)

Applicable to MBL 80186 (8 MHz) and MBL 80186-6 (6 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	0.5	+0.8	V	
V_{IH}	Input High Voltage (All except X1 and ($\overline{RES}$))	2.0	V_{CC}+0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA for $\overline{S0}$-$\overline{S2}$ I_{OL} = 2.0 mA for all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		550 450	mA	Max measured at T_A = 0°C T_A = 70°C
I_{LI}	Input Leakage Current		±10	μA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V < V_{OUT} < V_{CC}
V_{CLI}	Clock Input Low Voltage	−0.5	0.6	V	
V_{CHI}	Clock Input High Voltage	3.9	V_{CC}+1.0	V	
V_{CLO}	Clock Output Low Voltage		0.6	V	I_{OL} = 4.0 mA
V_{CHO}	Clock Output High Voltage	4.0		V	I_{OH} = −200 μA
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

A.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0° to 70°C)

MBL 80186 Timing Requirements All timings Measured At 1.5 Volts Unless Otherwise Noted.
Applicable to MBL 80186 (8 MHz) and MBL 80186-6 (6 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TDVCL	Data in Setup Time (A/D)	20		ns	
TCLDX	Data in Hold Time (A/D)	10		ns	
TARYHCH	Asynchronous Ready (AREADY) Active Setup Time	20		ns	
TARYLCL	AREADY Inactive Setup Time	35		ns	
TCHARYX	AREADY Hold Time	15		ns	
TARYCHL	Asynchronous Ready Inactive Hold Time	15		ns	
TSRYCL	Synchronous Ready (SREADY) Transition Setup Time	20		ns	
TCLSRY	SREADY Transition Hold Time	15		ns	
THVCL	HOLD Setup Time*	25		ns	
TINVCH	INTR, NMI, $\overline{TEST}$, TIMERIN, Setup Time*	25		ns	
TINVCL	DRQ0, DRQ1, Setup Time*	25		ns	

* To guarantee recognition at next clock.

A.C. CHARACTERISTICS (Continued)

MBL 80186 Master Interface Timing Responses

Symbol	Parameter	MBL 80186 (8 MHz)		MBL 80186-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	5	55	5	63	ns	C_L=20-200 pF all outputs
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	35	TCLAX	44	ns	
TCHCZ	Command Lines Float Delay		45		56	ns	
TCHCV	Command Lines Valid Delay (after Float)		55		76	ns	
TLHLL	ALE Width	TCLCL-35		TCLCL-35		ns	
TCHLH	ALE Active Delay		35		44	ns	
TCHLL	ALE Inactive Delay		35		44	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-25		TCHCL-30		ns	
TCLDV	Data Valid Delay	10	44	10	55	ns	
TCLDOX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time after $\overline{WR}$	TCLCL-40		TCLCL-50		ns	
TCVCTV	Control Active Delay 1	10	70	10	87	ns	
TCHCTV	Control Active Delay 2	10	55	10	76	ns	
TCVCTX	Control Inactive Delay	5	55	5	76	ns	
TCVDEX	$\overline{DEN}$ Inactive Delay (Non-Write Cycle)	10	70	10	87	ns	
TAZRL	Address Float to $\overline{RD}$ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	70	10	87	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	55	10	76	ns	
TRHAV	$\overline{RD}$ Inactive to Address Active	TCLCL-40		TCLCL-50		ns	
TCLHAV	HLDA Valid Delay	5	50	5	67	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-50		2TCLCL-50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL-40		2TCLCL-40		ns	
TAVAL	Address Valid to ALE Low	TCLCH-25		TCLCH-45		ns	
TCHSV	Status Active Delay	10	55	10	76	ns	
TCLSH	Status Inactive Delay	10	65	10	76	ns	
TCLTMV	Timer Output Delay		60		75	ns	100 pF max
TCLRO	Reset Delay		60		75	ns	
TCHQSV	Queue Status Dealy		35		44	ns	
TCHDX	Status Hold Time	10		10		ns	
TAVCH	Address Valid to Clock High	10		10		ns	

MBL 80186 Chip-Select Timing Responses

Symbol	Parameter	MBL 80186 (8 MHz)		MBL 80186-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLCSV	Chip-Select Active Delay		66		80	ns	
TCXCSX	Chip-Select Hold Time from Command Inactive	35		35		ns	
TCHCSX	Chip-Select Inactive Delay	5	35	5	47	ns	

A.C. CHARACTERISTICS (Continued)

MBL 80186 CLKIN Timing Requirements

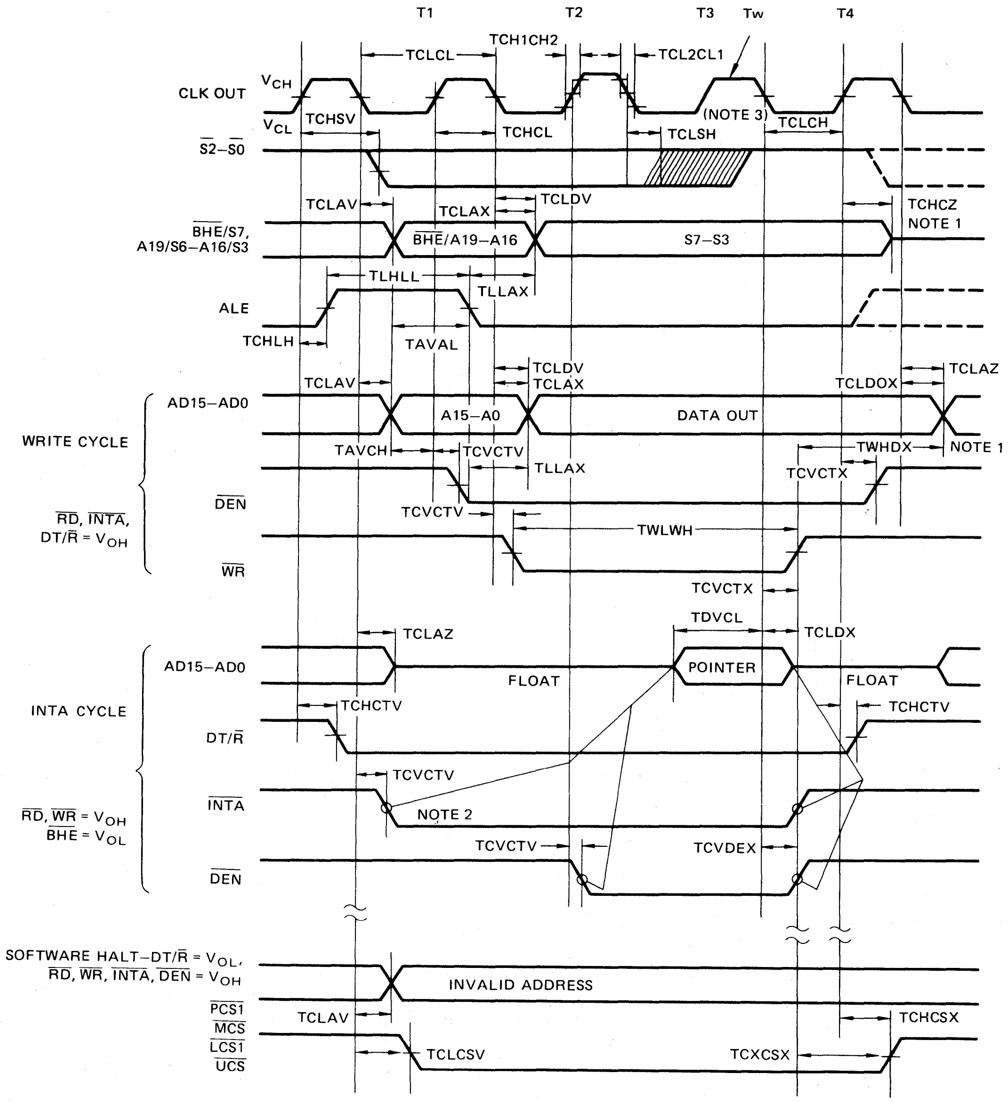
Symbol	Parameter	MBL 80186 (8 MHz)		MBL 80186-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCKIN	CLKIN Period	62.5	250	83	250	ns	
TCKHL	CLKIN Fall Time		10		10	ns	3.5 V to 1.0 V
TCKLH	CLKIN Rise Time		10		10	ns	1.0 V to 3.5 V
TCLCK	CLKIN Low Time	25		33		ns	1.5 V
TCHCK	CLKIN High Time	25		33		ns	1.5 V

MBL 80186 CLKOUT Timing Responses (200 pF load)

Symbol	Parameter	MBL 80186 (8 MHz)		MBL 80186-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCICO	CLKIN to CLKOUT Skew		50		62.5	ns	
TCLCL	CLKOUT Period	125	500	167	500	ns	
TCLCH	CLKOUT Low Time	½TCLCL-7.5		½TCLCL-7.5		ns	1.5 V
TCHCL	CLKOUT High Time	½TCLCL-7.5		½TCLCL-7.5		ns	1.5 V
TCH1CH2	CLKOUT Rise Time		15		15	ns	1.0 V to 3.5 V
TCL2CL1	CLKOUT Fall Time		15		15	ns	3.5 V to 1.0 V

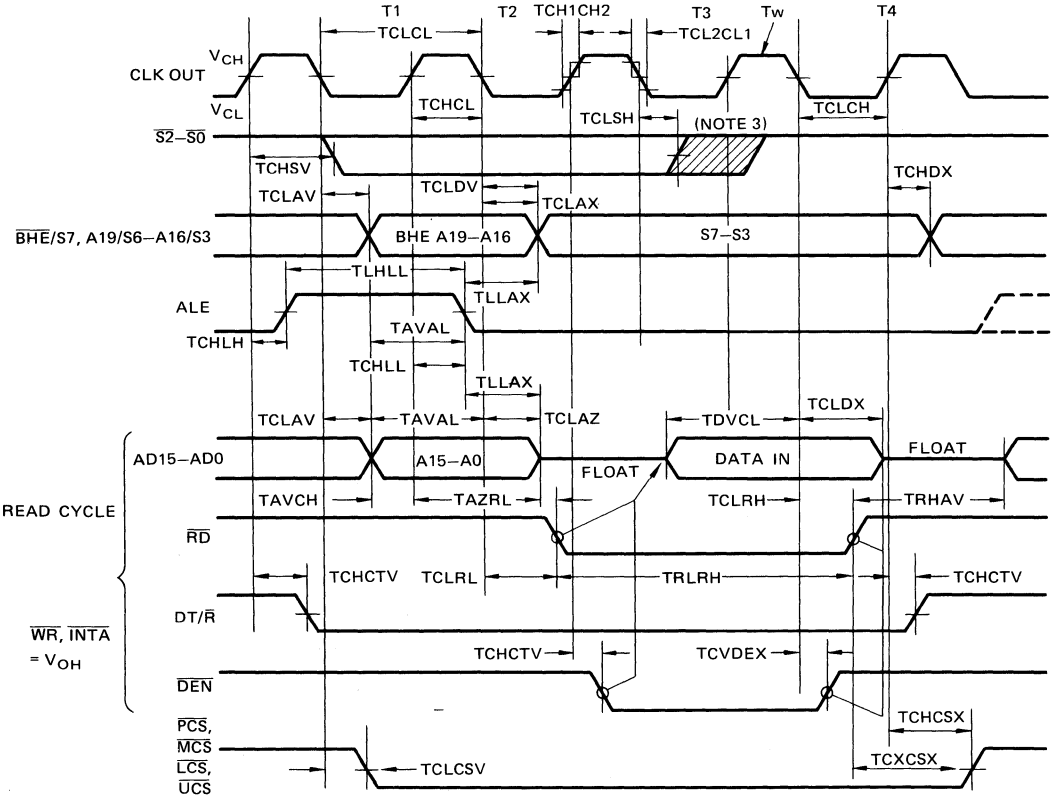
WAVEFORMS

MAJOR CYCLE TIMING



WAVEFORMS (Continued)

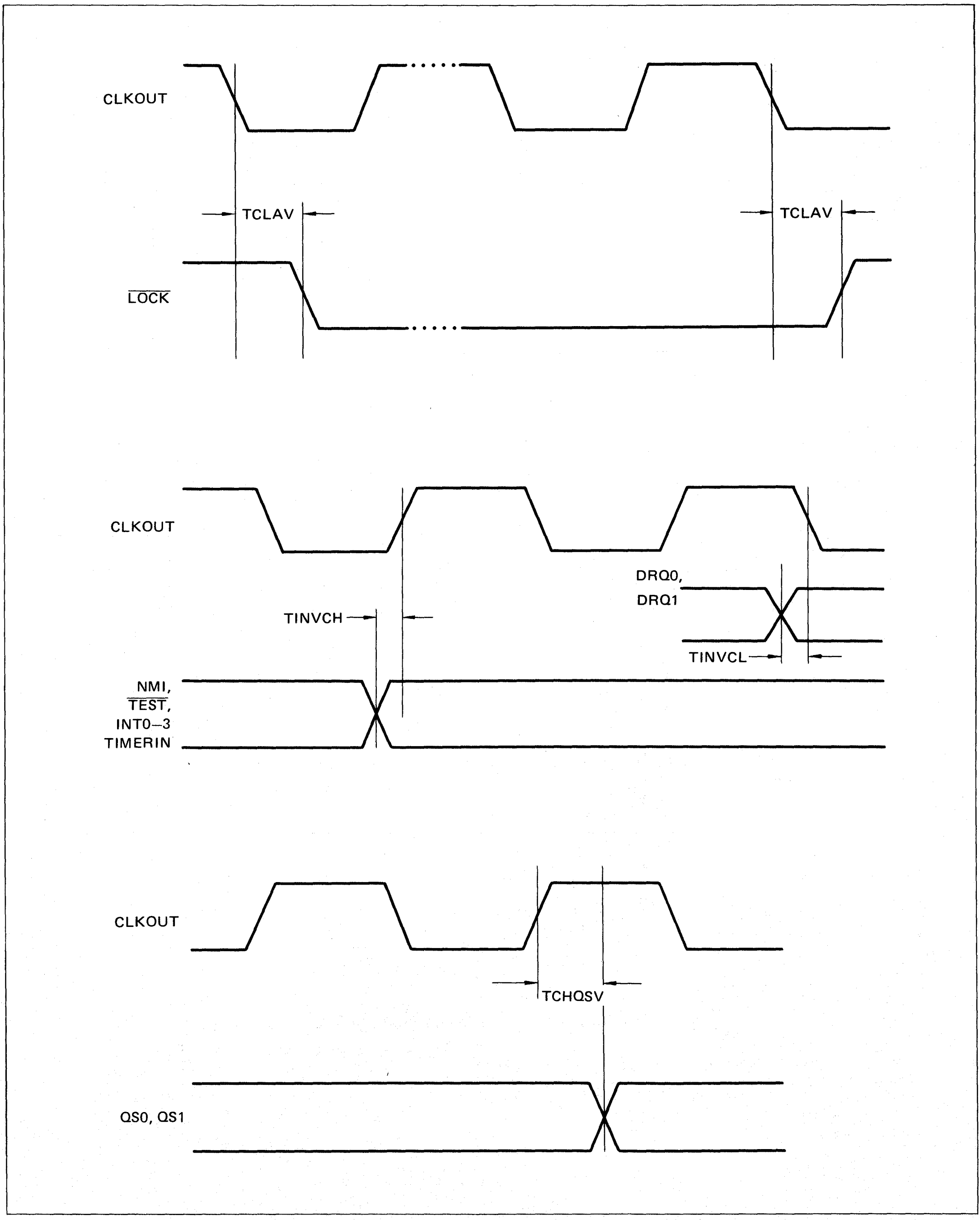
MAJOR CYCLE TIMING (Continued)



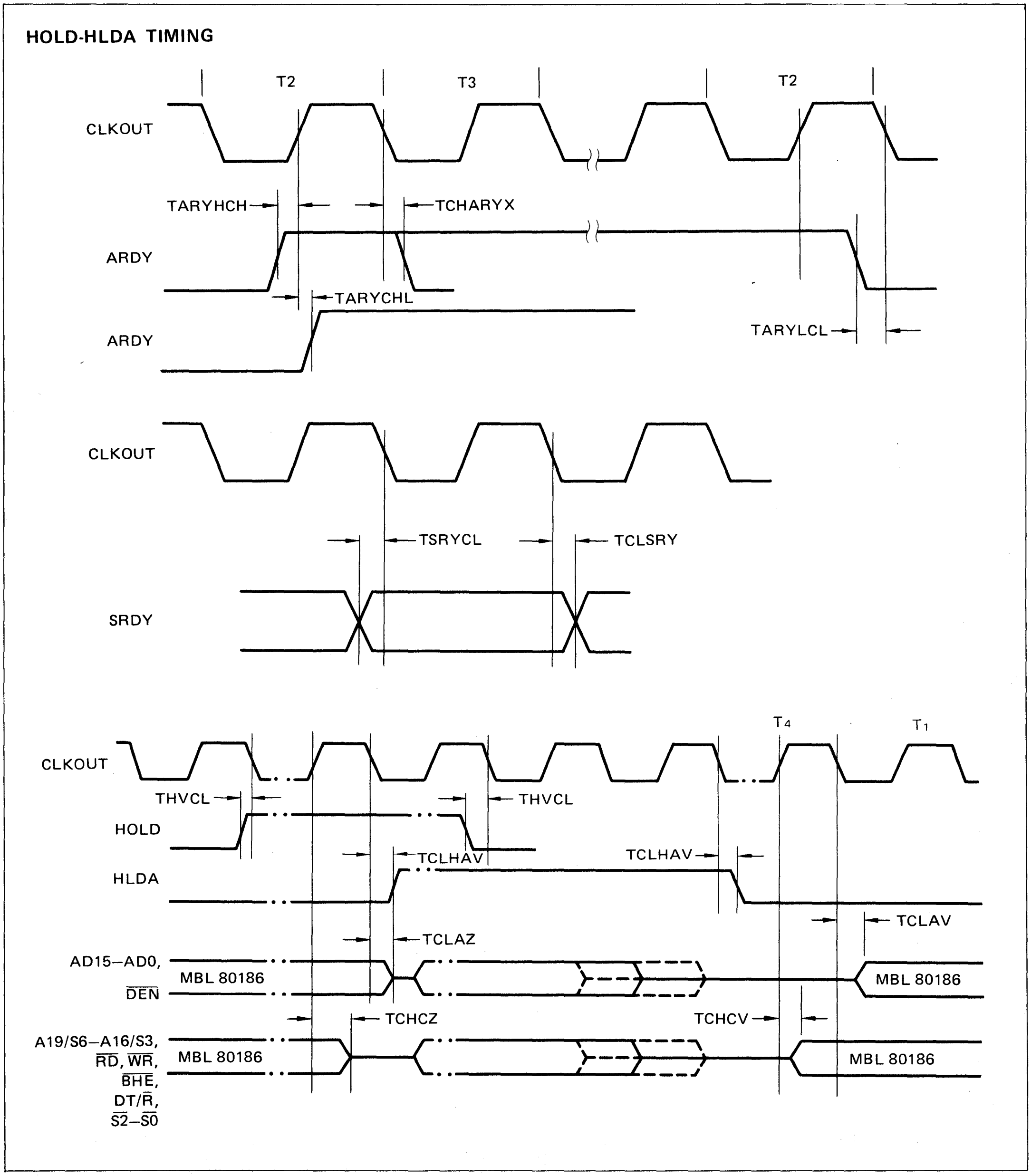
NOTES:

1. Following a Write cycle, the Local Bus is floated by the MBL 80186 only when the MBL 80186 enters a "Hold Acknowledge" state.
2. INTA occurs one clock later in iRMX-mode
3. Status inactive just prior to T4.

WAVEFORMS (Continued)

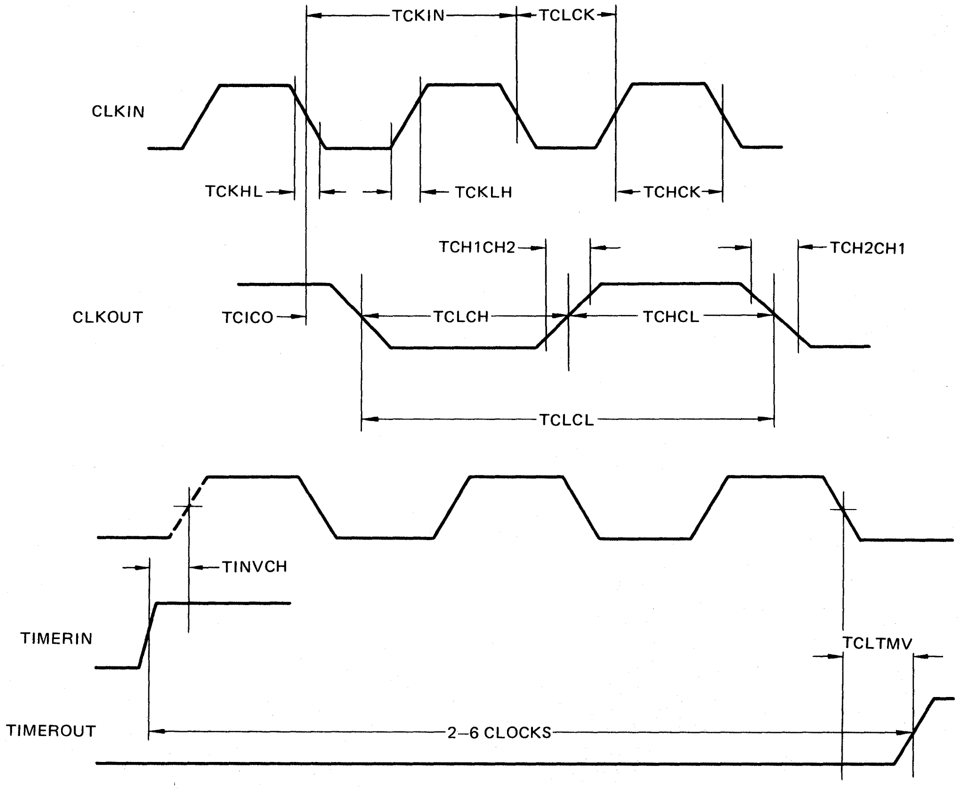


WAVEFORMS (Continued)



WAVEFORMS (Continued)

TIMER ON MBL 80186



MBL 80186 INSTRUCTION TIMINGS

The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDS occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory reference can require one (and in some cases, two) additional clocks above the minimum timings shown. This is due to the asynchronous nature of the handshake between the BIU and the Execution unit.

INSTRUCTION SET SUMMARY

FUNCTION	FORMAT				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to register/memory	1 0 0 0 1 0 0 w	mod reg r/m			2/12	
Register/memory to register	1 0 0 0 1 0 1 w	mod reg r/m			2/9	
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 000 r/m	data	data if w = 1	12–13	8/16-bit
Immediate to register	1 0 1 1 w reg	data	data if w = 1		3–4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high		9	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high		8	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m			2/9	
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	1 1 1 1 1 1 1 1	mod 110 r/m			16	
Register	0 1 0 1 0 reg				10	
Segment register	0 0 0 reg 1 1 0				9	
Immediate	0 1 1 0 1 0 s 0	data	data if s = 0		10	
PUSHA = Push All	0 1 1 0 0 0 0 0				36	
POP = Pop:						
Memory	1 0 0 0 1 1 1 1	mod 000 r/m			20	
Register	0 1 0 1 1 reg				10	
Segment register	0 0 0 reg 1 1 1	(reg ≠ 01)			8	
POPA = Pop All	0 1 1 0 0 0 0 1				51	
XCHG = Exchange:						
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m			4/17	
Register with accumulator	1 0 0 1 0 reg				3	
IN = Input from:						
Fixed port	1 1 1 0 0 1 0 w	port			10	
Variable port	1 1 1 0 1 1 0 w				8	
OUT = Output to:						
Fixed port	1 1 1 0 0 1 1 w	port			9	
Variable port	1 1 1 0 1 1 1 w				7	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1				11	
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m			6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m	(mod ≠ 11)		18	
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m	(mod ≠ 11)		18	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1				2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0				3	
PUSHF = Push flags	1 0 0 1 1 1 0 0				9	
POPF = Pop flags	1 0 0 1 1 1 0 1				8	
SEGMENT = Segment Override:						
CS	0 0 1 0 1 1 1 0				2	
SS	0 0 1 1 0 1 1 0				2	
DS	0 0 1 1 1 1 1 0				2	
ES	0 0 1 0 0 1 1 0				2	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
ARTHMETIC						
ADD = Add:						
Reg/memory with register to either	0 0 0 0 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 s w	mode 000 r/m	data	data if s w = 01	4/16	
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w = 1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	0 0 0 1 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 s w	mod 010 r/m	data	data if s w = 01	4/16	
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
INC = Increment:						
Register/memory	1 1 1 1 1 1 1 w	mod 000 r/m			3/15	
Register	0 1 0 0 0 reg				3	
SUB = Subtract:						
Reg/memory and register to either	0 0 1 0 1 0 d w	mod reg r/m			3/10	
Immediate from register/memory	1 0 0 0 0 0 s w	mod 101 r/m	data	data if s w = 01	4/16	
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w = 1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	0 0 0 1 1 0 d w	mod reg r/m			3/10	
Immediate from register/memory	1 0 0 0 0 0 s w	mod 011 r/m	data	data if s w = 01	4/16	
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w = 1		3/4	8/16-bit
DEC = Decrement:						
Register/memory	1 1 1 1 1 1 1 w	mod 001 r/m			3/15	
Register	0 1 0 0 1 reg				3	
CMP = Compare:						
Register/memory with register	0 0 1 1 1 0 1 w	mod reg r/m			3/10	
Register with register/memory	0 0 1 1 1 0 0 w	mod reg r/m			3/10	
Immediate with register/memory	1 0 0 0 0 0 s w	mod 111 r/m	data	data if s w = 01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w = 1		3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w	mod 011 r/m			3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1				8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1				4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1				7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1				4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w	mod 101 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43	
IMUL = Integer Immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s = 0	22–25/ 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 110 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
ARITHMETIC (Continued)						
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 111 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	
LOGIC						
Shift/Rotate instructions:						
Register/memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15	
Register/memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n	
Register/memory by count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n	
		TTT Instruction				
		0 0 0 ROL				
		0 0 1 ROR				
		0 1 0 RCL				
		0 1 1 RCR				
		1 0 0 SHL/SAL				
		1 0 1 SHR				
		1 1 1 SAR				
AND = And:						
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 100 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1		3/4	8/16-bit
TEST = And function to flags, no result:						
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 000 r/m	data	data if w = 1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 001 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 110 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	mod 010 r/m			3	
STRING MANIPULATION						
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w				22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12	
STOS = Stor byte/wd from AL/A	1 0 1 0 1 0 1 w				10	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w				14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
STRING MANIPULATION (Continued):						
Repeated by count in CX						
MOVS = Move string	11110010	1010010w			8 + 8n	
CMPS = Compare string	1111001z	1010011w			5 + 22n	
SCAS = Scan string	1111001z	1010111w			5 + 15n	
LODS = Load string	11110010	1010110w			6 + 11n	
STOS = Store string	11110010	1010101w			6 + 9n	
INS = Input string	11110010	0110110w			8 + 8n	
OUTS = Output string	11110010	0110111w			8 + 8n	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		15	
Register/memory indirect within segment	11111111	mod 010 r/m			13/19	
Direct intersegment	10011010	segment offset			23	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m		(mod ≠ 11)	38	
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/17	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m		(mod ≠ 11)	26	
RET = Return from CALL:						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
CONTROL TRANSFER (Continued):						
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp			4/13	
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp			4/13	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp			4/13	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp			4/13	
JO = Jump on overflow	0 1 1 1 0 0 0 0	disp			4/13	
JS = Jump on sign	0 1 1 1 1 0 0 0	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp			4/13	
JNB/JAE = Jump on not below/ above or equal	0 1 1 1 0 0 1 1	disp			4/13	
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp			4/13	
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1	disp			4/13	
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp			4/13	
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp			4/13	
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp			5/15	
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp			6/16	
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp			6/16	LOOP not taken/LOOP taken
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp			6/16	
ENTER = Enter Procedure	1 1 0 0 1 0 0 0	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	1 1 0 0 1 0 0 1				8	
INT = Interrupt:						
Type specified	1 1 0 0 1 1 0 1	type			47	
Type 3	1 1 0 0 1 1 0 0				45	if INT.taken/ if INT. not taken
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0				48/4	
IRET = Interrupt return	1 1 0 0 1 1 1 1				28	
BOUND = Detect value out of range	0 1 1 0 0 0 1 0	mod reg r/m			33 – 35	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{\text{test}}$ = 0
LOCK = Bus lock prefix	11110000	2	
ESC = Processor extension escape	11011TTT | mod LLL r/m	6	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

NOTE:
EA CALCULATION TIME IS 4 CLOCK CYCLES FOR ALL MODES, AND IS INCLUDED IN THE EXECUTION TIMES GIVEN WHENEVER APPROPRIATE.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

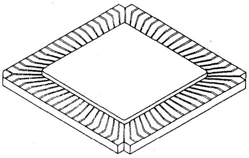
REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

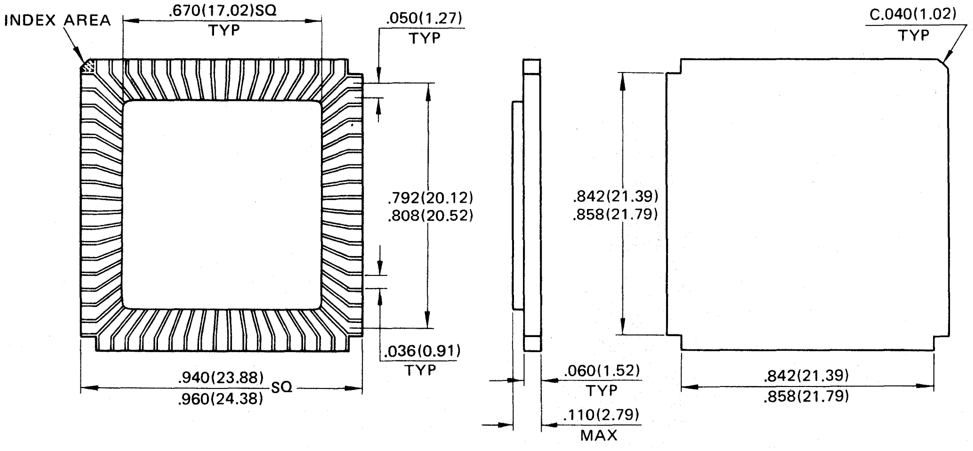
PACKAGE ILLUSTRATION

CERAMIC LCC
(METAL SEAL)



PACKAGE DIMENSIONS (Suffix -CV)

68-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-68C-A01)



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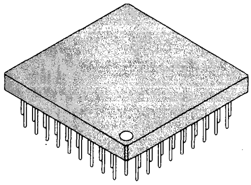
Dimensions in inches (millimeters)

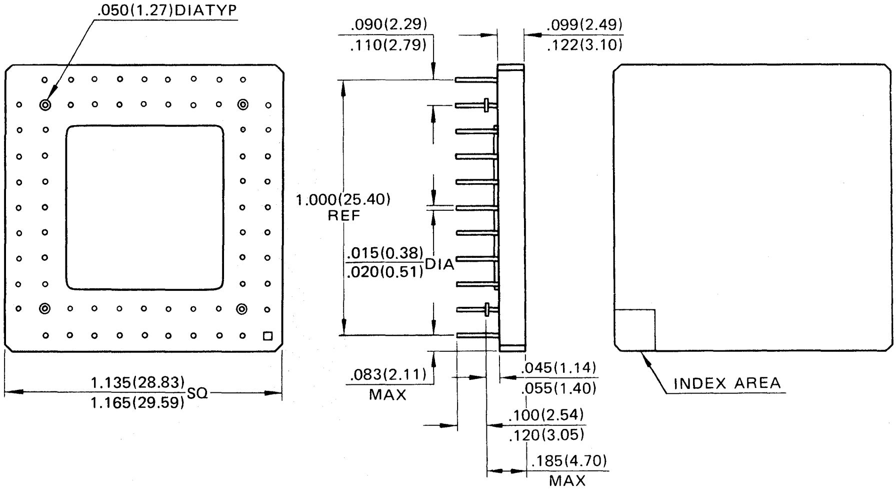
PACKAGE ILLUSTRATION

CERAMIC PGA
(METAL SEAL)



PACKAGE DIMENSION (Suffix -CR)

68-LEAD CERAMIC (METAL SEAL)
REPEATED QUAD IN-LINE PACKAGE
(CASE No.: RIT-68C-A01)



Dimensions in inches (millimeters)

FUJITSU

NMOS 16-BIT MICROPROCESSOR

MBL 8086
MBL 8086-2
MBL 8086-1

February 1985
Edition 4.0

NMOS 16-BIT MICROPROCESSOR

The Fujitsu MBL8086 high performance 16-bit CPU is available in three clock rates: 5, 8 and 10 MHz. The CPU is implemented in N-Channel, depletion load, silicon gate technology, and packaged in a 40-pin ceramic or plastic DIP. The MBL 8086 operates in both single processor and multiple processor configurations to achieve high performance levels.

- **Direct Addressing Capability of 1 MByte of Memory**
- **Architecture Designed for Powerful Assembly Language and Efficient High Level Languages.**
- **14 Word by 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Operations**
- **8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide**
- **Range of Clock Rates:**
  5 MHz for MBL 8086,
  8 MHz for MBL 8086-2,
  10 MHz for MBL 8086-1
- **MULTIBUS* System Compatible Interface**
- **40-Pin DIP:**
  Ceramic DIP (Suffix: -C)
  Plastic DIP (Suffix: -P)

Fig. 1 — BLOCK DIAGRAM

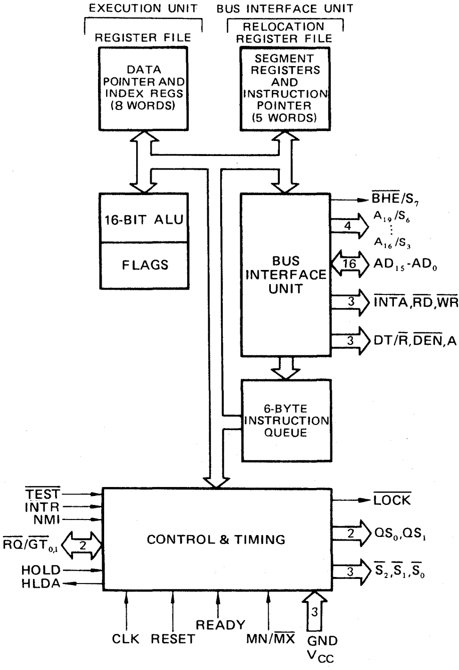


Fig. 2 — PIN CONFIGURATIONS

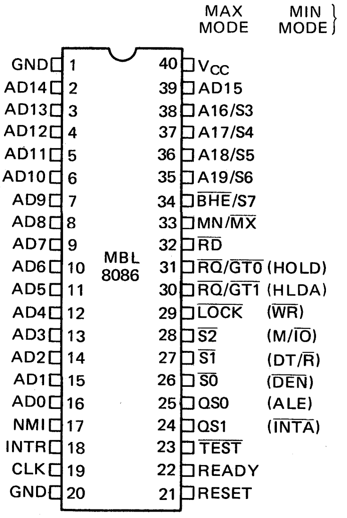


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TABLE 1 – PIN DESCRIPTION

The following pin function descriptions are for MBL 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the MBL 8086 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>AD_{15}-AD_0</td><td>2-16,39</td><td>I/O</td><td><b>Address Data Bus:</b> These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{\text{BHE}}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. (See $\overline{\text{BHE}}$.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge."</td></tr>
<tr><td>A_{19}/S_6,
A_{18}/S_5,
A_{17}/S_4,
A_{16}/S_3</td><td>35-38</td><td>O</td><td><b>Address/Status:</b> During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as shown.
This information indicates which relocation register is presently being used for data accessing.
These lines float to 3-state OFF during local bus "hold acknowledge."
<table>
<tr><th>A_{17}/S_4</th><th>A_{16}/S_3</th><th>Characteristics</th></tr>
<tr><td>0(LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1(HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S_6 is 0 (LOW)</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>$\overline{\text{BHE}}/S_7$</td><td>34</td><td>O</td><td><b>Bus High Enable/Status:</b> During T_1 the bus high enable signal ($\overline{\text{BHE}}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}-D_8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{\text{BHE}}$ to condition chip select functions. $\overline{\text{BHE}}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats of 3-state OFF in "hold." It is LOW during T_1 for the first interrupt acknowledge cycle.
<table>
<tr><th>$\overline{\text{BHE}}$</th><th>A_0</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>Whole word</td></tr>
<tr><td>0</td><td>1</td><td>Upper byte from/to odd address</td></tr>
<tr><td>1</td><td>0</td><td>Lower byte from/to even address</td></tr>
<tr><td>1</td><td>1</td><td>None</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{RD}}$</td><td>32</td><td>O</td><td><b>Read:</b> Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the MBL 8086 local bus. $\overline{\text{RD}}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the MBL 8086 local bus has floated.
This signal floats to 3-state OFF in "hold acknowledge."</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td><b>READY:</b> is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/IO is synchronized by the MBL 8284A Clock Generator to form READY. This signal is active HIGH. The MBL 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td><b>Interrupt Request:</b> is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</td></tr>
<tr><td>$\overline{\text{TEST}}$</td><td>23</td><td>I</td><td><b>$\overline{\text{TEST}}$:</b> Input is examined by the "Wait" instruction. If the $\overline{\text{TEST}}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</td></tr>
</table>

TABLE 1 — PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name and Function
NMI	17	I	**Non-maskable interrupt:** an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**Reset:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction Set description, when RESET returns LOW. RESET is internally synchrnoized.
CLK	19	I	**Clock:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** +5V power supply pin.
GND	1, 20		**Ground**
MN/$\overline{MX}$	33	I	**Minimum/Maximum:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the MBL 8086/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

<table>
<tr><td>$\overline{S_2}$,$\overline{S_1}$,$\overline{S_0}$</td><td>26-28</td><td>O</td><td><b>Status:</b> active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_W when READY is HIGH. This status is used by the MBL 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.
These signals float to 3-state OFF in "hold acknowledge." These status lines are encoded as shown.
<table>
<tr><th>$\overline{S_2}$</th><th>$\overline{S_1}$</th><th>$\overline{S_0}$</th><th>Characteristics</th></tr>
<tr><td>0(LOW)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1(HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}/\overline{GT_0}$,
$\overline{RQ}/\overline{GT_1}$</td><td>30, 31</td><td>I/O</td><td><b>Request/Grant:</b> pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 9):
1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the MBL 8086 (pulse 1).
2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the MBL 8086 to the requesting master (pulse 2), indicates that the MBL 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge."
3. A pulse 1 CLK wide from the requesting master indicates to the MBL 8086 (pulse 3) that the "hold" request is about to end and that the MBL 8086 can reclaim the local bus at the next CLK .
Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:
1. Request occurs on or before T_2.
2. Current cycle is not the low byte of a word (on an odd address).
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.</td></tr>
</table>

TABLE 1 – PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td></td><td></td><td></td><td>If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>29</td><td>O</td><td>$\overline{\text{LOCK}}$: output indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active LOW. The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge."</td></tr>
<tr><td>QS_1, QS_0</td><td>24, 25</td><td>O</td><td><b>Queue Status:</b> The queue status is valid during the CLK cycle after which the queue operation is performed.
QS_1 and QS_0 provide status to allow external tracking of the internal MBL 8086 instruction queue.
<table>
<tr><th>QS_1</th><th>QS_0</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>No Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Byte of Op Code from Queue</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Empty the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr>
</table></td></tr>
</table>

The following pin function descriptions are for the MBL 8086 in minimum mode (i.e., MN/$\overline{\text{MX}}$=V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

M/$\overline{\text{IO}}$	28	O	**Status line:** logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{\text{IO}}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M=HIGH, $\overline{\text{IO}}$=LOW). M/$\overline{\text{IO}}$ floats to 3-state OFF in local bus "hold acknowledge."
$\overline{\text{WR}}$	29	O	**Write:** indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{\text{IO}}$ signal. $\overline{\text{WR}}$ is active for T_2, T_3 and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge."
$\overline{\text{INTA}}$	24	O	$\overline{\text{INTA}}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3, and T_W of each interrupt acknowledge cycle.
ALE	25	O	**Address Latch Enable:** provided by the processor to latch the address into the MBL 8282/8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{\text{R}}$	27	O	**Data Transmit/Receive:** needed in minimum system that desires to use an MBL 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{\text{R}}$ is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/$\overline{\text{IO}}$. (T=HIGH, $\overline{\text{R}}$=LOW). This signal floats to 3-state OFF in local bus "hold acknowledge."
$\overline{\text{DEN}}$	26	O	**Date Enable:** provided as an output enable for the MBL 8286/8287 in a minimum system which uses the transceiver. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access and for $\overline{\text{INTA}}$ cycles. For a read or $\overline{\text{INTA}}$ cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{\text{DEN}}$ floats to 3-state OFF in local bus "hold acknowledge."
HOLD, HLDA	31, 30	I/O	**HOLD:** indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_4 or T_1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{\text{RQ}}/\overline{\text{GT}}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The internal functions of the MBL 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-in-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank (D_{15}-D_8) and a low bank (D_7-D_0) of 512K 8-bit bytes addressed in parallel by the processor's address lines A_{19}-A_1. Byte data with even addresses is transferred on the D_7-D_0 bus lines while odd addressed byte data (A_0 HIGH) is transferred on the D_{15}-D_8 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A_0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicity overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (see Figure 3b). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

Fig. 3a – MEMORY ORGANIZATION

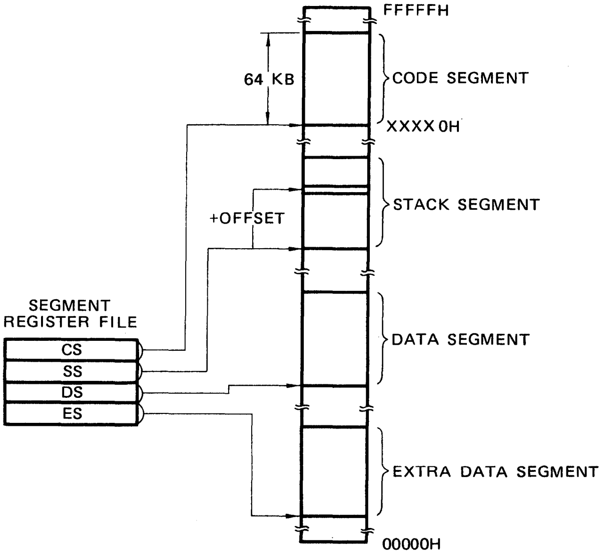
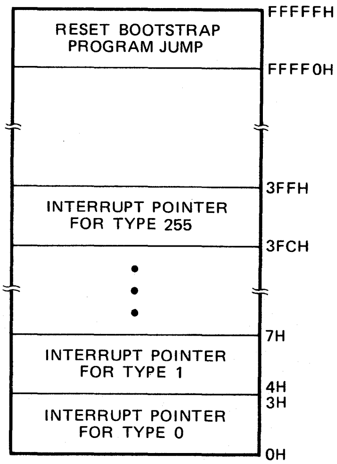


Fig. 3b – RESERVED MEMORY LOCATIONS


FFFFFH
RESET BOOTSTRAP PROGRAM JUMP
FFFF0H
3FFH
INTERRUPT POINTER FOR TYPE 255
3FCH
7H
INTERRUPT POINTER FOR TYPE 1
4H
3H
INTERRUPT POINTER FOR TYPE 0
0H

MINIMUM AND MAXIMUM MODE

The requirements for supporting minimum and maximum MBL 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the MBL 8086 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the MBL 8086 treats pins 24 through 31 in maximum mode. An MBL 8288 bus controller interprets status information coded into $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ to generate bus timing and control signals compatible with the MULTIBUS* architecture. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the MBL 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

*Trade Mark of Intel Corporation, USA

Fig. 4a – MINIMUM MODE MBL 8086 TYPICAL CONFIGURATION EXAMPLE

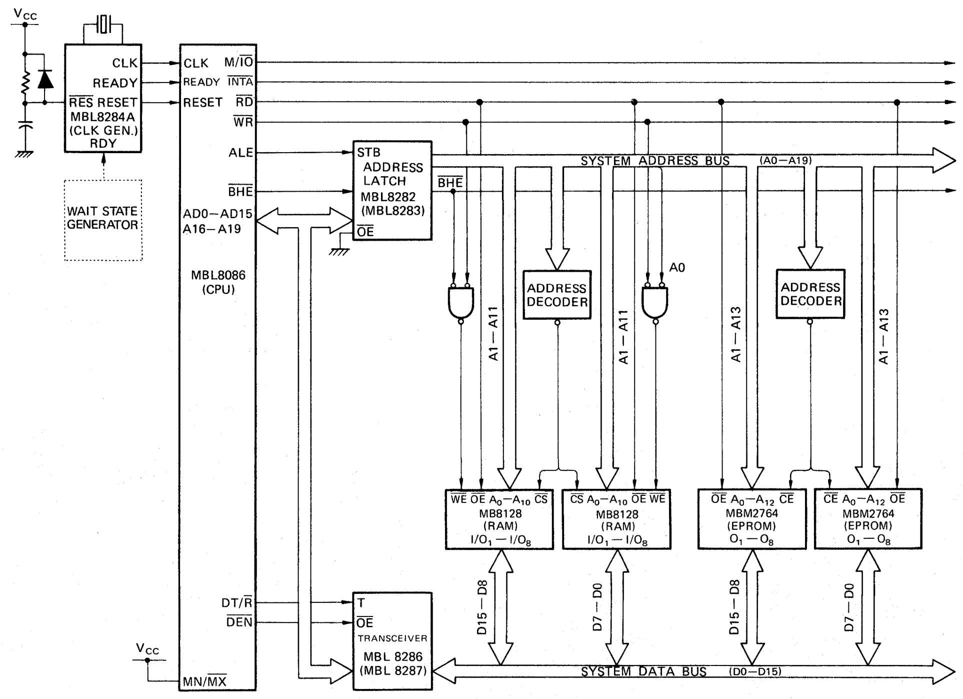
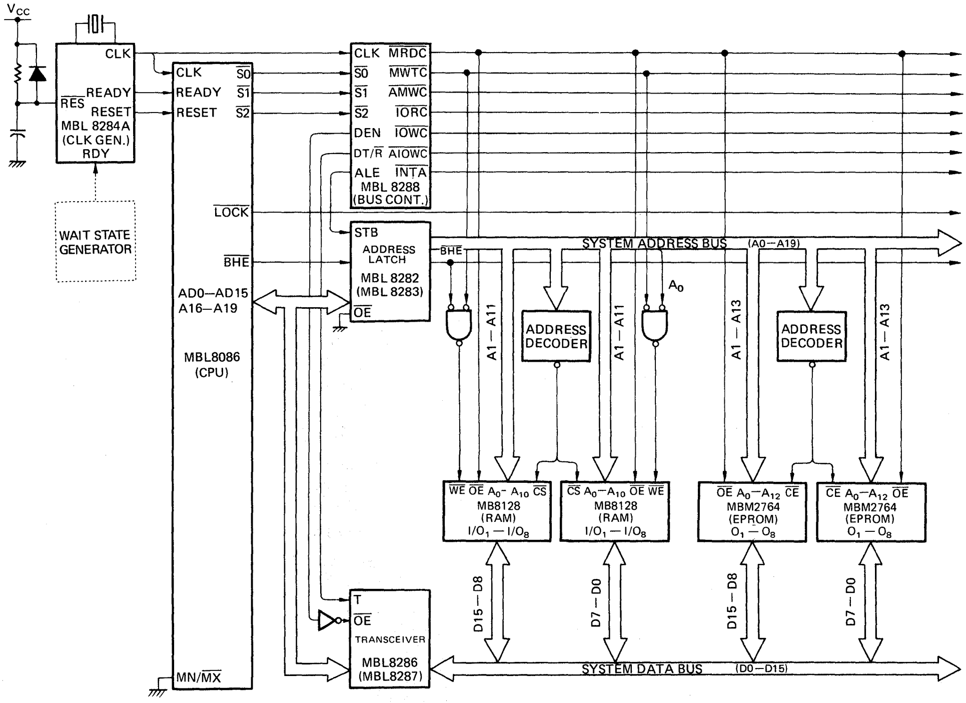


Fig. 4b – MAXIMUM MODE MBL 8086 TYPICAL CONFIGURATION EXAMPLE



BUS OPERATION

The MBL 8086 has a combined address and data bus commonly referred to as a time-multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 5). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_W) are inserted between T_3 and T_4. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between MBL 8086 bus cycles. These are referred to as "Idle" states (T_1) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the MBL 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bit S_3 through S_7 are multiplexed with high-order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle informing the address, according to the following table:

S_4	S_3	CHARACTERISTICS
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

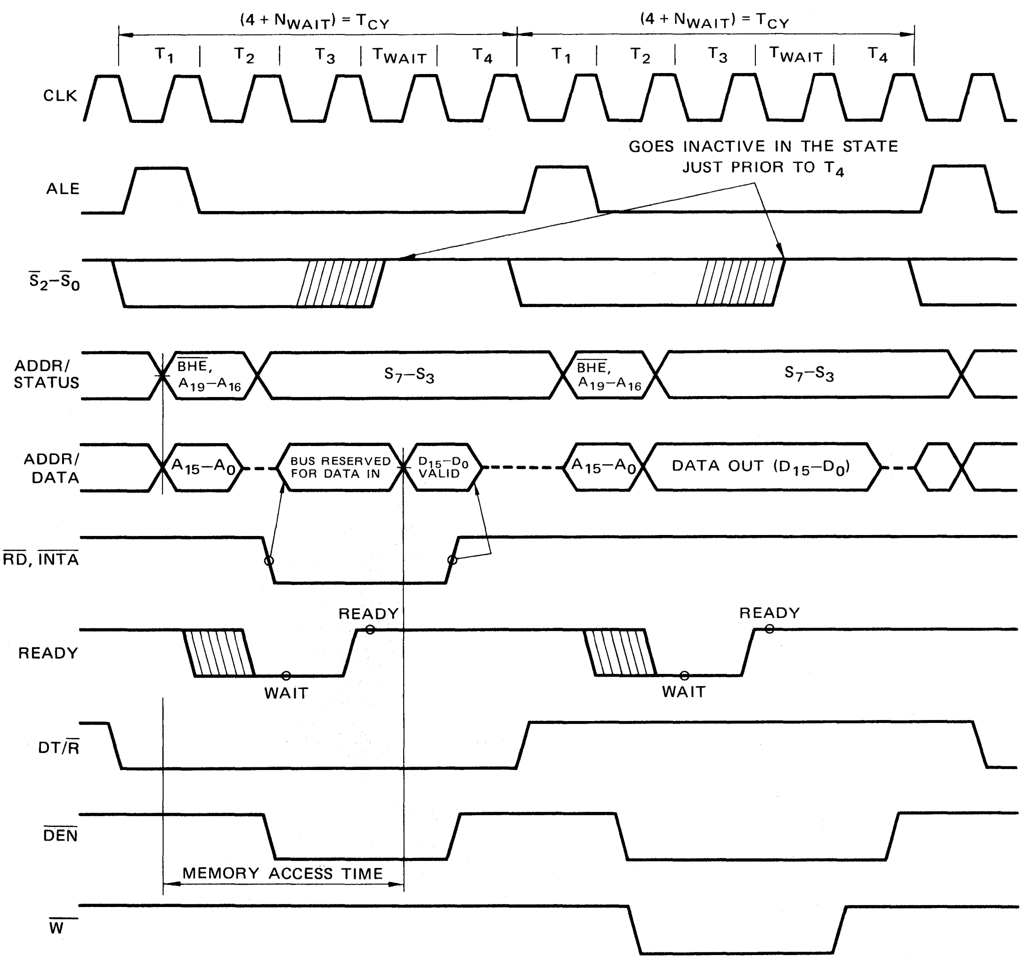
S_5 is a reflection of the PSW interrupt enable bit. $S_6 = 0$ and S_7 is a spare status bit.

I/O ADDRESSING

In the MBL 8086 I/O operations can addressed up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A_{15}-A_0. The address lines A_{19}-A_{16} are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on D_{15}-D_8. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

Fig. 5 — BASIC SYSTEM TIMING



EXTERNAL INTERFACE

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The MBL 8086 RESET is required to be HIGH for greater than 4 CLK cycles. The MBL 8086 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 10 CLK cycles. After this interval the MBL 8086 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3b). The details of this operation are specified in the Instruction Set description of the Family User's Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 μs after power-up, to allow complete initialization of the MBL 8086.

NMI may not be asserted prior to the 2nd CLK cycle following the end of RESET.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer or control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

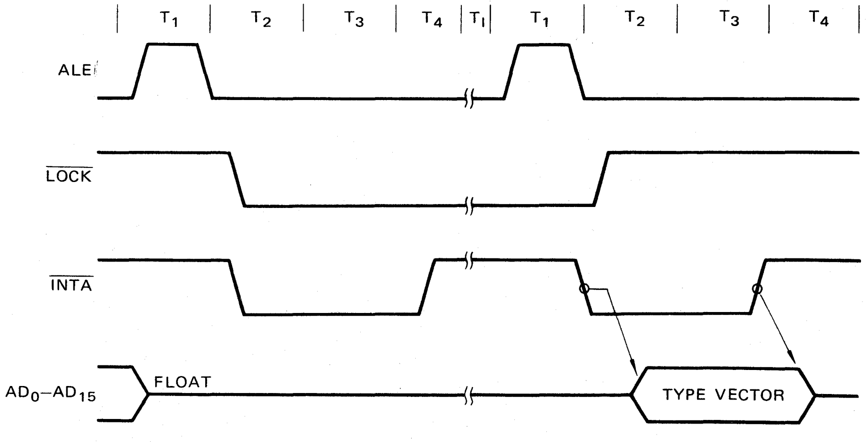
The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See instruction Set description.)

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The MBL 8086 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The

Fig. 6 — INTERRUPT ACKNOWLEDGE SEQUENCE



interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (figure 6) the processor excutes two successive (back-to-back) Interrupt acknowledge cycles. The MBL 8086 emits the $\overline{\text{LOCK}}$ signal from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external Interrupt system (e.g., MBL 8259A PIC) which idetifies the source (type) of the Interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In Maximum Mode, the processor issues appropriate HALT status on $\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$ and the MBL 8288 bus controller issues one ALE. The MBL 8086 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the MBL 8086 out of the "HALT" state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The $\overline{\text{LOCK}}$ status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{\text{LOCK}}$ signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{\text{LOCK}}$ is active a request on a $\overline{\text{RQ}}/\overline{\text{GT}}$ pin will be recorded and then honored at the end of the $\overline{\text{LOCK}}$.

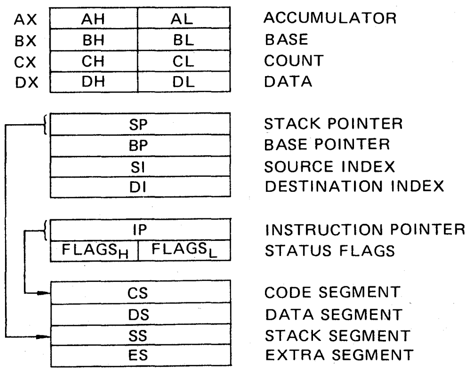
EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the MBL 8086 provides a single software-testable input known as the $\overline{\text{TEST}}$ signal. At any time the program may execute a WAIT instruction. If at that time the $\overline{\text{TEST}}$ signal is inactive (HIGH), program execution becomes suspended while the processor waits for $\overline{\text{TEST}}$ to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All MBL 8086 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-feches and re-executes the WAIT instruction upon returning from the interrupt.

BASIC SYSTEM TIMING

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/$\overline{\text{MX}}$ pin is strapped to V_{CC} and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/$\overline{\text{MX}}$ pin is strapped to V_{SS} and the processor emits coded status information which the MBL 8288 bus controller uses to generate MULTIBUS* compatible bus control signals. Figure 5 illustrates the signal timing relationships.

Fig. 7 — MBL 8086 REGISTER MODEL



AX	AH	AL	ACCUMULATOR
BX	BH	BL	BASE
CX	CH	CL	COUNT
DX	DH	DL	DATA
	SP		STACK POINTER
	BP		BASE POINTER
	SI		SOURCE INDEX
	DI		DESTINATION INDEX
	IP		INSTRUCTION POINTER
	FLAGS_H	FLAGS_L	STATUS FLAGS
	CS		CODE SEGMENT
	DS		DATA SEGMENT
	SS		STACK SEGMENT
	ES		EXTRA SEGMENT

*Trade Mark of Intel Corporation, USA

SYSTEM TIMING – MINIMUM SYSTEM

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the MBL 8282/8283 latch. The $\overline{BHE}$ and A_0 signals address the low, high, or both bytes. From T_1 to T_4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At T_2 the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (MBL 8286/8287) is required to buffer the MBL 8086 local bus, signal DT/$\overline{R}$ and $\overline{DEN}$ are provided by the MBL 8086.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In the T_2 immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of T_4. During T_2, T_3 and T_W the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for the bus to float.

The $\overline{BHE}$ and A_0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to the following table:

$\overline{BHE}$	A_0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on D_{15}-D_8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 6.) In the second of two successive INTA cycles, a byte of information is read from bus lines D_7-D_0 as supplied by the interrupt system logic (i.e., MBL 8259A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interupt vector lookup table, as described earlier.

BUS TIMING – MEDIUM SIZE SYSTEMS

For medium size systems the MN/$\overline{MX}$ pin is connected to GND and the MBL 8288 Bus Controller is added to the system as well as an MBL 8282/8283 latch for latching the system address, and a MBL 8286/8287 transceiver to allow for bus loading greater than the MBL 8086 is capable of handling. Signals ALE, DEN, and DT/$\overline{R}$ are generated by the MBL 8288 instead of the processor in this configuration although their timing remains relatively the same. The MBL 8086 status outputs ($\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$) provide type-of-cycle information and become MBL 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The MBL 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The MBL 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The MBL 8286/8287 transceiver receives the usual T and $\overline{OE}$ inputs from the MBL 8288's DT/$\overline{R}$ and DEN.

The pointer into the interrupt vector table, which is passed during the second INTA cycle, can derive from an MBL 8259A located on either the local bus or the system bus. If the master MBL 8259A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the MBL 8286/8287 transceiver when reading from the master MBL 8259A during the interrupt acknowledge sequence and software "poll".

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	–65°C to + 150°C
Voltage on Any Pin with Respect to Ground	–0.5 to + 7V
Power Dissipation	2.5 Watt

***NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(MBL 8086: V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)
(MBL 8086-2: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)
(MBL 8086-1: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
I_{CC}	Power Supply Current: MBL 8086 MBL 8086-2 MBL 8086-1		340 350 360	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	0V ⩽ V_{IN} ⩽ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V ⩽ V_{OUT} ⩽ V_{CC}
V_{CL}	Clock Input Low Voltage	-0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz

A.C. CHARACTERISTICS

(MBL 8086: V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)
(MBL 8086-2: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)
(MBL 8086-1: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	MBL 8086		MBL 8086-2		MBL 8086-1 (Preliminary)		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	100	500	ns	
TCLCH	CLK Low Time	118		68		53		ns	
TCHCL	CLK High Time	69		44		39		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		5		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into MBL 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into MBL 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into MBL 8086	118		68		53		ns	
TCHRYX	READY Hold Time into MBL 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		-8		-10		ns	
THVCH	HOLD Setup Time	35		20		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V

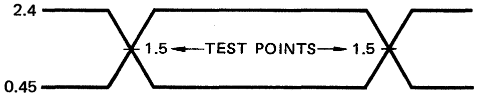
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	MBL 8086		MBL 8086-2		MBL 8086-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	10	110	10	60	10	50	ns	C_L= 20–100 pF for all MBL 8086 Outputs (in addition to MBL 8086 self-load)
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	10	40	ns	
TLHLL	ALE Width	TCLCH–20		TCLCH–10		TCLCH–10		ns	
TCLLH	ALE Active Delay		80		50		40	ns	
TCHLL	ALE Inactive Delay		85		55		45	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL–10		TCHCL–10		TCHCL–10		ns	
TCLDV	Data Valid Delay	10	110	10	60	10	50	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TWHDX	Data Hold Time After $\overline{WR}$	TCLCH–30		TCLCH–30		TCLCH–25		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	10	50	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	10	45	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	10	50	ns	
TAZRL	Address Float to READ Active	0		0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	10	70	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	10	60	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL–45		TCLCL–40		TCLCL–35		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	10	60	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL–75		2TCLCL–50		2TCLCL–40		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL–60		2TCLCL–40		2TCLCH–35		ns	
TAVAL	Address Valid to ALE Low	TCLCH–60		TCLCH–40		TCLCH–35		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

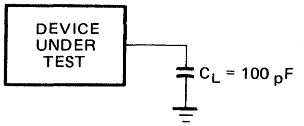
NOTES:
1. Signal at MBL 8284A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3).

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0".

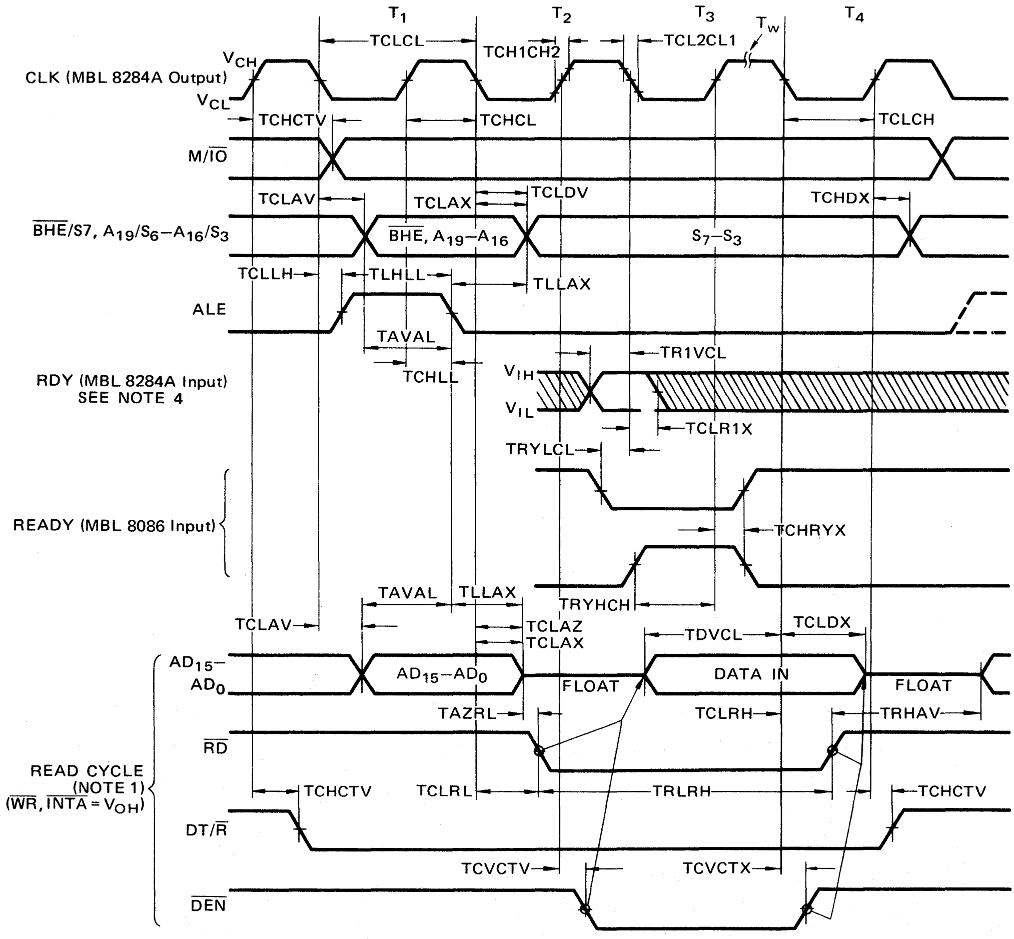
A.C. TESTING LOAD CIRCUIT



C_L: INCLUDES JIG CAPACITANCE

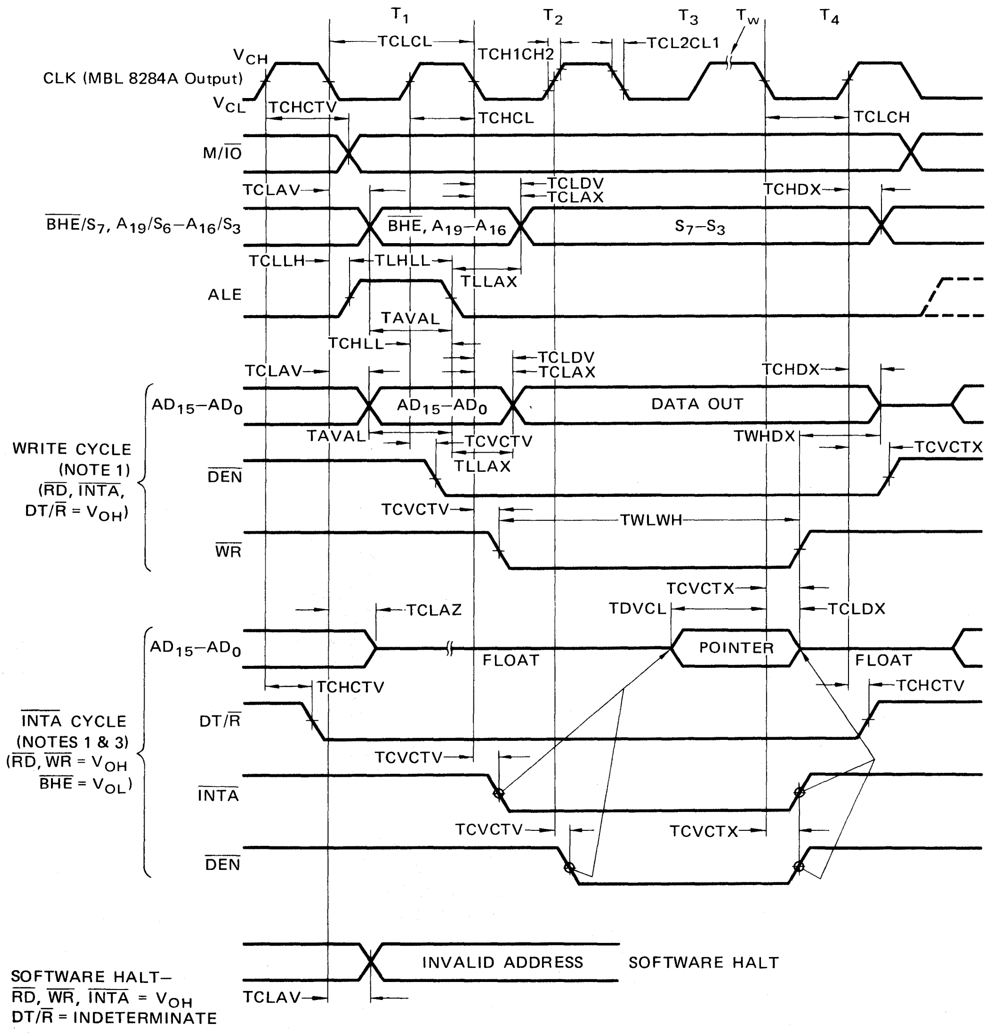
WAVEFORMS

MINIMUM MODE



WAVEFORMS (Continued)

MINIMUM MODE (Continued)



NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO $\overline{\text{INTA}}$ CYCLES RUN BACK-TO-BACK. THE MBL 8086 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH $\overline{\text{INTA}}$ CYCLES. CONTROL SIGNALS SHOWN FOR SECOND $\overline{\text{INTA}}$ CYCLE.
4. SIGNALS AT MBL 8284A ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING MBL 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	MBL 8086		MBL 8086-2		MBL 8086-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	100	500	ns	
TCLCH	CLK Low Time	118		68		53		ns	
TCHCL	CLK High Time	69		44		39		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		5		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into MBL 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into MBL 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into MBL 8086	118		68		53		ns	
TCHRYX	READY Hold Time into MBL 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	-8		-8		-10		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{\text{TEST}}$) (See Note 2)	30		15		15		ns	
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ Setup Time	30		15		12		ns	
TCHGX	$\overline{\text{RQ}}$ Hold Time into MBL 8086	40		30		20		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V

NOTES:

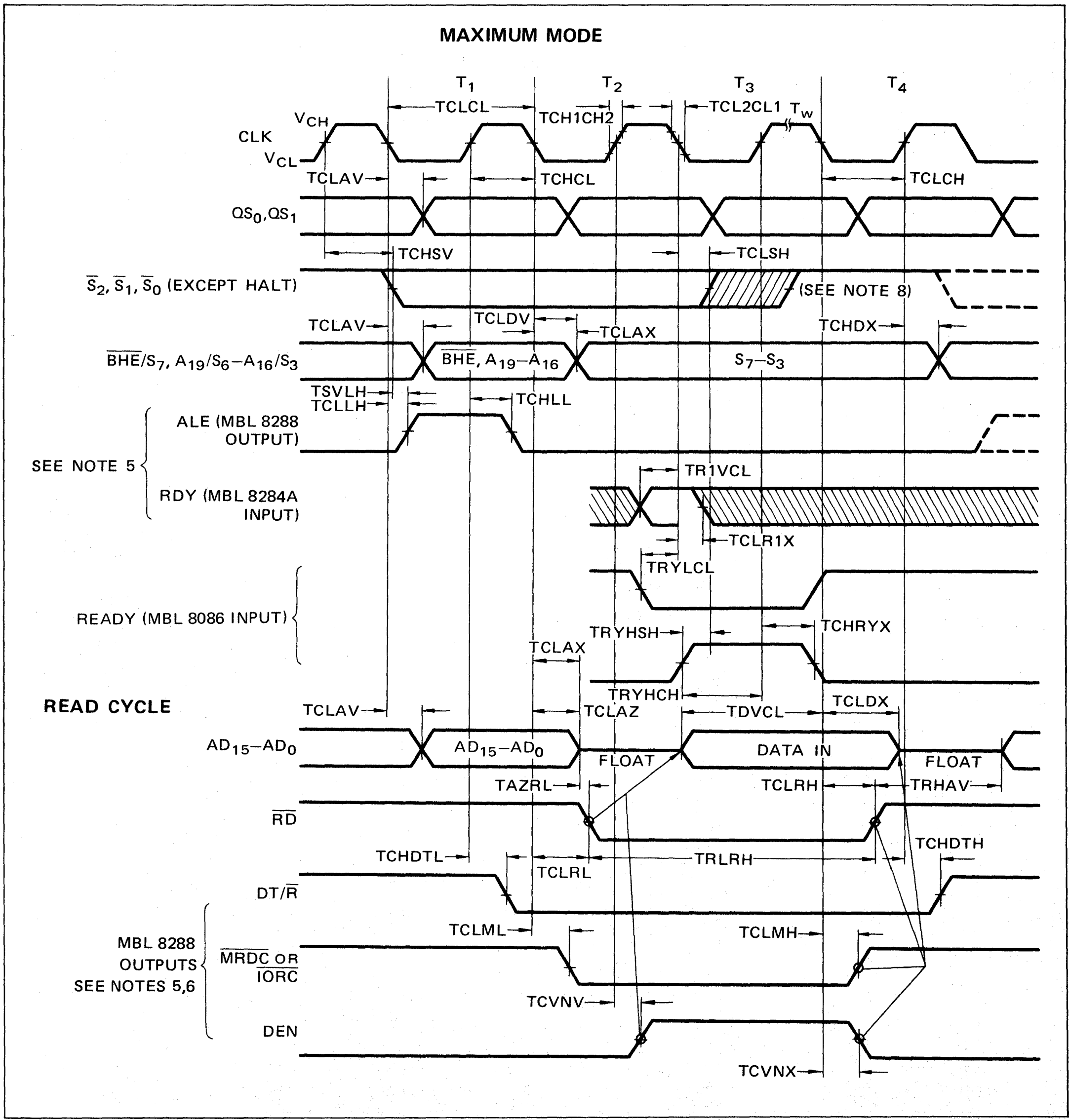
1. Signal at MBL 8284A or MBL 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

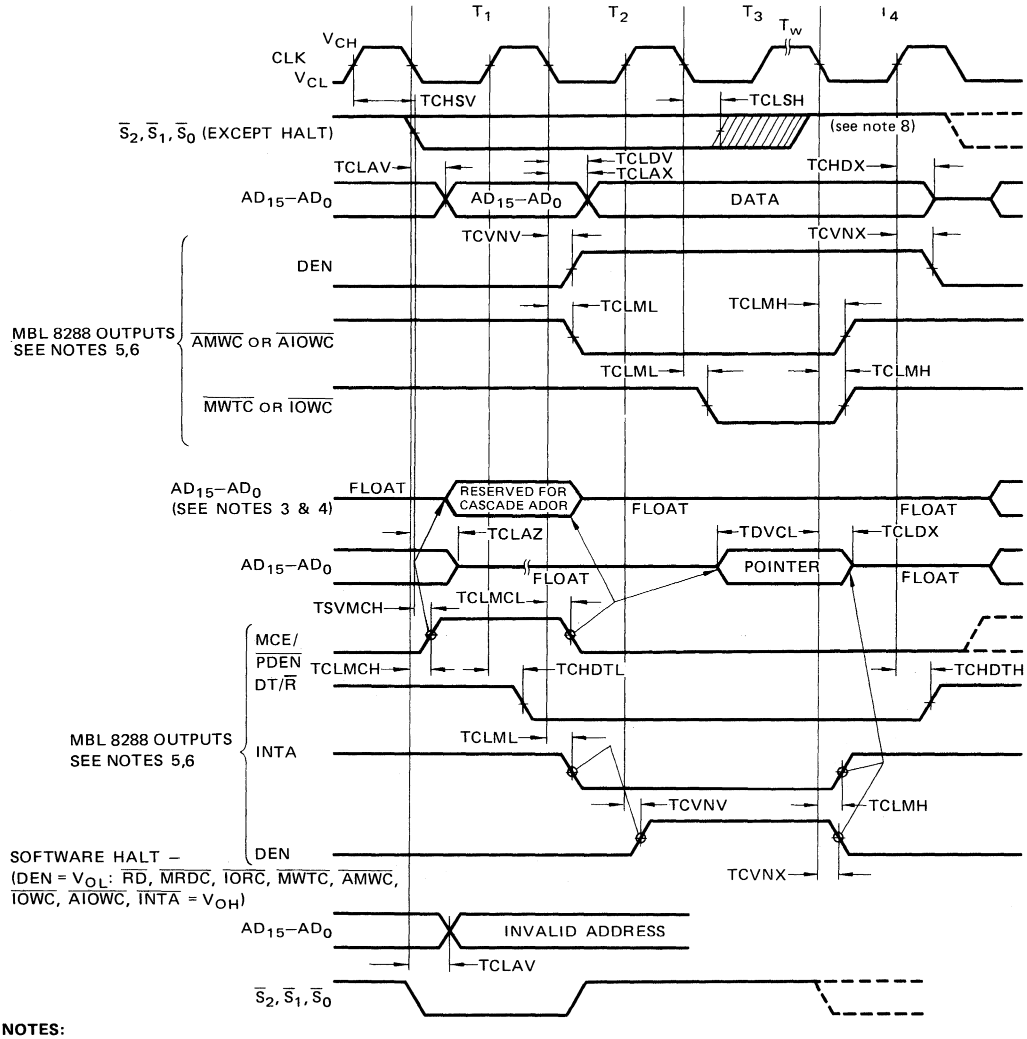
Symbol	Parameter	MBL 8086		MBL 8086-2		MBL 8086-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLML	Command Active Delay (See Note 1)	10	35	10	35	10	35	ns	*C_L = 20–100 pF for all MBL 8086 Outputs (in addition to MBL 8086 self-load)
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110		65		45	ns	
TCHSV	Status Active Delay	10	110	10	60	10	45	ns	
TCLSH	Status Inactive Delay	10	130	10	70	10	55	ns	
TCLAV	Address Valid Delay	10	110	10	60	10	50	ns	
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	10	40	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15		15	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	10	50	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	10	70	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	10	60	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL–45		TCLCL–40		TCLCL–35		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30		30	ns	
TCLGL	$\overline{GT}$ Active Delay	0	85	0	50	0	45	ns	
TCLGH	$\overline{GT}$ Inactive Delay	0	85	0	50	0	45	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL–75		2TCLCL–50		2TCLCL–40		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

WAVEFORMS


MAXIMUM MODE
T_1
T_2
T_3
T_4
T_W
TCLCL
TCH1CH2
TCL2CL1
CLK
V_{CH}
V_{CL}
TCLAV
TCHCL
TCLCH
QS_0, QS_1
TCHSV
TCLSH
$\overline{S_2}, \overline{S_1}, \overline{S_0}$ (EXCEPT HALT)
(SEE NOTE 8)
TCLAV
TCLDV
TCLAX
TCHDX
$\overline{BHE}/S_7, A_{19}/S_6-A_{16}/S_3$
$\overline{BHE}, A_{19}-A_{16}$
S_7-S_3
TSVLH
TCLLH
TCHLL
ALE (MBL 8288 OUTPUT)
SEE NOTE 5
TR1VCL
RDY (MBL 8284A INPUT)
TCLR1X
TRYLCL
READY (MBL 8086 INPUT)
TRYHSH
TCHRYX
TCLAX
TRYHCH
READ CYCLE
TCLAV
TCLAZ
TDVCL
TCLDX
$AD_{15}-AD_0$
$AD_{15}-AD_0$
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
$\overline{RD}$
TCHDTL
TCLRL
TRLRH
TCHDTH
$DT/\overline{R}$
TCLML
TCLMH
MBL 8288 OUTPUTS SEE NOTES 5,6
$\overline{MRDC}$ OR $\overline{IORC}$
TCVNV
DEN
TCVNX

WAVEFORMS (Continued)

MAXIMUM MODE (Continued)

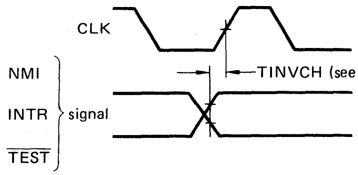

T1
T2
T3
Tw
T4
CLK
VCH
VCL
TCHSV
TCLSH
$\overline{S_2}, \overline{S_1}, \overline{S_0}$ (EXCEPT HALT)
(see note 8)
TCLAV
TCLDV
TCLAX
TCHDX
AD15–AD0
AD15–AD0
DATA
TCVNV
TCVNX
DEN
MBL 8288 OUTPUTS SEE NOTES 5,6
TCLML
TCLMH
$\overline{AMWC}$ OR $\overline{AIOWC}$
TCLML
TCLMH
$\overline{MWTC}$ OR $\overline{IOWC}$
AD15–AD0 (SEE NOTES 3 & 4)
FLOAT
RESERVED FOR CASCADE ADDR
FLOAT
FLOAT
TCLAZ
TDVCL
TCLDX
AD15–AD0
FLOAT
POINTER
FLOAT
TSVMCH
TCLMCL
MCE/PDEN
TCLMCH
TCHDTL
TCHDTH
DT/$\overline{R}$
MBL 8288 OUTPUTS SEE NOTES 5,6
TCLML
$\overline{INTA}$
TCVNV
TCLMH
DEN
TCVNX
SOFTWARE HALT – (DEN = VOL: $\overline{RD}$, $\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ = VOH)
AD15–AD0
INVALID ADDRESS
TCLAV
$\overline{S_2}, \overline{S_1}, \overline{S_0}$

NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_w TO DETERMINE IF T_w MACHINES STATES ARE TO BE INSERTED.
3. CASCADE ADDRESS IS VALID BETWEEN FIRST AND SECOND $\overline{\text{INTA}}$ CYCLE.
4. TWO $\overline{\text{INTA}}$ CYCLES RUN BACK-TO-BACK. THE MBL 8086 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH $\overline{\text{INTA}}$ CYCLES. CONTROL FOR POINTER ADDRESS IS SHOWN FOR SECOND $\overline{\text{INTA}}$ CYCLE.
5. SIGNALS AT MBL 8284A OR MBL 8288 ARE SHOWN FOR REFERENCE ONLY.
6. THE ISSUANCE OF THE MBL 8288 COMMAND AND CONTROL SIGNALS ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ AND DEN) LAGS THE ACTIVE HIGH MBL 8288 CEN.
7. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
8. STATUS INACTIVE IN STATE JUST PRIOR TO T_4.

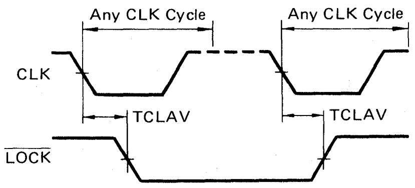
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION

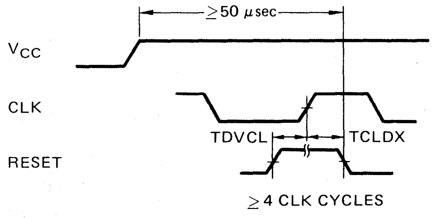


NOTE 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

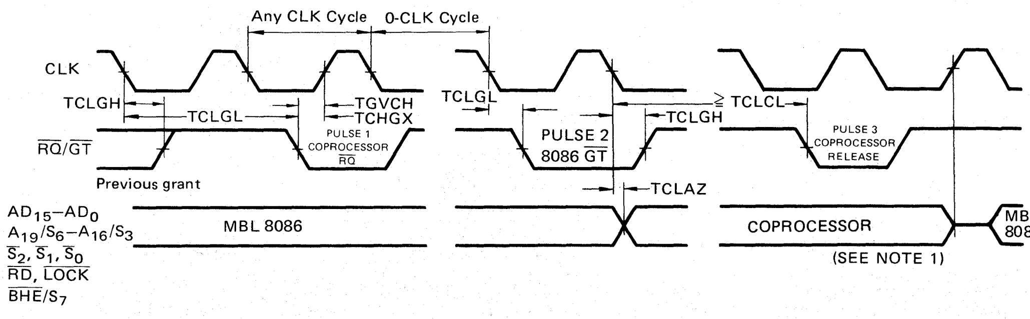
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING



REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE 1. THE COPROCESSOR MAY NOT DRIVE THE BUSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

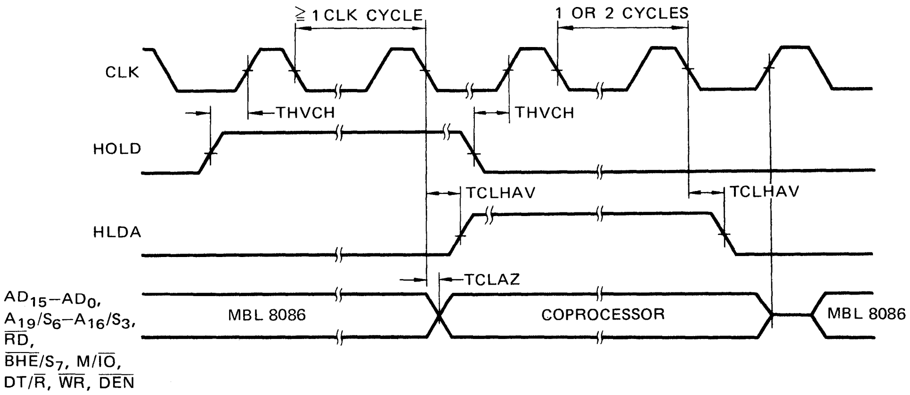


TABLE 2 – INSTRUCTION SET SUMMARY*

DATA TRANSFER

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
MOV = Move:				
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate to register	1 0 1 1 w reg	data	data if w=1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w=1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w=1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w=1	
SBB = Subtract with borrow				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w=1	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
DEC = Decrement:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG =Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w=01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w=1	
AAS =ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS =Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL =Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL=Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM=ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV =Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD =ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert byte to word	1 0 0 1 1 0 0 0			
CWD =Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT =Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL =Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR =Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL =Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR =Rotate through carry flag right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1	
TEST = And function to flags. no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w=1	

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z
MOVS = Move byte/word	1 0 1 0 0 1 0 w
CMPS = Compare byte/word	1 0 1 0 0 1 1 w
SCAS = Scan byte/word	1 0 1 0 1 1 1 w
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
STOS = Store byte/wd from AL/A	1 0 1 0 1 0 1 w

*Mnemonics © Intel Corporation, 1978

TABLE 2 – INSTRUCTION SET SUMMARY*

CONTROL TRANSFER

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CALL = Call:			
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	
JMP = Unconditional Jump:			
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1		
Within seg, adding immed, to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JMAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO = Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS = Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp
INT = Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET = Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CLC = Clear carry	1 1 1 1 1 0 0 0	
CMC = Complement carry	1 1 1 1 0 1 0 1	
STC = Set carry	1 1 1 1 1 0 0 1	
CLD = Clear direction	1 1 1 1 1 1 0 0	
STD = Set direction	1 1 1 1 1 1 0 1	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	
STI = Set interrupt	1 1 1 1 1 0 1 1	
HLT = Halt	1 1 1 1 0 1 0 0	
WAIT = Wait	1 0 0 1 1 0 1 1	
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	
NOP = No operation	1 0 0 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG
SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

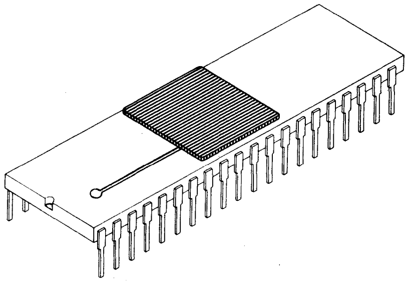
Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

*Mnemonics © Intel Corporation, 1978

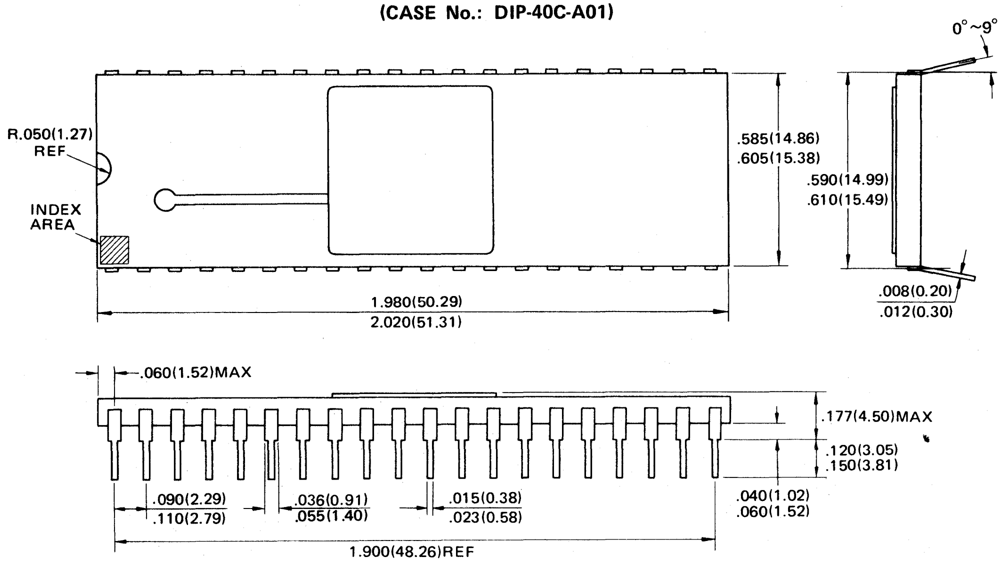
PACKAGE ILLUSTRATION

CERAMIC PAKAGE
(METAL SEAL)



PACKAGE DIMENSIONS (Suffix: -C)

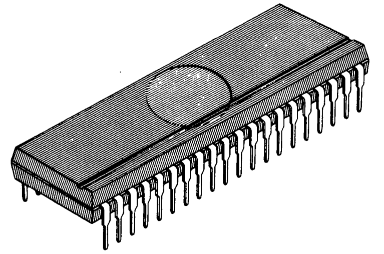
40-LEAD CERAMIC (Metal Seal) DUAL IN-LINE PACKAGE
(CASE No.: DIP-40C-A01)



Dimensions in
inches (millimeters)

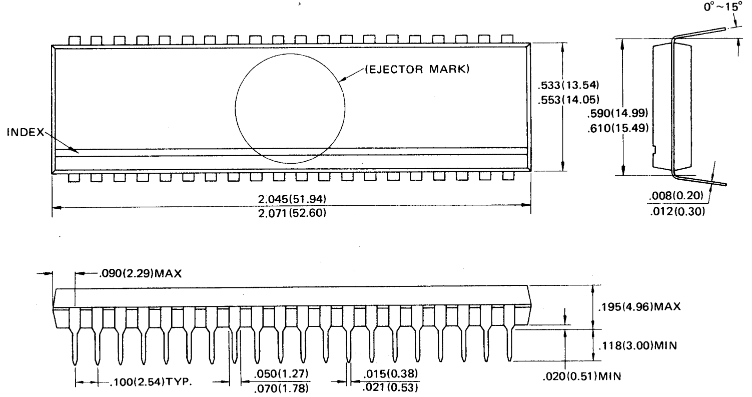
PACKAGE ILLUSTRATION

PLASTIC PACKAGE



PACKAGE DIMENSIONS (Suffix: -P)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in
inches (millimeters)

FUJITSU

NMOS HIGH-INTEGRATION 8-BIT MICROPROCESSOR

MBL 80188
MBL 80188-6

February 1986
Edition 1.0

NMOS HIGH-INTEGRATION 8-BIT MICROPROCESSOR

The Fujitsu MBL 80188 is a highly integrated microprocessor with an 8-bit data bus interface and a 16-bit internal architecture to give high performance. The MBL 80188 effectively combines 15-20 of the most common MBL 8088 components onto one. The MBL 80188 provides two times greater throughput than the standard 5MHz MBL 8088. The MBL 8088 is upward compatible with MBL 8086 and 88 software and adds 10 new instruction types to the existing set. It is housed in a 68-pad ceramic LCC (Leadless Chip Carrier: JEDEC Type A) or 68-pin ceramic PGA (Pin Grid Array) package.

- **Integrated Feature Set:**
  - **Enhanced MBL 8088-2 CPU**
  - **Clock Generator**
  - **2 Independent, High-Speed DMA Channels**
  - **Programmable Interrupt Controller**
  - **3 Programmable 16-bit Timers**
  - **Programmable Memory and Peripheral Chip-Select Logic**
  - **Programmable Wait State Generator**
  - **Local Bus Controller**
- **8-Bit Data Bus Interface: 16-bit internal architecture**
- **Available in 8 MHz (MBL 80188) and cost effective 6 MHz (MBL 80188-6) versions.**
- **High-performance 8 MHz Processor**
  - **2 Times the Performance of the Standard MBL 8088**
  - **2 MByte/Sec Bus Bandwidth Interface**
- **Direct Addressing Capability to 1 MByte of Memory**
- **Completely Object Code Compatible with All Existing MBL 8086, 88 Software**
  - **10 New Instruction Types**
- **High Performance Numerical Coprocessing Capability Through Intel 8087 Interface**
- **Two Package Options:**
  - **68-Pad Ceramic LCC (Suffix -CV) (JEDEC Type A)**
  - **68-Pin Ceramic PGA (Suffix -CR)**

Fig. 1 — BLOCK DIAGRAM

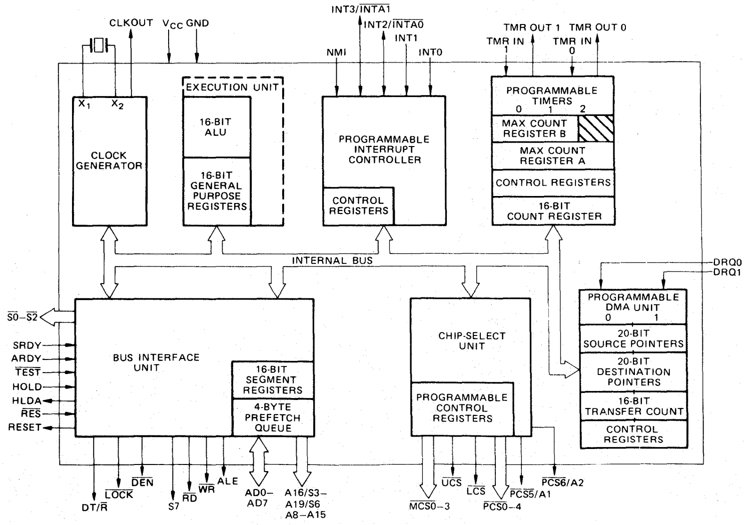


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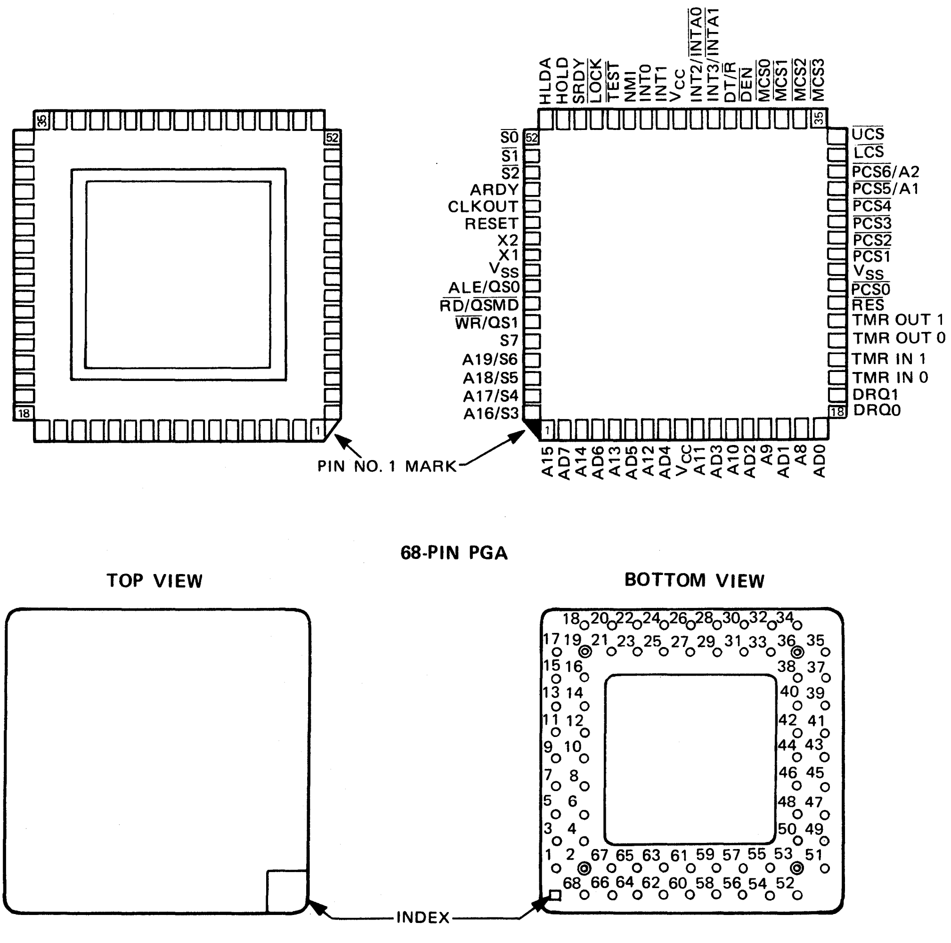
Fig. 2 — PIN CONFIGURATIONS



PIN DESCRIPTION

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
V_{CC}, V_{CC}	9, 43	I	**System Power:** +5 V power supply.
V_{SS}, V_{SS}	26, 60	I	**System Ground.**
RESET	57	O	**Reset Output** indicates that the MBL 80188 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1, X2	59, 58	I	**Crystal Inputs,** X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	**Clock Output** provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT has sufficient MOS drive capabilities for the 8087 Numeric Processor Extension.
$\overline{RES}$	24	I	**System Reset** causes the MBL 80188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the MBL 80188 clock. The MBL 80188 begins fetching instructions approximately 7 clock cycles after $\overline{RES}$ is returned HIGH. $\overline{RES}$ is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of $\overline{RES}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the MBL 80188 will drive the status lines to an inactive level for one clock, and then tri-state them.
$\overline{TEST}$	47	I	$\overline{TEST}$ is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the MBL 80188 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.
TMR IN 0, TMR IN 1	20 21	I I	**Timer Inputs** are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	**Timer Outputs** are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0, DRQ1	18 19	I I	**DMA Request** is driven HIGH by an external device when it desires that a DMA channel (Channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized.
NMI	46	I	**Non-Maskable Interrupt** is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0, INT1, INT2/$\overline{INTA0}$, INT3/INTA1	45, 44 42 41	I I/O I/O	**Maskable Interrupt Requests** can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

PIN DESCRIPTION (Continued)

Table 1 – PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>A19/S6,
A18/S5,
A17/S4,
A16/S3</td><td>65–68</td><td>O
O
O
O</td><td><b>Address Bus Outputs (16–19)</b> and <b>Bus Cycle Status (3–6)</b> reflect the four most significant address bits during T1. These signals are active HIGH. During T2, T3, Tw and T4, status information is available on these lines as encoded below:
<table>
<tr><th></th><th>Low</th><th>High</th></tr>
<tr><td>S6</td><td>Processor Cycle</td><td>DMA Cycle</td></tr>
</table>
S3, S4, and S5 are defined as LOW during T2–T4.</td></tr>
<tr><td>AD7–AD0</td><td>2,4,6,8
11,13,15,17</td><td>I/O</td><td><b>Address/Data Bus (0–7)</b> signals constitute the time mutiplexed memory or I/O address (T1) and data (T2, T3, Tw, and T4) bus. The bus is active HIGH.</td></tr>
<tr><td>A15–A8</td><td>1, 3, 5, 7
10,12,14,16</td><td>O</td><td><b>Address-only Bus (8–15),</b> containing valid address from T1–T4. The bus is active HIGH.</td></tr>
<tr><td>S7</td><td>64</td><td>O</td><td>This signal is always HIGH to indicate that the MBL 80188 has an 8-bit data bus, and is tri-state OFF during bus HOLD.</td></tr>
<tr><td>ALE/QS0</td><td>61</td><td>O</td><td><b>Address Latch Enable/Queue Status 0</b> is provided by the MBL 80188 to latch the address into the MBL 8282/8283 address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T1 of the associated bus cycle, effectively one-half clock cycle earlier than in the standard MBL 80188. The trailing edge is generated off the CLKOUT rising edge in T1 as in the MBL 80188. Note that ALE is never floated.</td></tr>
<tr><td>$\overline{WR}$/QS1</td><td>63</td><td>O</td><td><b>Write Strobe/Queue Status 1</b> indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during Reset, and then floated. When the MBL 80188 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
<table>
<tr><th>QS1</th><th>QS0</th><th>Queue Operation</th></tr>
<tr><td>0</td><td>0</td><td>No queue operation</td></tr>
<tr><td>0</td><td>1</td><td>First opcode byte fetched from the queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent byte fetched from the queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the queue</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$/$\overline{QSMD}$</td><td>62</td><td>O</td><td><b>Read Strobe</b> indicates that the MBL 80188 is performing a memory or I/O read cycle. $\overline{RD}$ is active LOW for T2, T3, and Tw of any read cycle. It is guaranteed not to go LOW in T2 until after the Address Bus is floated. $\overline{RD}$ is active LOW, and floats during "HOLD." $\overline{RD}$ is driven HIGH for one clock during Reset, and then the output driver is floated. A weak internal pull-up mechanism on the $\overline{RD}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the MBL 80188 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the Queue-Status should be provided. $\overline{RD}$ should be connected to GND to provide Queue-Status data.</td></tr>
<tr><td>ARDY</td><td>55</td><td>I</td><td><b>Asynchronous Ready</b> informs the MBL 80188 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the MBL 80188. This means that the falling edge of ARDY must be synchronized to the MBL 80188 clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied low.</td></tr>
</table>

PIN DESCRIPTION (Continued)

Table 1 – PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>SRDY</td><td>49</td><td>I</td><td><b>Synchronous Ready</b> must be synchronized externally to the MBL 80188. The use of SRDY provides a relaxed system-timing specification on the Ready input. This accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied low.</td></tr>
<tr><td>$\overline{\mathrm{LOCK}}$</td><td>48</td><td>O</td><td><b>$\overline{\mathrm{LOCK}}$</b> output indicates that other system bus masters are not to gain control of the system bus while $\overline{\mathrm{LOCK}}$ is active LOW. The $\overline{\mathrm{LOCK}}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the $\overline{\mathrm{LOCK}}$ prefix. It remains active until the completion of the instruction following the $\overline{\mathrm{LOCK}}$ prefix. No prefetches will occur while $\overline{\mathrm{LOCK}}$ is asserted. $\overline{\mathrm{LOCK}}$ is active LOW, is driven HIGH for one clock during RESET, and then floated.</td></tr>
<tr><td>$\overline{\mathrm{S0}}$, $\overline{\mathrm{S1}}$, $\overline{\mathrm{S2}}$</td><td>52–54</td><td>O</td><td><b>Bus Cycle Status</b> $\overline{\mathrm{S0}}$–$\overline{\mathrm{S2}}$ are encoded to provide bus-transaction information:
<table>
<tr><th colspan="4">MBL 80188 Bus Cycle Status Information</th></tr>
<tr><th>$\overline{\mathrm{S2}}$</th><th>$\overline{\mathrm{S1}}$</th><th>$\overline{\mathrm{S0}}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Data from Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Data to Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (no bus cycle)</td></tr>
</table>
The status pins float during "HOLD."
$\overline{\mathrm{S2}}$ may be used as a logical M/$\overline{\mathrm{IO}}$ indicator, and $\overline{\mathrm{S1}}$ and a DT/$\overline{\mathrm{R}}$ indicator. The status lines are driven HIGH for one clock during Reset, and then floated until a bus cycle begins.</td></tr>
<tr><td>HOLD,
HLDA</td><td>50
51</td><td>I
O</td><td><b>HOLD</b> indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the MBL 80188 clock. The MBL 80188 will issue a HLDA in response to a HOLD request at the end of T4 or T1. Simultaneous with the issuance of HLDA, the MBL 80188 will float the local bus and control lines. After HOLD is detected as being LOW, the MBL 80188 will lower HLDA. When the MBL 80188 needs to run another bus cycle, it will again drive the local bus and control lines.</td></tr>
<tr><td>$\overline{\mathrm{UCS}}$</td><td>34</td><td>O</td><td><b>Upper Memory Chip Select</b> is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{\mathrm{UCS}}$ is software programmable.</td></tr>
<tr><td>$\overline{\mathrm{LCS}}$</td><td>33</td><td>O</td><td><b>Lower Memory Chip Select</b> is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{\mathrm{LCS}}$ is software programmable.</td></tr>
<tr><td>$\overline{\mathrm{MCS0}}$–3</td><td>38–35</td><td>O</td><td><b>Mid-Range Memory Chip Select</b> signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{\mathrm{MCS0}}$–3 are software programmable.</td></tr>
</table>

PIN DESCRIPTION (Continued)

Table 1 – PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{\text{PCS0}}$–4	25, 27–30	O	**Peripheral Chip Select Signals 0–4** are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{\text{PCS0}}$–4 are software programmable.
$\overline{\text{PCS5}}$/A1	31	O	**Peripheral Chip Select 5 or Latched A1** may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{\text{PCS5}}$ is software programmable. When programmed to provide latched A1, rather than $\overline{\text{PCS5}}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active HIGH.
$\overline{\text{PCS6}}$/A2	32	O	**Peripheral Chip Select 6 or Latched A2** may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{\text{PCS6}}$ is software programmable. When programmed to provide latched A2, rather than $\overline{\text{PCS6}}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active HIGH.
DT/$\overline{\text{R}}$	40	O	**Data Transmit/Receive** controls the direction of data flow through the external MBL 8286/8287 data bus transceiver. When LOW, data is transferred to the MBL 80188. When HIGH, the MBL 80188 places write data bus.
$\overline{\text{DEN}}$	39	O	**Data Enable** is provided as an MBL 8286/8287 data bus transceiver output enable. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access. $\overline{\text{DEN}}$ is HIGH whenever DT/$\overline{\text{R}}$ changes state.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The following Functional Description describes the base architecture of the MBL 80188. This architecture is common to the MBL 8086, 88, and 286 microprocessor families as well. The MBL 80188 is a very high integration 8-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard MBL 8088. The MBL 80188 is object code compatible with the MBL 8086, 88 microprocessors and adds 10 new instruction types to the existing MBL 8086, 88 instruction set.

MBL 80188 BASE ARCHITECTURE

The MBL 8086, 88, 186, 188, and 286 family all contain the same basic set of registers, instructions and addressing modes. The MBL 80188 processor is upward compatible with the MBL 8086, 8088, 80186, and 80286 CPUs.

Register Set

The MBL 80188 base architecture has fourteen registers as shown in Fig. 3a and 3b. These registers are grouped into the following categories.

- **General Registers**

Eight 16-bit general purpose registers may be used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

- **Segment Registers**

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

- **Base and Index Registers**

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

- **Status and Control Registers**

Two 16-bit special purpose registers record or alter certain aspects of the MBL 80188 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Fig. 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the MBL 80188 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

Fig. 3a – GENERAL PURPOSE REGISTER SET

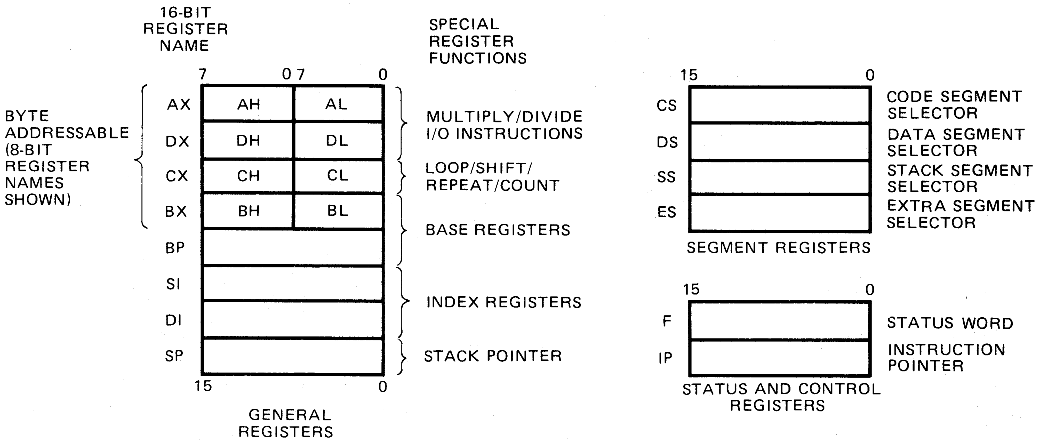


Fig. 3b – STATUS WORD FORMAT

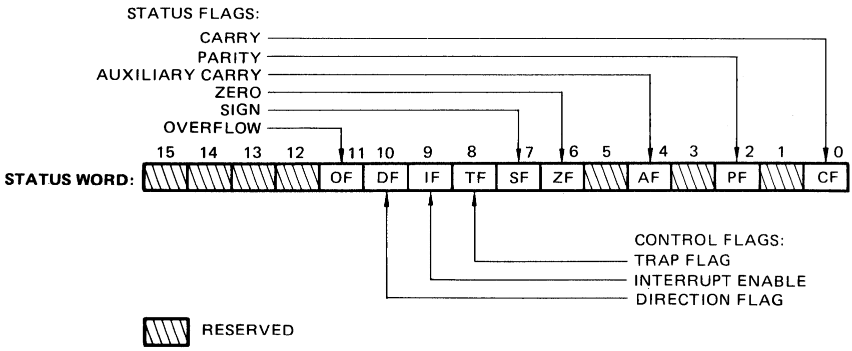


Table 2 – STATUS WORD BIT FUNCTIONS

Bit Position	Name	Function
0	CF	Carry Flag – Set on high-order bit carry or borrow; cleared otherwise.
2	PF	Parity Flag – Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise.
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise.
6	ZF	Zero Flag – Set if result is zero; cleared otherwise.
7	SF	Sign Flag – Set equal to high-order bit of result (0 if positive, 1 if negative).
8	TF	Single Step Flag – Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-Enable Flag – When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag – Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag – Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Fig. 4.

An MBL 80188 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Fig. 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Fig. 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overriden for special cases. The stack, data, and extra segments may coincide for simple programs.

Fig. 4 – MBL 80188 INSTRUCTION SET

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Fig. 4 – MBL 80188 INSTRUCTION SET (continued)

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign
JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign

UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

Fig. 5 – TWO COMPONENT ADDRESS

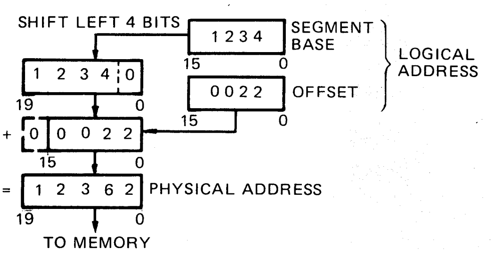
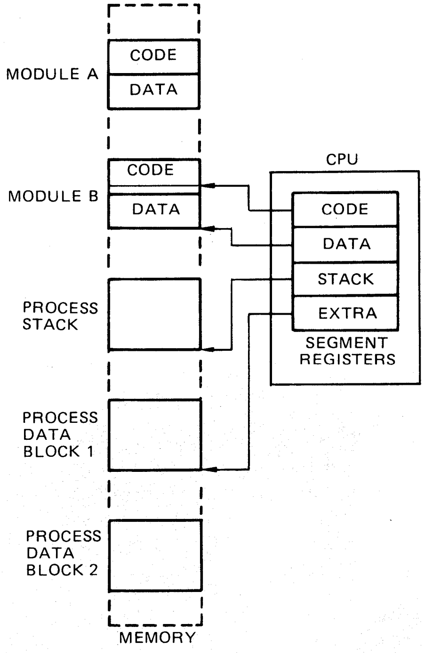


Table 3 – SEGMENT REGISTER SELECTION RULES

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

Fig. 6 – SEGMENTED MEMORY HELPS STRUCTURE SOFTWARE



Addressing Modes

The MBL 80188 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The MBL 80188 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using the MBL 80188 and Intel 8087 Numeric Data Processor.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using the MBL 80188 and Intel 8087 Numeric Data Processor configuration).

In general, individual data elements must fit within defined segment limits. Fig. 7 graphically represents the data types supported by the MBL 80188.

I/O Space

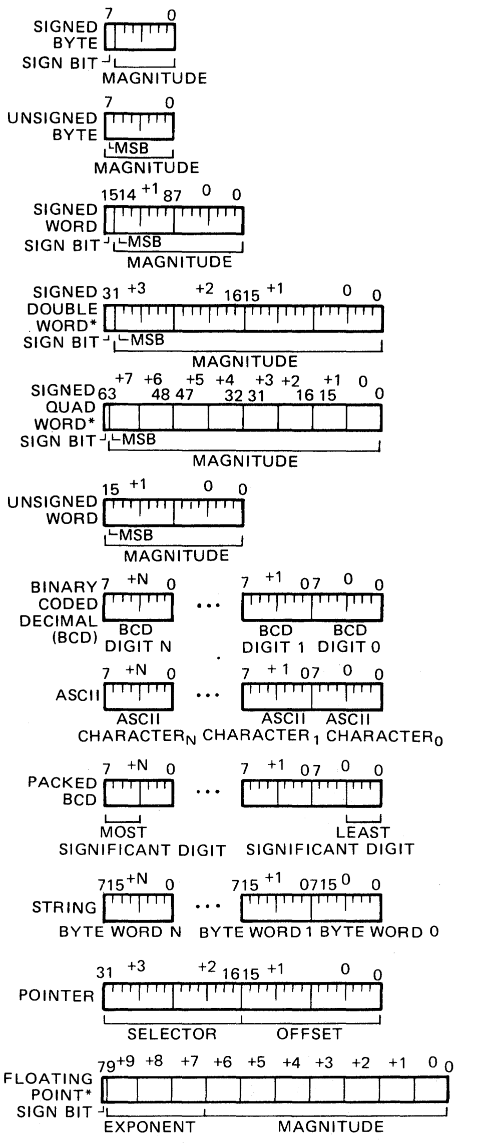
The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A15–A8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS: IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return in-

Fig. 7 — MBL 80188 SUPPORTED DATA TYPES



NOTE:
*SUPPORTED BY MBL 80188 AND INTEL 8087 NUMERIC DATA PROCESSOR CONFIGURATION.

struction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0-31, some of which are used for instruction exceptions, are reserved. Table 4 shows the MBL 80188 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the MBL 80188 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and non-cascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The MBL 80188 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INTO, DIV, IDIV, etc.) All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

The software generated MBL 80188 interrupts are described below.

- **Divide Error Exception (Type 0)**
  Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

- **Single-Step Interrupt (Type 1)**
  Generated after most instructions if the TF flag is set. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction.

- **Non-Maskable Interrupt—NMI (Type 2)**
  An external interrupt source which cannot be masked.

Table 4 – MBL 80188 INTERRUPT VECTORS

Interrupt Name	Vector Type	Default Priority	Related Instructions
Divide Error Exception	0	*1	DIV, IDIV
Single Step Interrupt	1	12**2	All
NMI	2	1	All
Breakpoint Interrupt	3	*1	INT
INTO Detected Overflow Exception	4	*1	INTO
Array Bounds Exception	5	*1	BOUND
Unused-Opcode Exception	6	*1	Undefined Opcodes
ESC Opcode Exception	7	*1***	ESC Opcodes
Timer 0 Interrupt	8	2A****	
Timer 1 Interrupt	18	2B****	
Timer 2 Interrupt	19	2C****	
Reserved	9	3	
DMA 0 Interrupt	10	4	
DMA 1 Interrupt	11	5	
INT0 Interrupt	12	6	
INT1 Interrupt	13	7	
INT2 Interrupt	14	8	
INT3 Interrupt	15	9	

NOTES:

*1. These are generated as the result of an instruction execution.

**2. This is handled as in the MBL 8088.

****3. All three timers constitute one source of request to the interrupt controller. The Timer interrpts all have the same default priority level with respect to all other interrupt sources. However, they have a defined priority ordering amongst themselves. (Priority 2A is higher priority than 2B.) Each Timer interrupt has a separate vector type number.

4. Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.

***5. An escape opcode will cause a trap only if the proper bit is set in the peripheral control block relocation register.

- **Breakpoint Interrupt (Type 3)**

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

- **INTO Detected Overflow Exception (Type 4)**

Generated during an INTO instruction if the OF bit is set.

- **Array Bounds Exception (Type 5)**

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands: The other operand indicates the value of the index to be checked.

- **Unused Opcode Exception (Type 6)**

Generated if execution is attempted on undefined opcodes.

- **Escape Opcode Exception (Type 7)**

Generated if execution is attempted of ESC opcodes (D8H–DFH). This exception will only be generated if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The MBL 80188 provides maskable hardware interrupt request pins INT0-INT3. In addition, maskable interrupts may be generated by the MBL 80188 integrated DMA controller and the integrated timer unit. The vector types for these interrupts is shown in Table 4. Software enables these inputs by setting the interrupt flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the MBL 80188 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt (NMI) is also provided. This interrupt is serviced regardless of the state of the IF bit. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced.

Single-Step Interrupt

The MBL 80188 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single-step interrupt and is controlled by the single-step flag bit (TF) in the Status Word. Once this bit is set, an internal single-step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{\text{RES}}$ input pin LOW. $\overline{\text{RES}}$ forces the MBL 80188 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{\text{RES}}$ is active. After $\overline{\text{RES}}$ becomes inactive and an internal processing interval elapses, the MBL 80188 begins execution with the instruction at physical location FFFF0(H). $\overline{\text{RES}}$ also sets some registers to predefined values as shown in Table 5.

Table 5 – MBL 80188 INITIAL REGISTER STATE AFTER RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

THE MBL 80188 COMPARED TO THE MBL 80186

The MBL 80188 CPU is an 8-bit processor designed around the MBL 80186 internal structure. Most internal functions of the MBL 80188 are identical to the equivalent MBL 80186 functions. The MBL 80188 handles the external bus the same way the MBL 80186 does with the distinction of handling only 8 bits at a time. Sixteen bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the MBL 80188 and MBL 80186 are outlined below. Internally, there are three differences between the MBL 80188 and the MBL 80186. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the MBL 80188, whereas the MBL 80186 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The MBL 80188 BIU will fetch a new instruction to load into the queue each time. There is a 1-byte hole (space available) in the queue. The MBL 80186 waits until a 2-byte space is available.
- The internal execution time of the instruction is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU may also be limited by the speed of instruction fetches when a series of simple operations occur. When the more sophisticated instructions of the MBL 80188 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The MBL 80188 and MBL 80186 are completely software compatible by virture of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally well on an MBL 80188 or an MBL 80186.

The hardware interface of the MBL 80188 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes.

- A8-A15 – These pins are only address outputs on the MBL 80188. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{\text{BHE}}$ has no meaning on the MBL 80188 and has been eliminated.

MBL 80188 CLOCK GENERATOR

The MBL 80188 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

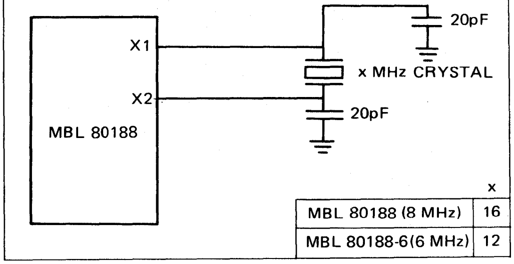
Oscillator

The oscillator circuit of the MBL 80188 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the MBL 80188. The crystal frequency selected will be double the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the MBL 80188. The recommended crystal configuration is shown in Fig. 8.

The following parameters may be used for choosing a crystal:

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	30Ω max
CO (Shunt Capacitance of Crystal):	7.0 pF max
CL (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max

Fig. 8 – RECOMMENDED MBL 80188 CRYSTAL CONFIGURATION



	x
MBL 80188 (8 MHz)	16
MBL 80188-6(6 MHz)	12

Clock Generator

The MBL 80188 clock generator provides the 50% duty cycle processor clock for the MBL 80188. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the MBL 80188. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The MBL 80188 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T2, T3 and again in the middle of each Tw until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used. Full synchronization is performed only on the rising edge of ARDY, i.e., the falling edge of ARDY must be synchronized to the CLKOUT signal if it will occur during T2, T3 or Tw. HIGH-to-LOW transitions of ARDY must be performed synchronously to the CPU clock.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T2, T3 and again at the end of each Tw until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated.

This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the MBL 80188, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The MBL 80188 provides both a $\overline{\text{RES}}$ input pin and a synchronized RESET pin for use with other system components. The $\overline{\text{RES}}$ input pin on the MBL 80188 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET is guaranteed to remain active for at least five clocks given a $\overline{\text{RES}}$ input of at least six clocks. RESET may be delayed up to two and one-half clocks behind $\overline{\text{RES}}$.

Multiple MBL 80188 processors may be synchronized through the $\overline{\text{RES}}$ input pin, since this input resets both the processor and divide-by-two internal counter in the clock generator. In order to insure that the divide-by-two counters all begin counting at the same time, the active going edge of $\overline{\text{RES}}$ must satisfy a 25 ns setup time before the falling edge of the MBL 80188 clock input. In addition, in order to insure that all CPUs begin executing in the same clock cycle, the reset must satisfy a 25 ns setup time before the rising edge of the CLKOUT signal of all the processors.

LOCAL BUS CONTROLLER

The MBL 80188 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides control lines that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The MBL 80188 provides ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ bus control signals. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are used to strobe data from memory to the MBL 80188 or to strobe data from the MBL 80188 to memory. The ALE line provides a strobe to address latches for the multiplexed address/data bus. The MBL 80188 local bus controller does not provide a memory/$\overline{\text{I/O}}$ signal. If this is required, the user will have to use the $\overline{\text{S2}}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The MBL 80188 generates two control signals to be connected to MBL 8286/8287 transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{\text{R}}$ and $\overline{\text{DEN}}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6 – TRANSCEIVER CONTROL SIGNALS DESCRIPTION

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/ Receive)	Determines the direction to travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The MBL 80188 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The MBL 80188 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. This requires external circuitry to arbitrate which external device will gain control of the bus from the MBL 80188 when there is more than one alternate local bus master. When the MBL 80188 relinquishes control of the local bus, it floats $\overline{DEN}$,$\overline{RD}$, $\overline{WR}$, $\overline{S0}$-$\overline{S2}$, $\overline{LOCK}$, AD0-AD15, A16-A19, S7, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The MBL 80188 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is the highest-priority activity request which the processor may receive: higher than instruction fetching or internal DMA cycles. However, if a DMA cycle is in progress, the MBL 80188 will complete the transfer before relinquishing the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency time can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clocks or more, if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

Local Bus Controller and Reset

Upon receipt of a RESET pulse from the $\overline{RES}$ input, the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float.

  NOTE: $\overline{RD}$ is also provided with an internal pull-up device to prevent the processor from inadvertently entering Queue Status mode during reset.

- Drive $\overline{S0}$-$\overline{S2}$ to the passive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Tristate AD0-7, A8-19, S7, DT/$\overline{R}$.
- Drive ALE LOW (ALE is never floated).
- Drive HLDA LOW.

INTERNAL PERIPHERAL INTERFACE

All the MBL 80188 integrated peripherals are controlled via 16-bit registers contained within an internal 256-byte control block. This control block may be mapped into either memory or I/O space. Internal logic will recognize the address and respond to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D7-0, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the MBL 80188 CPU at any time. The location of any register contained within the 256-byte control block is determined by the current base address of the control block.

The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Fig. 9). It provides the upper 12 bits of the base address of the control block. Note that mapping the control register block into an address range corresponding to a chip-select range is not recommended (the chip select circuitry is discussed later in this data sheet). In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space, whereas if the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

Whenever mapping the MBL 80188 peripheral control block to another location, the programming of the relocation register should be done with a byte write (i.e. OUT DX,AL). Any access to the control block is done 16 bits at a time. Thus, internally, the relocation register will get written with 16 bits of the AX register while externally, the BIU will run only one 8 bit bus cycle. If a word instruction is used (i.e. OUT DX,AX), the relocation register will be written on the first bus cycle. The BIU will then run a second bus cycle which is unnecessary. The address of the second bus cycle will no longer be within the control

block (i.e. the control block was moved on the first cycle), and therefore, will require the generation of an external ready signal to complete the cycle. For this reason we recommend byte operations to the relocation register. Byte instructions may also be used for the other registers in the control block and will eliminate half of the bus cycles required if a word operation had been specified. Byte operations are only valid on even addresses though, and are undefined on odd addresses.
In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into iRMX mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register is set to 20FFH. This causes the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Fig. 10.

The integrated MBL 80188 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data locations in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks. The overall interaction and function of the peripheral blocks has not substantially changed. The data access from/to the 256-byte internal control block will always be 16-bit and done in one bus cycle. Externally the BIU will still run two bus cycles for each 16-bit operation.

CHIP-SELECT/READY GENERATION LOGIC

The MBL 80188 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The MBL 80188 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes.

Fig. 10 – INTERNAL REGISTER MAP

	OFFSET
Relocation Register	FEH
DMA Descriptors Channel 1	DAH D0H
DMA Descriptors Channel 0	CAH C0H
Chip-Select Control Registers	A8H A0H
Timer 2 Control Registers	66H 60H
Timer 1 Control Registers	5EH 58H
Timer 0 Control Registers	56H 50H
Interrupt Controller Registers	3EH 20H

- **Upper Memory $\overline{CS}$**

The MBL 80188 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the MBL 80188 begins executing at memory location FFFF0H.

Fig. 9 – RELOCATION REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: FEH	ET	RMX	X	M/IO	Relocation Address Bits R19–R8											

ET = ESC Trap / No ESC Trap (1/0)
M/IO = Register block located in Memory / I/O Space (1/0)
RMX = Master Interrupt Controller mode / iRMX compatible Interrupt Controller mode (0/1)

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7 – UMCS PROGRAMMING VALUES

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0 = R1 = R2 = 0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Fig. 11). This register is at offset A0H in the internal control block. The legal values for bits 6-13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6-13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

Any internally generated 20-bit address whose upper 16 bits are greater than or equal to UMCS (with bits 0-5 "0") will cause UCS to be activated. UMCS bits R2-R0 are used to specify READY mode for the area of memory defined by this chip-select register, as explained below.

- **Lower Memory $\overline{CS}$**

The MBL 80188 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is also defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

The upper limit of this memory block is defined in the LMCS register (see Fig. 12). This register is at offset A2H in the internal control block. The legal values for bits 6-15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6-15 not shown in Table 8 will result in undefined operation. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Table 8 – LMCS PROGRAMMING VALUES

Upper Address	Memory Block Size	LMCS Value (Assuming R0 = R1 = R2 = 0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0-5 "1") will cause $\overline{LCS}$ to be active. LMCS register bits R2-R0 are used to specify the READY mode for the area of memory defined by this chip-select register.

- **Mid-Range Memory $\overline{CS}$**

The MBL 80188 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the MBL 80188 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8-14 of the MPCS register (see Fig. 13). This register is at location A8H in the internal control block. One and only one of bits 8-14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. Thus, if the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as described in a later section.

Table 9 – MPCS PROGRAMMING VALUES

Total Block Size	Individual Select Size	MPCS Bits 14-8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15-9 of the MMCS register (see Fig. 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{\text{MCS}}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After reset, the contents of both of these registers are undefined. However, none of the $\overline{\text{MCS}}$ lines will be active until both the MMCS and MPCS registers are accessed.

MMCS bits R2–R0 specify READY mode of operation for all mid-range chip selects. All devices in mid-range memory must use the same number of WAIT states.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{\text{LCS}}$ line was programmed, there would be an internal conflict between the $\overline{\text{LCS}}$ ready generation logic and the $\overline{\text{MCS}}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{\text{UCS}}$ ready generation logic. Since the $\overline{\text{LCS}}$ chip-select line does not become active until programmed, while the $\overline{\text{UCS}}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{\text{LCS}}$ range must not be programmed.

Peripheral Chip Selects

The MBL 80188 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven $\overline{\text{CS}}$ lines called $\overline{\text{PCS0-6}}$ are generated by the MBL 80188. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{\text{PCS5}}$ and $\overline{\text{PCS6}}$ can also be programmed to provide latched

Fig. 11 — UMCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A0H	1	1	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
	A19								A11							

Fig. 12 — LMCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A2H	0	0	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
	A19								A11							

Fig. 13 — MPCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A8H	1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0

Fig. 14 — MMCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A6H	U	U	U	U	U	U	U	1	1	1	1	1	1	R2	R1	R0
	A19						A13									

Fig. 15 — PACS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A4H	U	U	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
	A19									A10						

address bits A1, A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0, A1 pins used for selecting internal registers of 8-bit peripheral chips. This scheme simplifies the hardware interface because the 8-bit registers of peripherals are simply treated as 16-bit registers located on even boundaries in I/O space or memory space where only the lower 8-bits of the register are significant: the upper 8-bits are "don't cares."

The starting address of the peripheral chip-select block is defined by the PACS register (see Fig. 15). This register is located at offset A4H in the internal control block. Bits 15-6 of this register correspond to bits 19-10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9-0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12-15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

The user should program bits 15-6 to correspond to the desired peripheral base location. PACS bits 0-2 are used to specify READY mode for $\overline{\text{PCS0}}$-$\overline{\text{PCS3}}$.

Table 10 — PCS ADDRESS RANGES

PCS Line	Active between Locations
PCS0	PBA – PBA + 127
PCS1	PBA + 128 – PBA + 255
PCS2	PBA + 256 – PBA + 383
PCS3	PBA + 384 – PBA + 511
PCS4	PBA + 512 – PBA + 639
PCS5	PBA + 640 – PBA + 767
PCS6	PBA + 768 – PBA + 895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Fig. 16). This register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{\text{PCS5}}$ and $\overline{\text{PCS6}}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After reset, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11 — MS, EX PROGRAMMING VALUES

Bit	Description
MS	1 = Peripherals mapped into memory space. 0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{\text{PCS}}$ lines. A1, A2 provided. 1 = 7 $\overline{\text{PCS}}$ lines. A1, A2 are not provided.

MPCS bits 0-2 are used to specify READY mode for $\overline{\text{PCS4}}$-$\overline{\text{PCS6}}$ as outlined below.

READY Generation Logic

The MBL 80188 can generate a "READY" signal internally for each of the memory or peripheral $\overline{\text{CS}}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0-3 wait states for all accesses to the area for which the chip select is active. In addition, the MBL 80188 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{\text{CS}}$ line or group of lines generated by the MBL 80188. The interpretation of the ready bits is shown in Table 12.

Table 12 — READY BITS PROGRAMMING

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). This means, for example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2-R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2-R0 of PACS set the PCS0-3 READY mode, R2-R0 of MPCS set the PCS4-6 READY mode.

Chip Select/Ready Logic and Reset

Upon reset, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the UCS line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to allow the maximum number of internal wait states in conjunction with external Ready consideration (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the PCS lines will become active.

DMA CHANNELS

The MBL 80188 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of one MByte/sec.

DMA Operation

Each channel has six registers in the control block which define each channel's specific operation. The control registers consist of a 20-bit Source Pointer (2 words), a 20-bit Destination Pointer (2 words), a 16-bit Transfer Counter, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Fig. 18). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13 – DMA CONTROL BLOCK FORMAT

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Counter	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular MBL 80188 DMA channel. This register specifies:

- the mode of synchronization;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

Fig. 16 – MPCS REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET: A8H	1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0

Fig. 17 – DMA UNIT BLOCK DIAGRAM

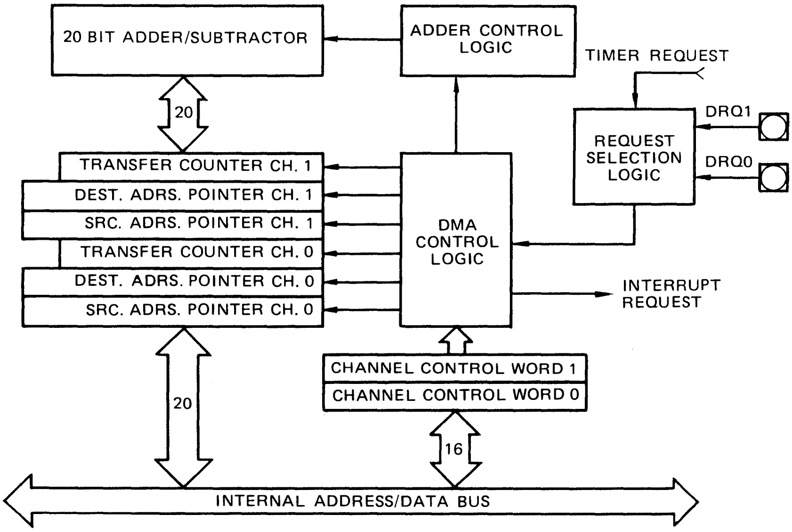


Fig. 18 – DMA CONTROL REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M/$\overline{\text{IO}}$	DESTINATION DEC	INC	M/$\overline{\text{IO}}$	SOURCE* DEC	INC	TC	INT	SYN		P	TDRQ	X	CHG/ NOCHG	ST/ STOP	X

X = DON'T CARE.

DMA Control Word Bit Descriptions

ST/$\overline{\text{STOP}}$: Start/Stop (1/0) Channel.

CHG/$\overline{\text{NOCHG}}$: Change/Do not change (1/0) ST/$\overline{\text{STOP}}$ bit. If this bit is set when writing to the control word, the ST/$\overline{\text{STOP}}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{\text{STOP}}$ bit will not be altered. This bit is not stored; it will always be a 0 on read.

INT: Enable Interrupts to CPU on byte count termination.

TC: If set, DMA will terminate when the contents of the Transfer Count register reach zero. The ST/$\overline{\text{STOP}}$ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN: (2 bits)

00 No synchronization.

NOTE: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.

01 Source synchronization.

10 Destination synchronization.

11 Unused.

SOURCE: INC Increment source pointer by 1 after each transfer.

M/$\overline{\text{IO}}$ Source pointer is in M/IO space (1/0).

DEC Decrement source pointer by 1 after each transfer.

DEST:	INC	Increment destination pointer by 1 after each transfer.
	M/$\overline{\text{IO}}$	Destination pointer is in M/IO space (1/0).
	DEC	Decrement destination pointer by 1 after each transfer.
P:		Channel priority – relative to other channel. 0: low priority. 1: high priority. Channels will alternate cycles if both set at same priority level.
TDRQ:		0: Disable DMA requests from timer 2. 1: Enable DMA requests from timer 2.
Bit 3:		Bit 3 is not used.

If both INC and DEC are specified for the same pointer, the pointer will remain constant after each cycle.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Fig. 18a). These pointers may be individually incremented or decremented after each transfer. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or unsynchronized transfers are programmed, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). No prefetching occurs when destination synchronization is performed, however. Data will not be fetched from the source address until the destination device signals that it is ready to receive it. When destination synchronized transfers are requested, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another DMA cycle will begin after two processor clocks. This is done to allow the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. These lead to the maximum DMA transfer rates shown in Table 14.

Table 14 – MAXIMUM DMA TRANSFER RATES

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	1MBytes/sec	1MBytes/sec
Source Synch	1MBytes/sec	1MBytes/sec
Destination Synch	0.65MBytes/sec	0.75MBytes/sec

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from

Fig. 18a – DMA MEMORY POINTER REGISTER FORMAT

	15			0
HIGHER REGISTER ADDRESS	XXX	XXX	XXX	A19–A16
LOWER REGISTER ADDRESS	A15–A12	A11–A8	A7–A4	A3–A0

XXX = DON'T CARE

a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed such that one channel is always given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses the odd memory locations; however, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/$\overline{\text{STOP}}$ bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also have been generated. Therefore, the source and destination transfer pointers, and the transfer count register (if used) must be programmed before this bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/$\overline{\text{NOCHG}}$ bit is cleared when the control register is written, the ST/$\overline{\text{STOP}}$ bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- The Start/Stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

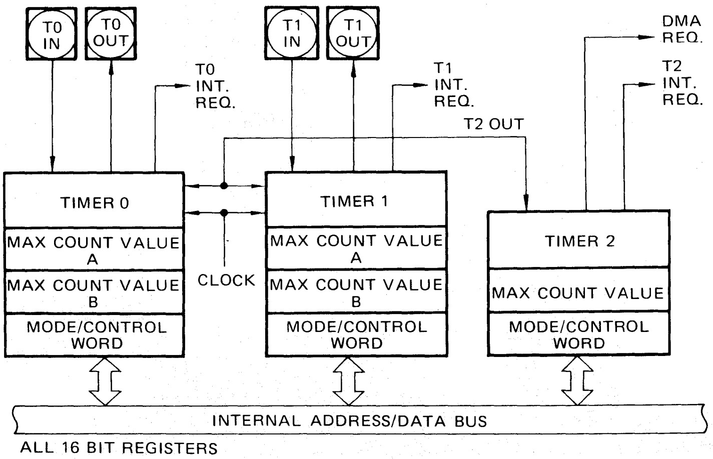
TIMERS

The MBL 80188 provides three internal 16-bit programmable timers (see Fig. 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

Timer Operation

The timers are controlled by 11 16-bit registers in the internal peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incre-

Fig. 19 — TIMER BLOCK DIAGRAM



mented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values programmed by the user. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 2 clocks after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input. Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Fig. 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15 – TIMER CONTROL BLOCK FORMAT

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

ALT:

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating nonrepetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT:

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

EXT:

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the MBL 80188 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit.

Fig. 20 – TIMER MODE/CONTROL REGISTER

15	14	13	12	11		5	4	3	2	1	0
EN	$\overline{\text{INH}}$	INT	RIU	0	....	MC	RTG	P	EXT	ALT	CONT

The maximum input to output transition latency time may be .as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

P:
The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG:
Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the MBL 80188 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN:
The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH:
The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:
When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller.)

MC:
The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts. Programmer intervention is required to clear this bit.

RIU:
The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. The condition which causes a timer to reset is equivalent between the current count value and the max count being used. This means that if the count is changed to be above the max count value, or if the max count value is changed to be below the current value, the timer will not reset to zero, but rather will count to its maximum value, "wrap around" to zero, then count until the max count is reached.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- All SEL (Select) bits are reset to zero. This selects MAX COUNT register A, resulting in the Timer Out pins going HIGH upon RESET.

INTERRUPT CONTROLLER

The MBL 80188 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The MBL 80188 interrupt controller has its own control registers that set the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Fig. 21.

The interrupt controller has a special iRMX 86 compatibility mode that allows the use of the MBL 80188 within the iRMX 86 operating system interrupt structure. The controller is set in this mode by setting bit 14 in the peripheral control block relocation register (see iRMX 86 Compatibility Mode section). In this mode, the internal MBL 80188 interrupt controller functions as a "slave" controller to an external "master" controller. Special initialization software must be included to properly set up the MBL 80188 interrupt controller in iRMX 86 mode.

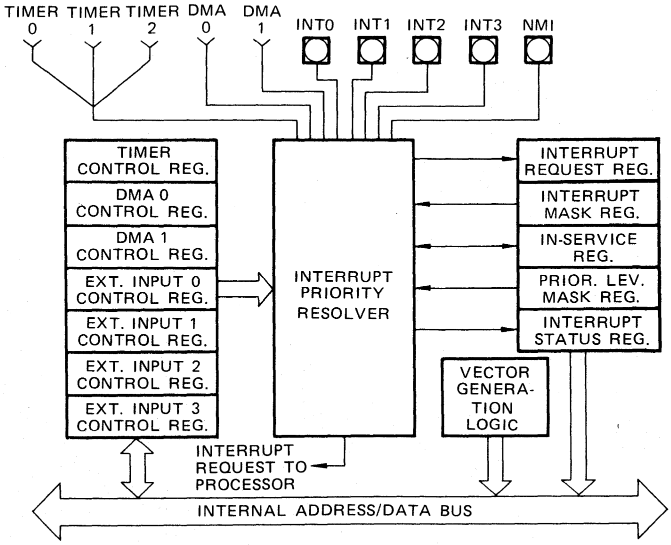
NON-iRMX MODE OPERATION

Interrupt Controller External Interface

For external interrupt sources, five dedicated pins are provided. One of these pins is dedicated to NMI, non-maskable interrupt. This is typically used for power-fail interrupts, etc. The other four pins may function either as four interrupt input lines with internally generated interrupt vectors, as an interrupt line and an interrupt acknowledge line (called the "cascade mode") along with two other input lines with internally generated interrupt vectors, or as two interrupt input lines and two dedicated interrupt acknowledge output lines. When the interrupt lines are configured in cascade mode, the MBL 80188 interrupt controller will not generate internal interrupt vectors.

External sources in the cascade mode use externally gene-

Fig. 21 – INTERRUPT CONTROLLER BLOCK DIAGRAM



rated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the MBL 80188 on the second cycle. The capability to interface to external MBL 8259A programmable interrupt controllers is thus provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in non-iRMX mode are similar to the MBL 8259A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

- **Fully Nested Mode**

When in the fully nested mode four pins are used as direct interrupt requests. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled without being themselves interrupted by lower-priority interrupts. Since interrupts are enabled, higher-priority interrupts will be serviced.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is issued at the end of the service routine just before the issuance of the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

- **Cascade Mode**

The MBL 80188 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Fig. 22. INT0 is an interrupt input interfaced to an MBL 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave MBL 8259As. Three levels of priority are created, requiring priority resolution in the MBL 80188 interrupt controller, the master MBL 8259As, and the slave MBL 8259As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

- **Special Fully Nested Mode**

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external MBL 8259A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same MBL 80188 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the MBL 80188 controller until the MBL 80188 in-service bit is reset. In special fully nested mode, the MBL 80188 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority MBL 80188 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the external master's IS register is required to determine if there is more than one bit set. If so, the IS bit in the MBL 80188 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Fig. 31). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0-4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-

Service bit of the highest-priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The MBL 80188 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

Non-iRMX Mode Features

- **Programmable Priority**

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0-7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, it allows other requests to be serviced.

- **End-of-Interrupt Command**

The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

- **Trigger Mode**

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the MBL 80188 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to reenable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

- **Interrupt Vectoring**

The MBL 80188 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Mode. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Fig. 23. It contains 15 registers. All registers can both be read or written unless specified otherwise.

- **In-Service Register**

This register can be read from or written into. The format

Fig. 22 – CASCADE MODE INTERRUPT CONNECTION

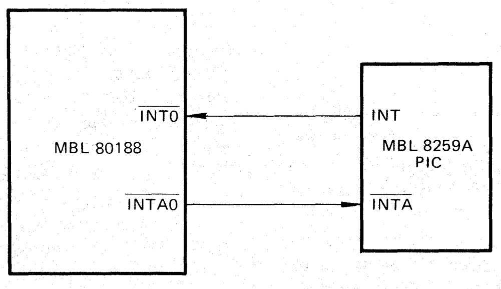


Fig. 23 – INTERRUPT CONTROLLER REGISTERS (NON-iRMX 86 MODE)

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA1 CONTROL REGISTER	36H
DMA0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

is shown in Fig. 24. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command issued by the CPU.

- **Interrupt Request Register**

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Fig. 24. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits show exactly when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

- **Mask Register**

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in

Fig. 24 – IN-SERVICE, INTERRUPT REQUEST, AND MASK REGISTER FORMATS

15	14		10	9	8	7	6	5	4	3	2	1	0
0	0	· · ·	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Fig. 25 – PRIORITY MASK REGISTER FORMAT

15	14		3	2	1	0
0	0	· · · · · · · · · ·	0	PRM2	PRM1	PRM0

Fig. 26 – INTERRUPT STATUS REGISTER FORMAT

15	14		7	6	5	4	3	2	1	0
DHLT	0	· · · · · ·	0	0	0	0	0	IRT2	IRT1	IRT0

Fig. 24. A one in a bit position corresponding to a particular source serves to mask the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

- **Priority Mask Register**

This register is used to mask all interrupts below particular interrupt priority levels. The format of this register is shown in Fig. 25. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so all interrupts are unmasked.

- **Interrupt Status Register**

This register contains general interrupt controller status information. The format of this register is shown in Fig. 26. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. The purpose of this bit is to allow prompt service of all non-maskable interrupts. This bit may also be set by the CPU.

IRTx: These three bits represent the individual timer interrupt request bits. These bits are used to differentiate the timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

- **Timer, DMA 0, 1 Control Registers**

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Fig. 27. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

- **INT0—INT3 Control Registers**

These registers are the control words for the four external input pins. Fig. 28 shows the format of the INT0 and INT1 Control registers; Fig. 29 shows the format of the INT2 and INT3 Control registers. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PR0-2: Priority programming information. Highest priority = 000, lowest priority = 111.

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt Input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is

Fig. 27 — TIMER/DMA CONTROL REGISTER FORMATS

15	14		4	3	2	1	0
0	0	· · · · · · · · ·	0	MSK	PR2	PR1	PR0

Fig. 28 — INT0/INT1 CONTROL FORMATS

15	14		7	6	5	4	3	2	1	0
0	0	· · · · · ·	0	SFNM	C	LTM	MSK	PR2	PR1	PR0

Fig. 29 — INT2/INT3 CONTROL REGISTER FORMATS

15	14		5	4	3	2	1	0
0	0	· · · · · · · ·	0	LTM	MSK	PR2	PR1	PR0

high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = nonmask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special fully nested mode bit, 1 = SFNM

- **EOI Register**

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Fig. 30. It initiates an EOI command when written to by the MBL 80188 CPU.

The bits in the EOI register are encoded as follows:

Sx: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10. Note that to reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

NSPEC/: A bit that determines the type of EOI com-
SPEC mand. Nonspecific = 1, Specific = 0.

- **Poll and Poll Status Registers**

These registers contain polling information. The format of these registers is shown in Fig. 31. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

Sx: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

Table 16 – INTERNAL SOURCE PRIORITY LEVEL

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA 1
4	Timer 1
5	Timer 2

iRMX 86 COMPATIBILITY MODE

This mode allows iRMX 86-80188 compatibility. The interrupt model of iRMX 86 requires one master and multiple slave MBL 8259As is cascaded fashion. When iRMX mode is used, the internal MBL 80188 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal MBL 80188 resources will be monitored through the internal interrupt controller, while the external controller functions as the system master interrupt controller.

Upon reset, the MBL 80188 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX 86 mode, bit 14 of the Relocation Register should be set.

Because of pin limitations caused by the need to interface to an external MBL 8259A master, the internal interrupt controller will no longer accept external inputs. There are however, enough MBL 80188 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit,

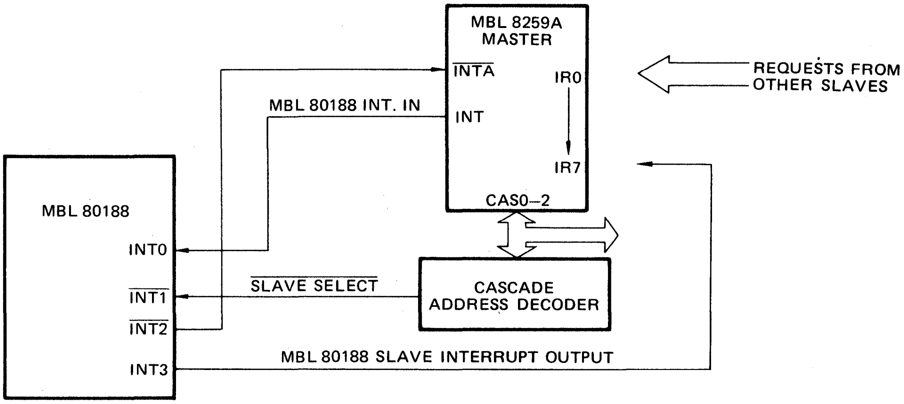
Fig. 30 – EOI REGISTER FORMAT

15	14	13		5	4	3	2	1	0
SPEC/ NSPEC	0	0	· · · · · ·	0	S4	S3	S2	S1	S0

Fig. 31 – POLL REGISTER FORMAT

15	14	13		5	4	3	2	1	0
INT REQ	0	0	· · · · ·	0	S4	S3	S2	S1	S0

Fig. 32 – iRMX 86 INTERRUPT CONTROLLER INTERCONNECTION



and control word.

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the MBL 80188 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source. The required priority levels for the internal interrupt sources in iRMX mode are shown in Table 16.

These level assignments must remain fixed in the iRMX 86 mode of operation.

iRMX 86 Mode External Interface

The configuration of the MBL 80188 with respect to an external MBL 8259A master is shown in Fig. 32. The INT0 input is used as the MBL 80188 CPU interrupt input. INT3 functions as an output to send the MBL 80188 slave-interrupt-request to one of the 8 master-PIC-inputs.

Correct master-slave interface requires decoding of the slave addresses (CAS0-2). Slave MBL 8259As do this internally. Because of pin limitations, the MBL 80188 slave address will have to be decoded externally. $\overline{\text{INT1}}$ is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{\text{INT2}}$ is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an MBL 8259A.

Interrupt Nesting

iRMX 86 mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the iRMX 86 Mode

Vector generation in iRMX mode is exactly like that of an MBL 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic. These bits represent the encoding of the priority level requesting service. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the iRMX 86 Mode

All control and command registers are located inside the internal peripheral control block. Fig. 33 shows the offsets of these registers.

- **End-of-Interrupt Register**

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Fig. 34. It initiates an EOI command when written by the MBL 80188 CPU.

The bits in the EOI register are encoded as follows:

Lx: Encoded value indicating the priority of the IS bit to be reset.

- **In-Service Register**

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Fig. 35. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

- **Interrupt Request Register**

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Fig. 35. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

- **Mask Register**

This register contains a mask bit for each interrupt source. The format for this register is shown in Fig. 35. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bit are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

Fig. 33 – INTERRUPT CONTROLLER REGISTERS (iRMX 86 MODE)

	OFFSET
LEVEL 5 CONTROL REGISTER (TIMER 2)	3AH
LEVEL 4 CONTROL REGISTER (TIMER 1)	38H
LEVEL 3 CONTROL REGISTER (DMA 1)	36H
LEVEL 2 CONTROL REGISTER (DMA 0)	34H
LEVEL 0 CONTROL REGISTER (TIMER 0)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

- **Control Registers**

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Fig. 36. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

PRx: 3-bit encoded field indicating a priority level for the source; not that each source must be programmed at specified levels.

MSK: mask bit for the priority level indicated by PRx bits.

Fig. 34 – SPECIFIC EOI REGISTER FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · ·	0	0	0	0	0	0	L2	L1	L0

Fig. 35 – IN-SERVICE, INTERRUPT REQUEST, AND MASK REGISTER FORMATS

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · · ·	0	0	0	TMR2	TMR1	D1	D0	0	TMR0

- **Interrupt Vector Register**

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Fig. 37. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

tx: 5-bit field indicating the upper five bits of the vector address.

- **Priority-Level Mask Register**

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

mx: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

- **Interrupt Status Register**

This register is defined exactly as in non-iRMX mode (see Fig. 26).

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

Fig. 36 – CONTROL WORD FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · ·	0	0	0	0	0	MSK	PR2	PR1	PR0

Fig. 37 – INTERRUPT VECTOR REGISTER FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · ·	0	t4	t3	t2	t1	t0	0	0	0

Fig. 38 – PRIORITY LEVEL MASK REGISTER FORMAT

15	14	13		8	7	6	5	4	3	2	1	0
0	0	0	· · · ·	0	0	0	0	0	0	m2	m1	m0

Fig. 39 – TYPICAL MBL 80188 COMPUTER

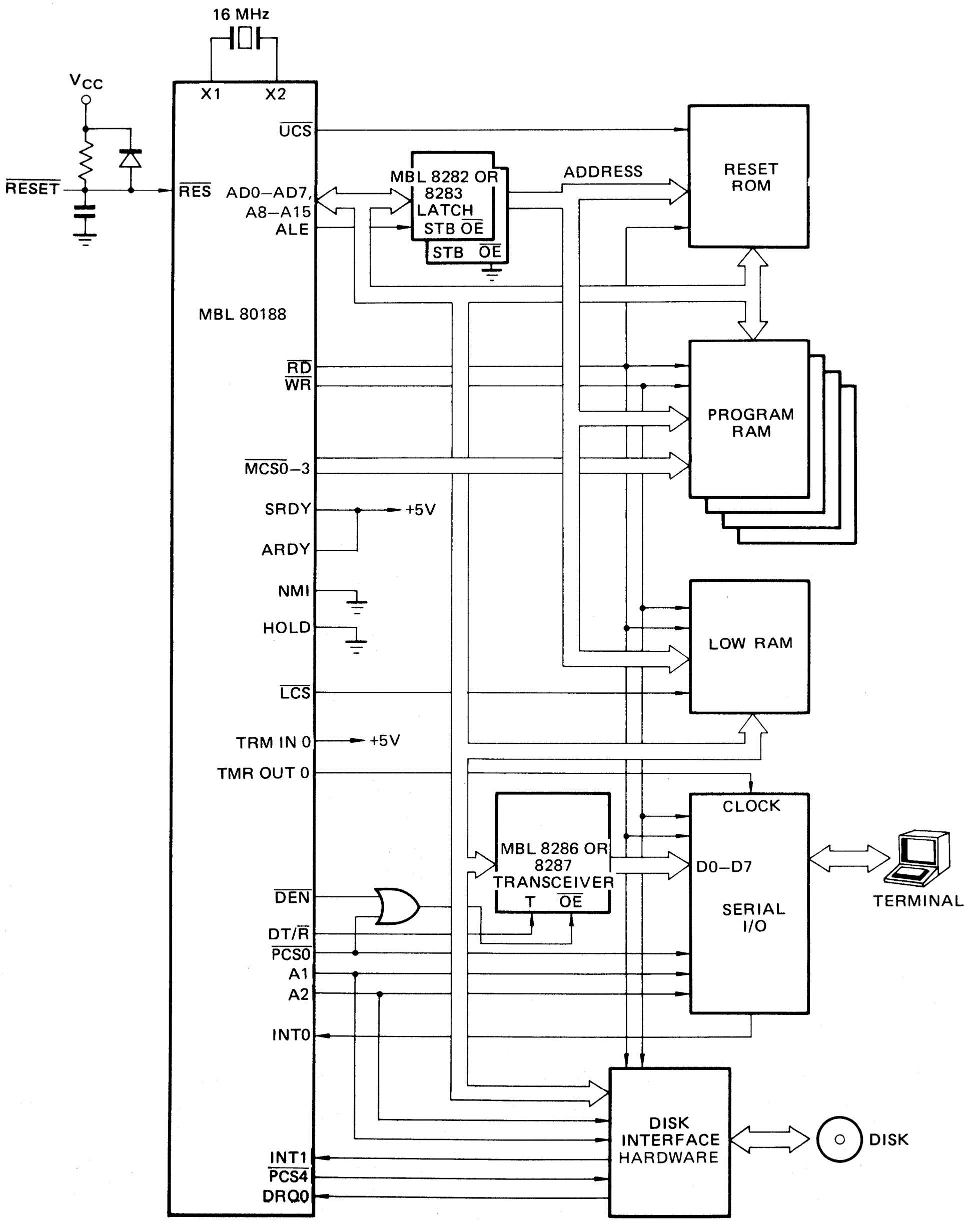
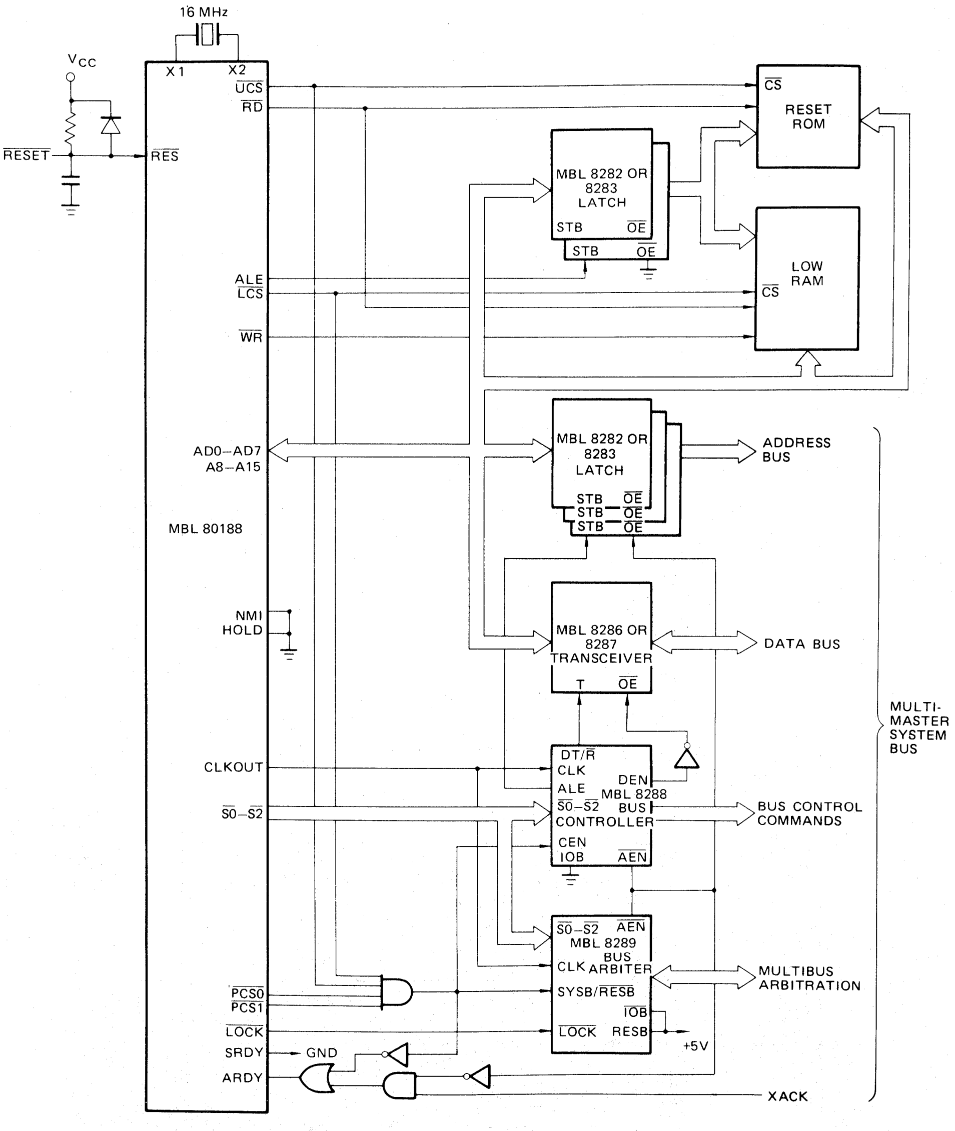


Fig. 40 – TYPICAL MBL 80188 MULTI-MASTER BUS INTERFACE



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias . . . . 0°C to 70°C
Storage Temperature . . . . -65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . -1.0V to +7V
Power Dissipation . . . . 3 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0° to 70°C)

Applicable to MBL 80188 (8 MHz) and MBL 80188-6 (6 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	2.0	V_{CC}+0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA for $\overline{S0}$-$\overline{S2}$ I_{OL} = 2.0 mA for all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
I_{CC}	Power Supply Current		550 450	mA	Max measured at T_A = 0° C T_A = 70°C
I_{LI}	Input Leakage Current		±10	μA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V < V_{OUT} < V_{CC}
V_{CLI}	Clock Input Low Voltage	-0.5	0.6	V	
V_{CHI}	Clock Input High Voltage	3.9	V_{CC}+1.0	V	
V_{CLO}	Clock Output Low Voltage		0.6	V	I_{OL} = 4.0 mA
V_{CHO}	Clock Output High Voltage	4.0		V	I_{OH} = -200 μA
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

A.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0° to 70°C)

MBL 80188 Timing Requirements All Timings Measured At 1.5 Volts Unless Otherwise Noted.

Applicable to MBL 80188 (8 MHz) and MBL 80188-6 (6 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TDVCL	Data in Setup Time (A/D)	20		ns	
TCLDX	Data in Hold Time (A/D)	10		ns	
TARYHCH	Asynchronous Ready (AREADY) Active Setup Time*	20		ns	
TARYLCL	AREADY Inactive Setup Time	35		ns	
TARYCHL	Asynchronous Ready Inactive Hold Time	15		ns	
TCHARYX	AREADY Hold Time	15		ns	
TSRYCL	Synchronous Ready (SREADY) Transition Setup Time	20		ns	
TCLSRY	SREADY Transition Hold Time	15		ns	
THVCL	HOLD Setup Time*	25		ns	
TINVCH	INTR, NMI, $\overline{TEST}$, TIMERIN, Setup Time*	25		ns	
TINVCL	DRQ0, DRQ1, Setup Time*	25		ns	

* To guarantee recognition at next clock.

A.C. CHARACTERISTICS (Continued)

MBL 80188 Master Interface Timing Responses

Symbol	Parameters	MBL 80188 (8 MHz)		MBL 80188-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	5	55	5	63	ns	C_L= 20–200 pF all outputs
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	35	TCLAX	44	ns	
TCHCZ	Command Lines Float Delay		45		56	ns	
TCHCV	Command Lines Valid Delay (after Float)		55		76	ns	
TLHLL	ALE Width	TCLCL-35		TCLCL-35		ns	
TCHLH	ALE Active Delay		35		44	ns	
TCHLL	ALE Inactive Delay		35		44	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-25		TCHCL-30		ns	
TCLDV	Data Valid Delay	10	44	10	55	ns	
TCLDOX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time after $\overline{\mathrm{WR}}$	TCLCL-40		TCLCL-50		ns	
TCVCTV	Control Active Delay 1	10	70	10	87	ns	
TCHCTV	Control Active Delay 2	10	55	10	76	ns	
TCVCTX	Control Inactive Delay	5	55	5	76	ns	
TCVDEX	$\overline{\mathrm{DEN}}$ Inactive Delay (Non-Write Cycle)	10	70	10	87	ns	
TAZRL	Address Float to $\overline{\mathrm{RD}}$ Active	0		0		ns	
TCLRL	$\overline{\mathrm{RD}}$ Active Delay	10	70	10	87	ns	
TCLRH	$\overline{\mathrm{RD}}$ Inactive Delay	10	55	10	76	ns	
TRHAV	$\overline{\mathrm{RD}}$ Inactive to Address Active	TCLCL-40		TCLCL-50		ns	
TCLHAV	HLDA Valid Delay	5	50	5	67	ns	
TRLRH	$\overline{\mathrm{RD}}$ Width	2TCLCL-50		2TCLCL-50		ns	
TWLWH	$\overline{\mathrm{WR}}$ Width	2TCLCL-40		2TCLCL-40		ns	
TAVAL	Address Valid to ALE Low	TCLCH-25		TCLCH-45		ns	
TCHSV	Status Active Delay	10	55	10	76	ns	
TCLSH	Status Inactive Delay	10	65	10	76	ns	
TCLTMV	Timer Output Delay		60		75	ns	100 pF max
TCLRO	Reset Delay		60		75	ns	
TCHQSV	Queue Status Delay		35		44	ns	
TCHDX	Status Hold Time	10		10		ns	
TAVCH	Address Valid to Clock High	10		10		ns	

MBL 80188 Chip-Select Timing Responses

Symbol	Parameter	MBL 80188 (8 MHz)		MBL 80188-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLCSV	Chip-Select Active Delay		66		80	ns	
TCXCSX	Chip-Select Hold Time from Command Inactive	35		35		ns	
TCHCSX	Chip-Select Inactive Delay	5	35	5	47	ns	

A.C. CHARACTERISTICS (Contiuned)

MBL 80188 CLKIN Timing Requirements

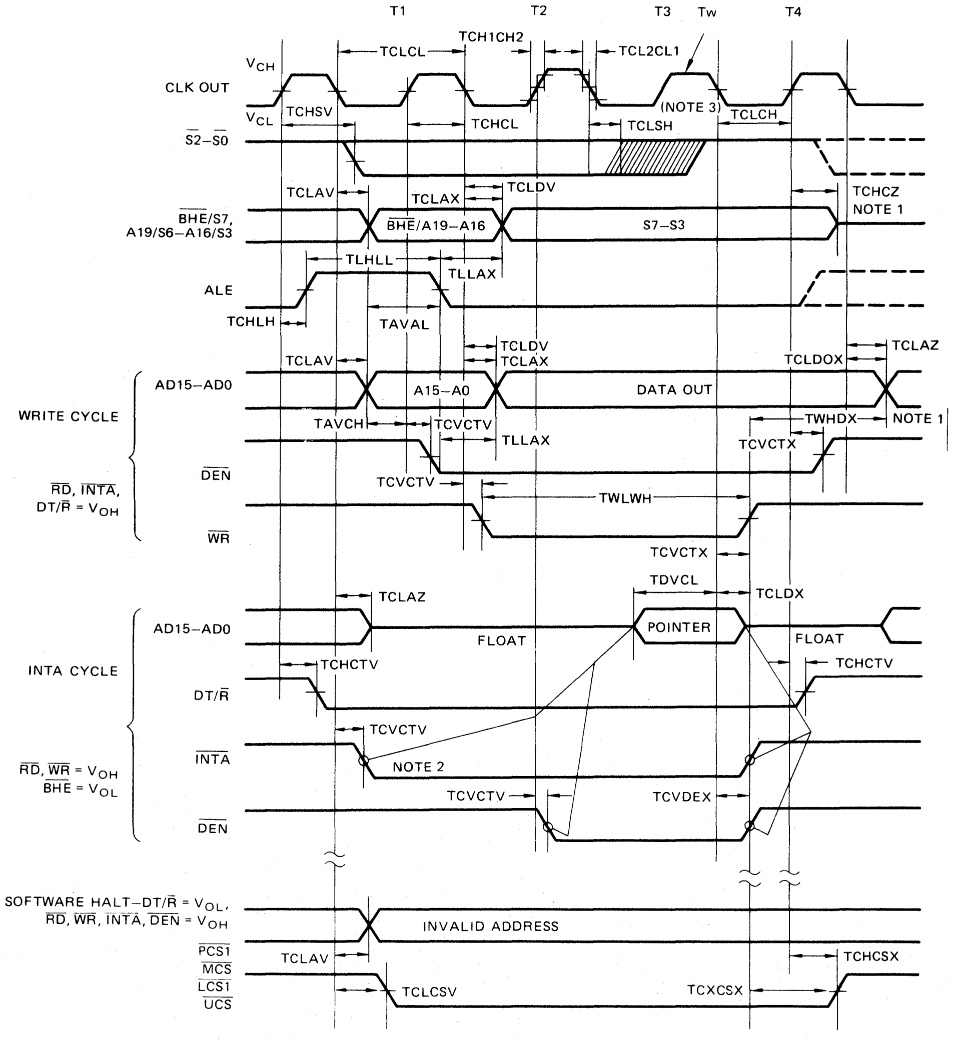
Symbol	Parameter	MBL 80188 (8 MHz)		MBL 80188-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCKIN	CLKIN Period	62.5	250	83	250	ns	
TCKHL	CLKIN Fall Time		10		10	ns	3.5 V to 1.0 V
TCKLH	CLKIN Rise Time		10		10	ns	1.0 V to 3.5 V
TCLCK	CLKIN Low Time	25		33		ns	1.5 V
TCHCK	CLKIN High Time	25		33		ns	1.5 V

MBL 80188 CLKOUT Timing Responses (200 pF load)

Symbol	Parameter	MBL 80188 (8 MHz)		MBL 80188-6 (6 MHz)		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCICO	CLKIN to CLKOUT Skew		50		62.5	ns	
TCLCL	CLKOUT Period	125	500	167	500	ns	
TCLCH	CLKOUT Low Time	½TCLCL-7.5		½TCLCL-7.5		ns	1.5 V
TCHCL	CLKOUT High Time	½TCLCL-7.5		½TCLCL-7.5		ns	1.5 V
TCH1CH2	CLKOUT Rise Time		15		15	ns	1.0 V to 3.5 V
TCL2CL1	CLKOUT Fall Time		15		15	ns	3.5 V to 1.0 V

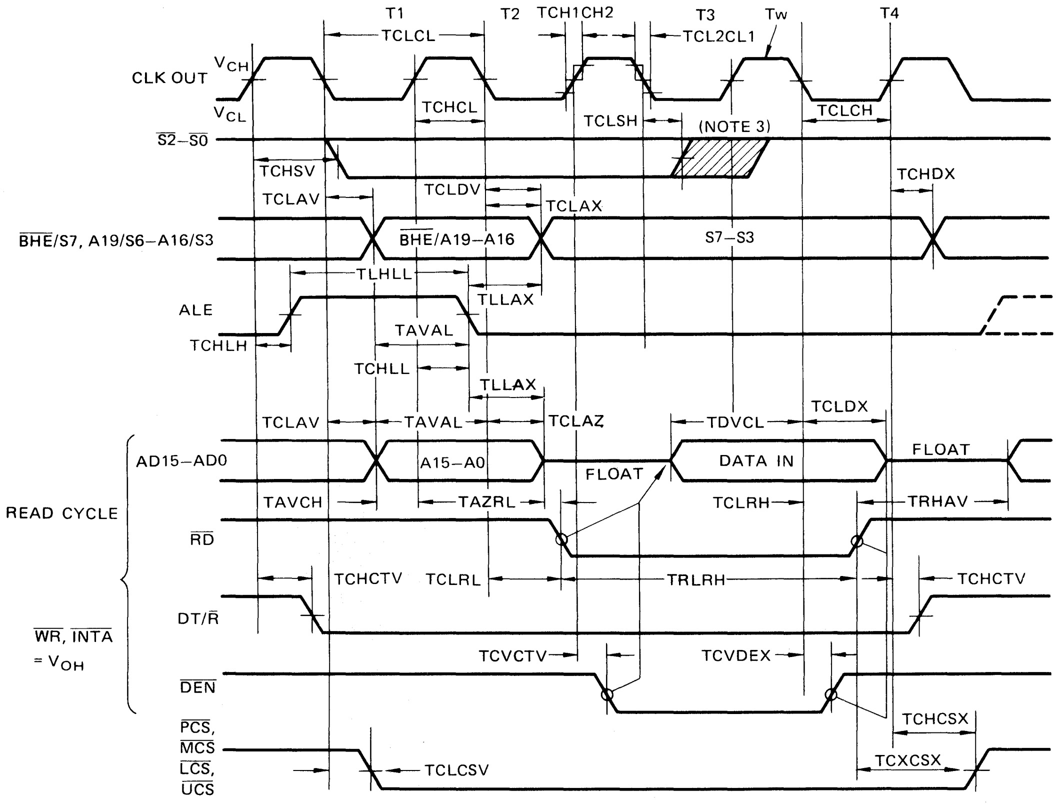
WAVEFORMS

MAJOR CYCLE TIMING



WAVEFORMS (Continued)

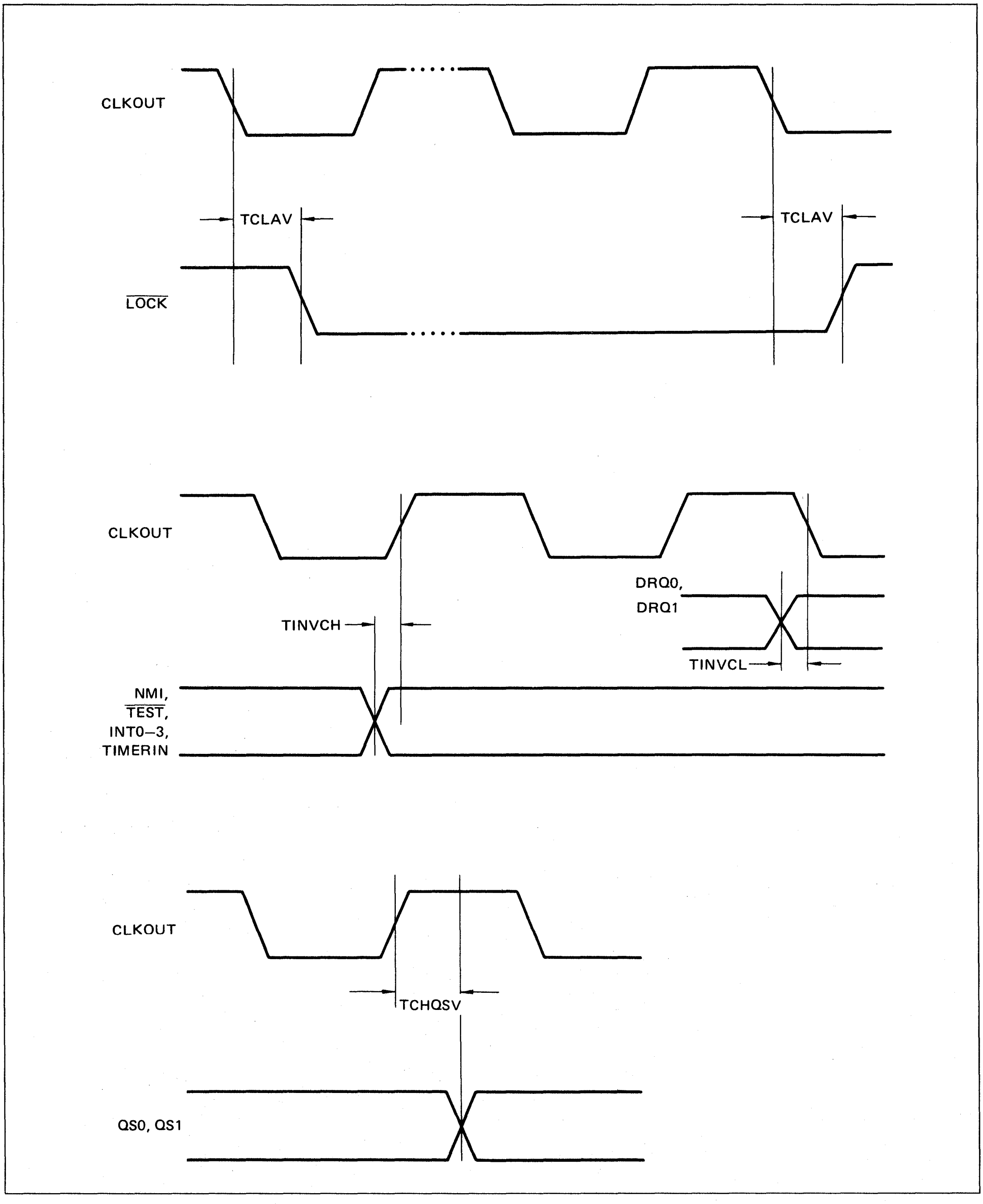
MAJOR CYCLE TIMING (Continued)



NOTES:

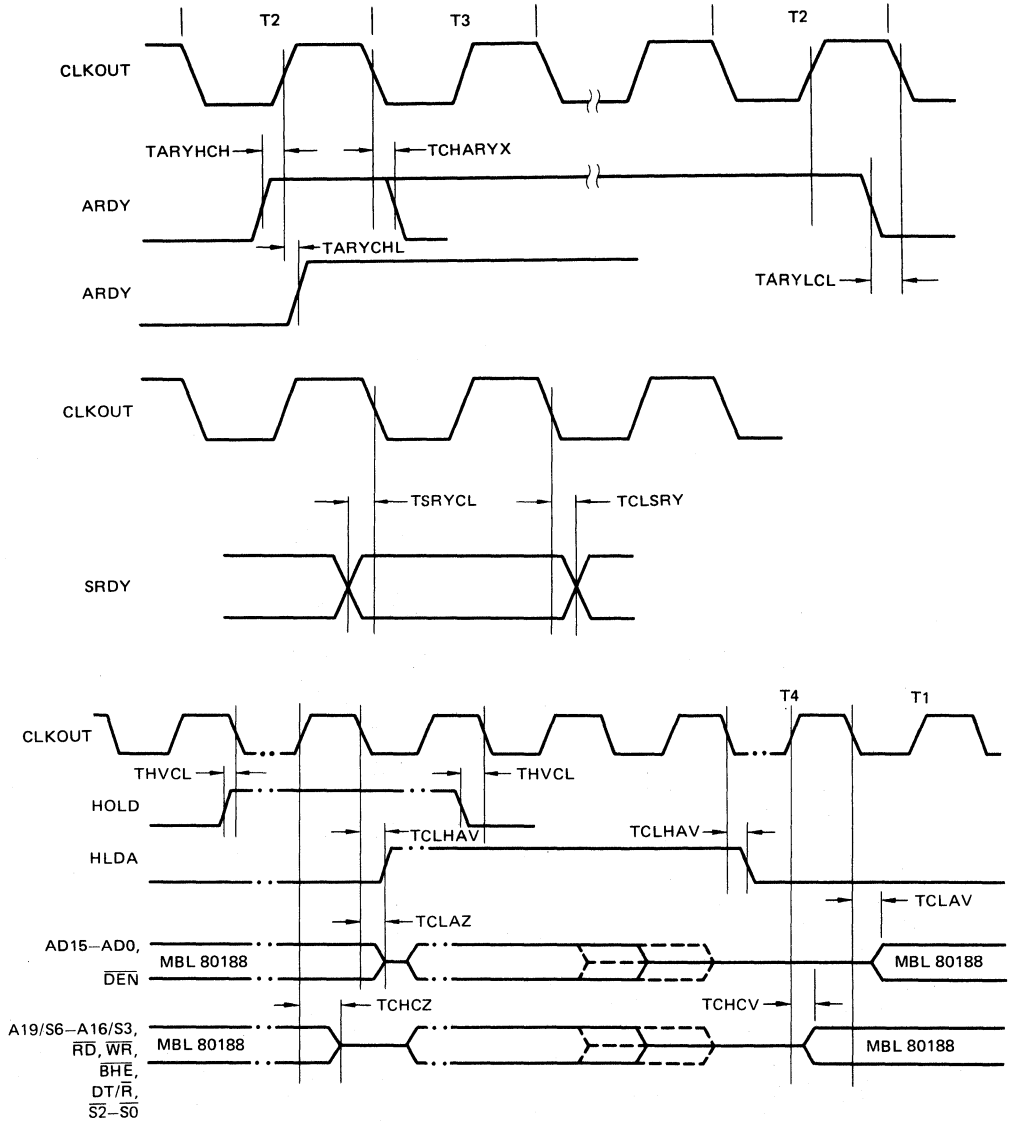
1. Following a Write cycle, the Local Bus is floated by the MBL 80188 only when the MBL 80188 enters a "Hold Acknowledge" state.
2. INTA occurs one clock later in iRMX-mode.
3. Status inactive just prior to T4.

WAVEFORMS (Continued)

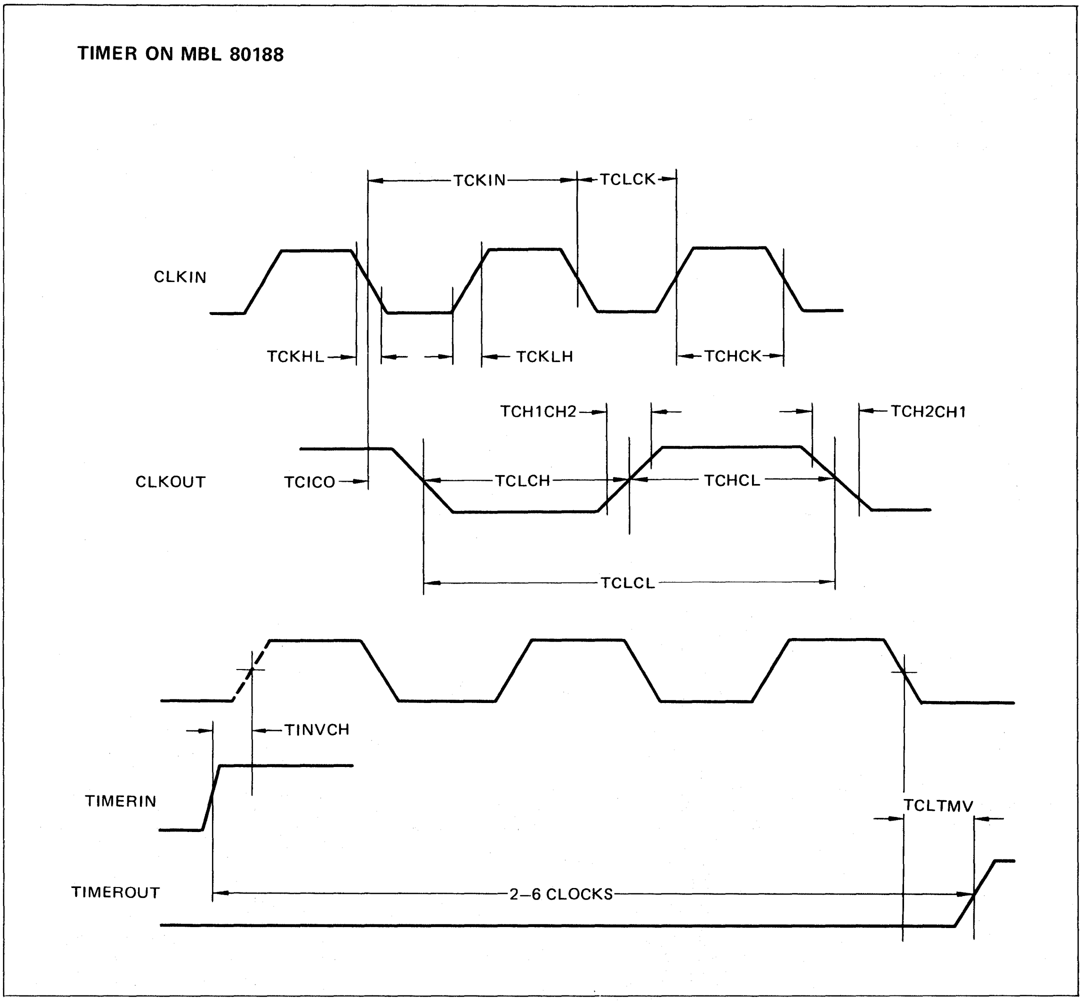


WAVEFORMS (Continued)

HOLD-HLDA TIMING



WAVEFORMS (Continued)



MBL 80188 INSTRUCTION TIMINGS

The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDS occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory reference can require one (and in some cases, two) additional clocks above the minimum timings shown. This is due to the asynchronous nature of the handshake between the BIU and the Execution unit.

INSTRUCTION SET SUMMARY

FUNCTION	FORMAT				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to register/memory	1 0 0 0 1 0 0 w	mod reg r/m			2/12*	
Register/memory to register	1 0 0 0 1 0 1 w	mod reg r/m			2/9*	
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 000 r/m	data	data if w = 1	12–13*	8/16-bit
Immediate to register	1 0 1 1 w reg	data	data if w = 1		3–4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high		9*	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high		8*	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m			2/13	
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m			2/15	
PUSH = Push:						
Memory	1 1 1 1 1 1 1 1	mod 110 r/m			20	
Register	0 1 0 1 0 reg				14	
Segment register	0 0 0 reg 1 1 0				13	
Immediate	0 1 1 0 1 0 s 0	data	data if s = 0		14	
PUSHA = Push All	0 1 1 0 0 0 0 0				68	
POP = Pop:						
Memory	1 0 0 0 1 1 1 1	mod 000 r/m			24	
Register	0 1 0 1 1 reg				14	
Segment register	0 0 0 reg 1 1 1	(reg ≠ 01)			12	
POPA = Pop All	0 1 1 0 0 0 0 1				83	
XCHG = Exchange:						
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m			4/17*	
Register with accumulator	1 0 0 1 0 reg				3	
IN = Input from:						
Fixed port	1 1 1 0 0 1 0 w	port			10*	
Variable port	1 1 1 0 1 1 0 w				8*	
OUT = Output to:						
Fixed port	1 1 1 0 0 1 1 w	port			9*	
Variable port	1 1 1 0 1 1 1 w				7*	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1				15	
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m			6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m	(mod ≠ 11)		26	
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m	(mod ≠ 11)		26	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1				2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0				3	
PUSHF = Push flags	1 0 0 1 1 1 0 0				13	
POPF = Pop flags	1 0 0 1 1 1 0 1				12	
SEGMENT = Segment Override						
CS	0 0 1 0 1 1 1 0				2	
SS	0 0 1 1 0 1 1 0				2	
DS	0 0 1 1 1 1 1 0				2	
ES	0 0 1 0 0 1 1 0				2	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w = 01	4/16*	
Immediate to accumulator	0000010w	data	data if w = 1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w = 01	4/16*	
Immediate to accumulator	0001010w	data	data if w = 1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15*	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w = 01	4/16*	
Immediate from accumulator	0010110w	data	data if w = 1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w = 01	4/16*	
Immediate from accumulator	0001110w	data	data if w = 1		3/4	8/16-bit
DEC = Decrement:						
Register/memory	1111111w	mod 001 r/m			3/15*	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10*	
Register with register/memory	0011100w	mod reg r/m			3/10*	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w = 01	3/10*	
Immediate with accumulator	0011110w	data	data if w = 1		3/4	8/16-bit
NEG = Change sign	1111011w	mod 011 r/m			3	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43*	
IMUL = Integer multiply (signed):	1111011w	mod 101 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43*	
IMUL = Integer immediate multiply (signed)	011010s1	mod reg r/m	data	data if s = 0	22–25/ 29–32*	
DIV = Divide (unsigned):	1111011w	mod 110 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44*	

Shaded areas a indicate instructions not available in MBL 8086, 88 microsystems.

*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
ARITHMETIC (Continued)						
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 1 1 1 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67*	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	
LOGIC						
Shift/Rotate Instructions:						
Register/memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15*	
Register/memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n*	
Register/memory by count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n*	
	TTT	**Instruction**				
	0 0 0	ROL				
	0 0 1	ROR				
	0 1 0	RCL				
	0 1 1	RCR				
	1 0 0	SHL/SAL				
	1 0 1	SHR				
	1 1 1	SAR				
AND = And:						
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 100 r/m	data	data if w = 1	4/16*	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1		3/4	8/16-bit
TEST = And function to flags, no result:						
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10*	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 000 r/m	data	data if w = 1	4/10*	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 001 r/m	data	data if w = 1	4/16*	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 110 r/m	data	data if w = 1	4/16*	
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	mod 010 r/m			3	
STRING MANIPULATION						
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14*	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w				22*	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15*	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12*	
STOS = Stor byte/wd from AL/A	1 0 1 0 1 0 1 w				10*	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w				14*	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14*	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
STRING MANIPULATION (Continued)						
Repeated by count in CX						
MOVS = Move string	11110010	1010010w			8 + 8n*	
CMPS = Compare string	1111001z	1010011w			5 + 22n*	
SCAS = Scan string	1111001z	1010111w			5 + 15n*	
LODS = Load string	11110010	1010110w			6 + 11n*	
STOS = Store string	11110010	1010101w			6 + 9n*	
INS = Input string	11110010	0110110w			8 + 8n*	
OUTS = Output string	11110010	0110111w			8 + 8n*	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		19	
Register/memory indirect within segment	11111111	mod 010 r/m			17/27	
Direct intersegment	10011010	segment offset			31	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m		(mod ≠ 11)	54	
JMP = Unconditional jump:						
Short long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register memory indirect within segment	11111111	mod 100 r/m			11/21	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m		(mod ≠ 11)	34	
RET = Return from CALL:						
Within segment	11000011				20	
Within seg adding immed to SP	11000010	data-low	data-high		22	
Intersegment	11001011				30	
Intersegment adding immediate to SP	11001010	data-low	data-high		33	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	
INTO = Interrupt on overflow	11001110				48/4	if INT.taken/ if INT. not taken
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33 – 35	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	1 1 1 1 1 0 0 0	2	
CMC = Complement carry	1 1 1 1 0 1 0 1	2	
STC = Set carry	1 1 1 1 1 0 0 1	2	
CLD = Clear direction	1 1 1 1 1 1 0 0	2	
STD = Set direction	1 1 1 1 1 1 0 1	2	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	2	
STI = Set interrupt	1 1 1 1 1 0 1 1	2	
HLT = Halt	1 1 1 1 0 1 0 0	2	
WAIT = Wait	1 0 0 1 1 0 1 1	6	if $\overline{\text{test}}$ = 0
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	2	
ESC = Processor extension escape	1 1 0 1 1 T T T | mod LLL r/m (TTT LLL are opcode to processor extension)	6	

Shaded areas indicate instructions not available in MBL 8086, 88 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if/r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

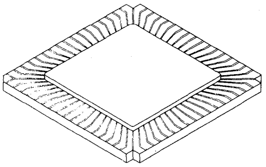
REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

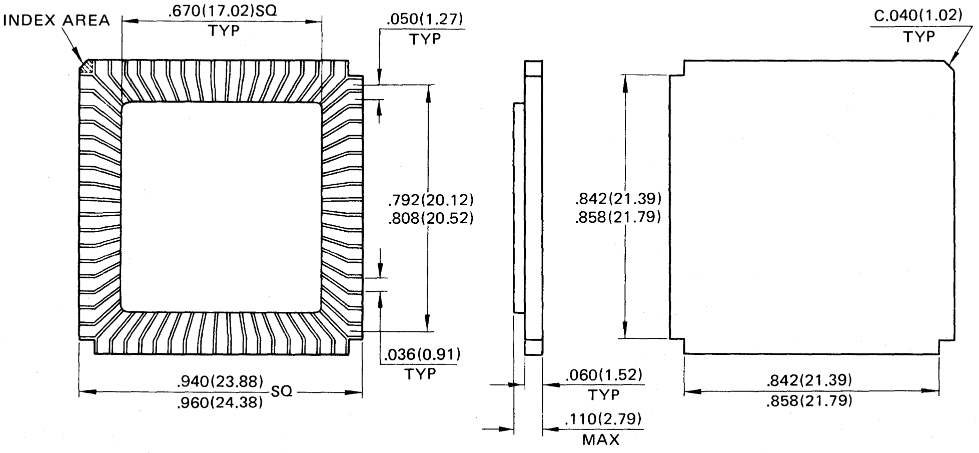
PACKAGE ILLUSTRATION

CERAMIC LCC
(METAL SEAL)



PACKAGE DIMENSIONS (Suffix -CV)

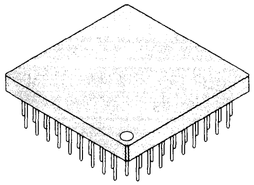
68-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-68C-A01)



Dimension in
inches (millimeters)

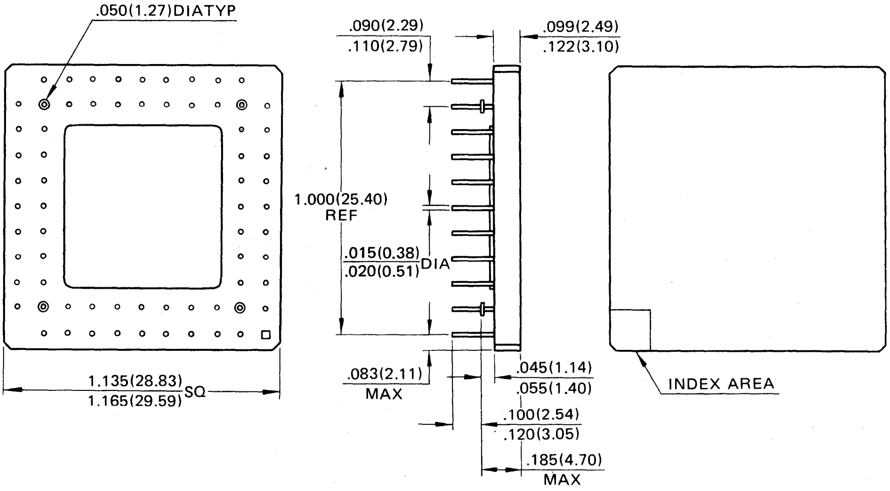
PACKAGE ILLUSTRATION

CERAMIC PGA
(METAL SEAL)



PACKAGE DIMENSIONS (Suffix -CR)

68-LEAD CERAMIC (METAL SEAL)
REPEATED QUAD IN-LINE PACKAGE
(CASE No.: RIT-68C-A01)



Dimensions in
inches (millimeters)

FUJITSU

NMOS 8-BIT MICROPROCESSOR

MBL 8088
MBL 8088-2
MBL 8088-1

February 1985
Edition 4.0

NMOS 8-BIT MICROPROCESSOR

The Fujitsu MBL 8088 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (NMOS), and packaged in a 40-pin ceramic or plastic DIP. The processor has attributes of both 8- and 16-bit microprocessors. It is directly compatible with MBL 8086 software and Intel 8080/8085 hardware and peripherals.

- **8-Bit Data Bus Interface**
- **16-Bit Internal Architecture**
- **Direct Addressing Capability to 1 Mbyte of Memory**
  Direct Software Compatibility with MBL 8086 CPU
  14-Word by 16-Bit Register Set with Symmetrical Operations
- **24 Operand Addressing Modes**
- **Byte, Word, and Block Operations**
- **8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide**
- **Compatible with 8155-2, 8755A-2 and 8185-2 Multiplexed Peripherals**
- **Two Clock Rates:**
  5MHz for MBL 8088,
  8MHz for MBL 8088-2,
  10MHz for MBL 8088-1
- **40-Pin DIP:**
  Ceramic DIP (Suffix: -C)
  Plastic DIP (Suffix: -P)

Fig. 1 – BLOCK DIAGRAM

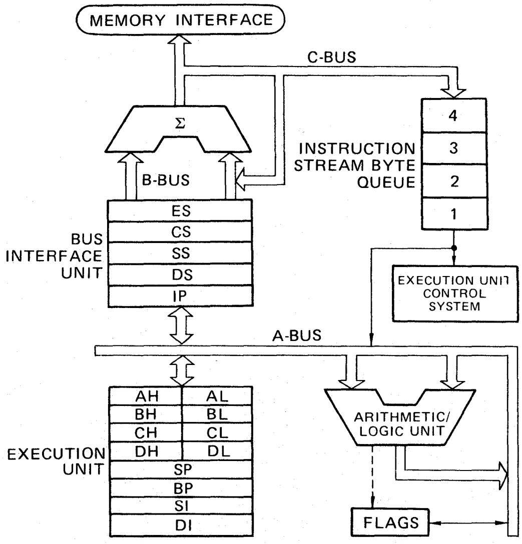


Fig. 2 – PIN CONFIGURATION

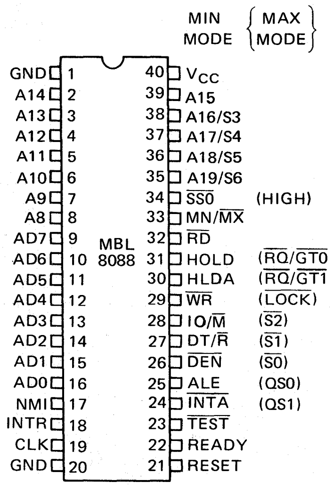


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TABLE 1 — PIN DESCRIPTION

The following pin function descriptions are for MBL 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the MBL 8088 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>AD_7–AD_0</td><td>9-16</td><td>I/O</td><td><b>Address Data Bus:</b> These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, Tw, and T_4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A_{15}–A_8</td><td>2-8, 39</td><td>O</td><td><b>Address Bus:</b> These lines provide address bits 8 through 15 for the entire bus cycle (T_1–T_4). These lines do not have to be latched by ALE to remain valid. A_{15} – A_8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A_{19}/S_6,
A_{18}/S_5,
A_{17}/S_4,
A_{16}/S_3</td><td>35-38</td><td>O</td><td><b>Address/Status:</b> During T_1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is avalable on these lines during T_2, T_3, Tw, and T_4. S_6 is always low. The status of the interrupt enable flag bit (S_5) is updated at the beginning of each clock cycle. S_4 and S_3 are encoded as shown.
This information indicates which segment register is presently being used for data accessing.
These lines float to 3-state OFF during local bus "hold acknowledge".
<table>
<tr><th>S_4</th><th>S_3</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S_6 is 0 (LOW)</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td><b>Read:</b> Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S_2. This signal is used to read devices which reside on the MBL 8088 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and Tw of any read cycle, and is guaranteed to remain HIGH in T_2 until the MBL 8088 local bus has floated.
This signal floats to 3-state OFF in "hold acknowledge".</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td><b>READY:</b> is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the MBL 8284A clock generator to form READY. This signal is active HIGH. The MBL 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td><b>Interrupt Request:</b> is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</td></tr>
<tr><td>$\overline{TEST}$</td><td>23</td><td>I</td><td><b>$\overline{TEST}$:</b> input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</td></tr>
<tr><td>NMI</td><td>17</td><td>I</td><td><b>Non-Maskable Interrupt:</b> is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.</td></tr>
</table>

TABLE 1 — PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name and Function
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**Clock:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC} :** is the +5V ±10% power supply pin.
GND	1, 20		**GND:** are the ground pins.
MN/$\overline{\text{MX}}$	33	I	**Minimum/Maximum:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the MBL 8088 minimum mode (i.e., MN/$\overline{\text{MX}}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

IO/$\overline{\text{M}}$	28	O	**Status Line:** is an inverted maximum mode $\overline{S_2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{\text{M}}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (I/O=HIGH, $\overline{\text{M}}$=LOW). IO/$\overline{\text{M}}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{\text{WR}}$	29	O	**Write:** strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{\text{M}}$ signal. $\overline{\text{WR}}$ is active for T_2, T_3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{\text{INTA}}$	24	O	**INTA:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3, and Tw of each interrupt acknowledge cycle.
ALE	25	O	**Address Latch Enable:** is provided by the processor to latch the address into the MBL 8282/8283 address latch. It is a HIGH pulse active during clock low of T_1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{\text{R}}$	27	O	**Data Transmit/Receive:** is needed in a minimum system that desires to use an MBL 8286/8287 data bus transceiver. It is used to control to direction of data flow through the transceiver. Logically, DT/$\overline{\text{R}}$ is equivalent to S_1 in the maximum mode, and its timing is the same as for IO/$\overline{\text{M}}$ (T=HIGH, $\overline{\text{R}}$=LOW). This signal floats to 3-state OFF in local "hold acknowledge".
$\overline{\text{DEN}}$	26	O	**Data Enable:** is provided as an output enable for the MBL 8286/8287 in a minimum system which uses the transceiver. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access, and for $\overline{\text{INTA}}$ cycles. For a read or $\overline{\text{INTA}}$ cycle, it is active from the middle of T_2 until the middle of T_4, while for a write cycle, it is active from the beginning of T_2 until the middle of T_4. $\overline{\text{DEN}}$ floats to 3-state OFF during local bus "hold acknowledge".
HOLD, HLDA	30, 31	I, O	**HOLD:** indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T_4 or T_1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.

TABLE 1 — PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{SSO}$</td><td>34</td><td>O</td><td><b>Status line:</b> is logically equivalent to $\overline{SO}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.
<table>
<tr><th>IO/$\overline{M}$</th><th>DT/$\overline{R}$</th><th>$\overline{SSO}$</th><th>Characteristics</th></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
</table>

The following pin function descriptions are for the MBL 8088, 8228 system in maximum mode (i.e., MN/$\overline{MX}$=GND.) Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

<table>
<tr><td>$\overline{S2}$, $\overline{S1}$, $\overline{S0}$</td><td>26-28</td><td>O</td><td><b>Status:</b> is active during clock high of T_4, T_1, and T_2, and is returned to the passive state (1,1,1) during T_3 or during Tw when READY is HIGH. This status is used by the MBL 8288 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or Tw is used to indicate the end of a bus cycle.
These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock they float to 3-state OFF.
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}/\overline{GT0}$,
$\overline{RQ}/\overline{GT1}$</td><td>30, 31</td><td>I/O</td><td><b>Request/Grant:</b> pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor, so may be left unconnected. The request/grant sequence is as follows (See Fig. 8):
1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the MBL 8088 (pulse 1).
2. During a T_4 or T_1 clock cycle, a pulse one clock wide from the MBL 8088 to the requesting master (pulse 2), indicates that the MBL 8088 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released.
3. A pulse one CLK wide from the requesting master indicates to the MBL 8088 (pulse 3) that the "hold" request is about to end and that the MBL 8088 can reclaim the local bus at the next CLK. The CPU then enters T_4.</td></tr>
</table>

TABLE 1 – PIN DESCRIPTION (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{\text{RQ/GT0}}$,
$\overline{\text{RQ/GT1}}$</td><td>30, 31</td><td>I/O</td><td>Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:
1. Request occurs on or before T_2.
2. Current cycle is not the low byte of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>29</td><td>O</td><td>$\overline{\text{LOCK}}$: indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active (LOW). The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge".</td></tr>
<tr><td>QS1, QS0</td><td>24, 25</td><td>O</td><td><b>Queue Status:</b> provide status to allow external tracking of the internal MBL 8088 instruction queue.
The queue status is valid during the CLK cycle after which the queue operation is performed.
<table>
<tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>No operation</td></tr>
<tr><td>0</td><td>1</td><td>First byte of opcode from queue</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Empty the queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent byte from queue</td></tr>
</table></td></tr>
<tr><td>–</td><td>34</td><td>O</td><td>Pin 34 is always high in the maximum mode.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Fig. 3.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. (See Fig. 4.) Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Fig. 3 – MEMORY ORGANIZATION

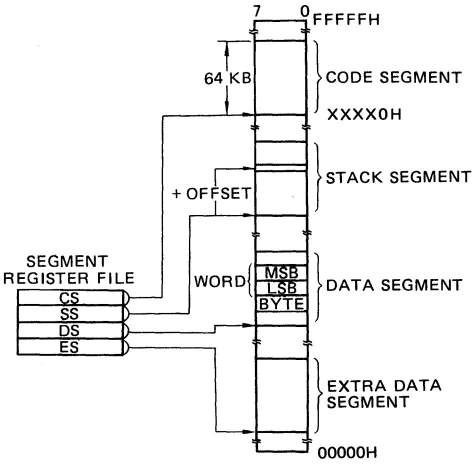
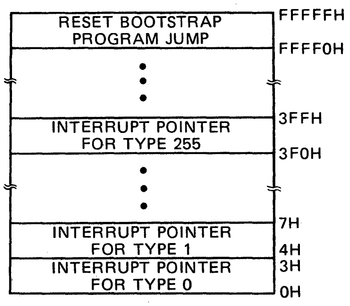


Fig. 4 – RESERVED MEMORY LOCATIONS


RESET BOOTSTRAP PROGRAM JUMP
FFFFFH
FFFF0H
INTERRUPT POINTER FOR TYPE 255
3FFH
3F0H
INTERRUPT POINTER FOR TYPE 1
7H
4H
INTERRUPT POINTER FOR TYPE 0
3H
0H

MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum MBL 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the MBL 8088 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the MBL 8088 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the MBL 8088 generates bus control signals itself on pins 24 through 31 and 34.

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicity overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicity selected using a segment override.

The minimum mode MBL 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the MCS-85* multiplexed bus peripherals (Intel 8155, 8156, 8355, 8755A, and 8185). This configuration (See Fig. 5.) provides the user with a minimum chip count system. This architecture provides the MBL 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. An MBL 8286 or MBL 8287 transceiver can also be used if data bus buffering is required. (See Fig. 6.) The MBL 8088 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the MBL 8288 bus controller. (See Fig. 7.) The MBL 8288 decodes status lines $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$, and provides the system with all bus control signals. Moving the bus control to the MBL 8288 provides better source and sink current capability to the control lines, and frees the MBL 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the MBL 8088 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

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Fig. 5 – MULTIPLEXED BUS CONFIGURATION

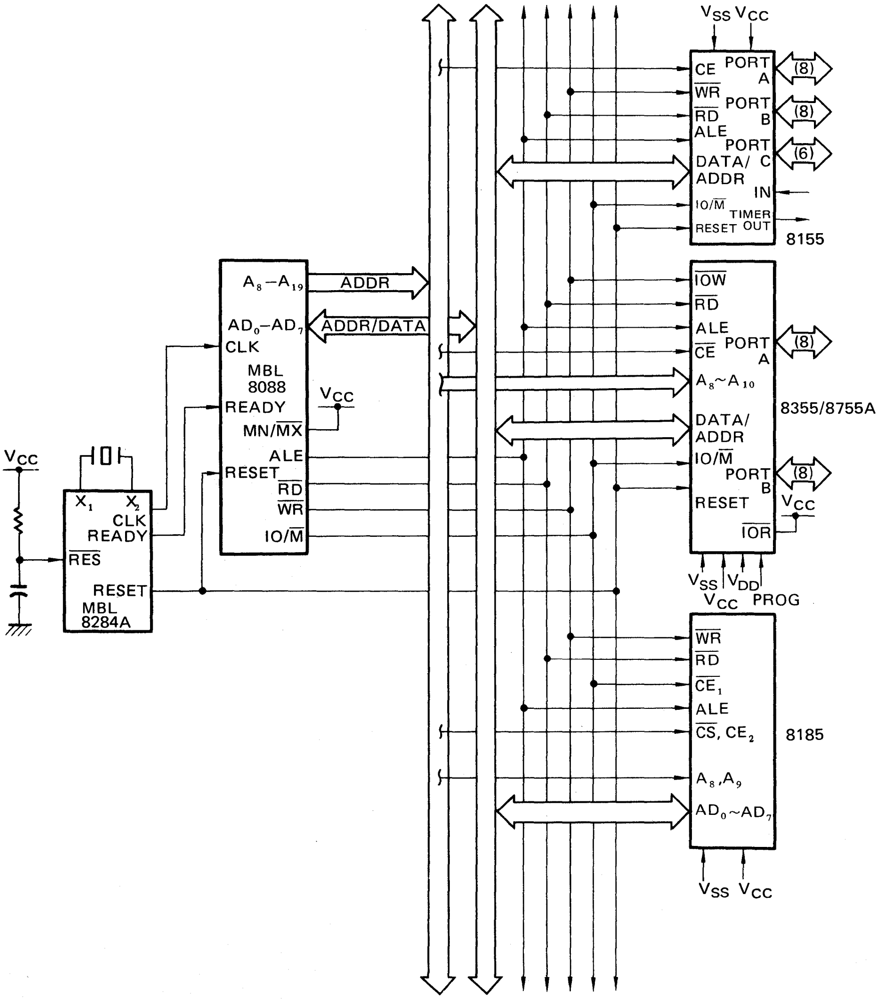


Fig. 6 – DEMULTIPLEXED BUS CONFIGRATION EXAMPLES (MINIMUM MODE)

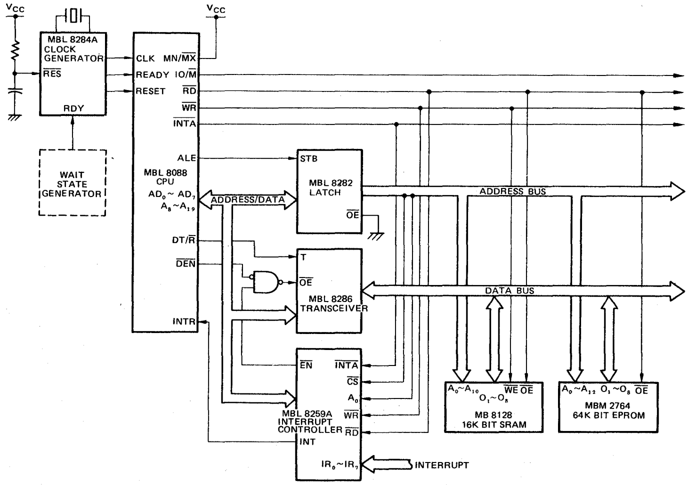
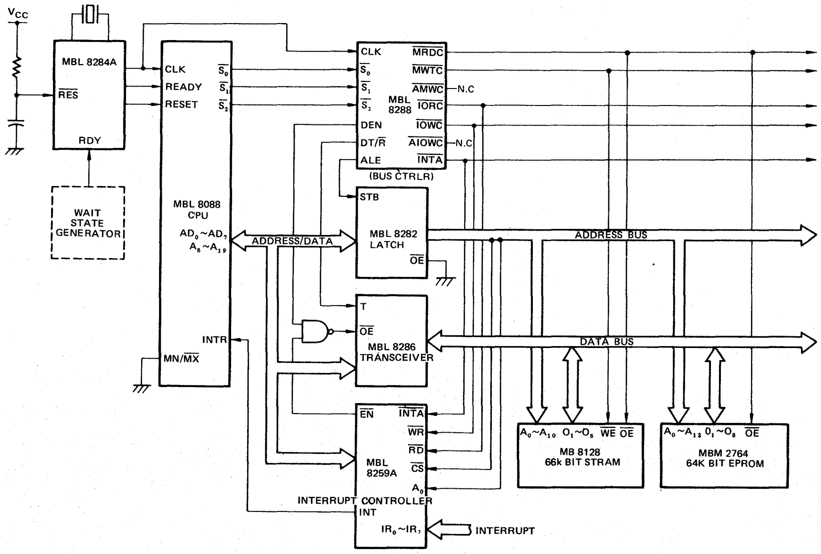


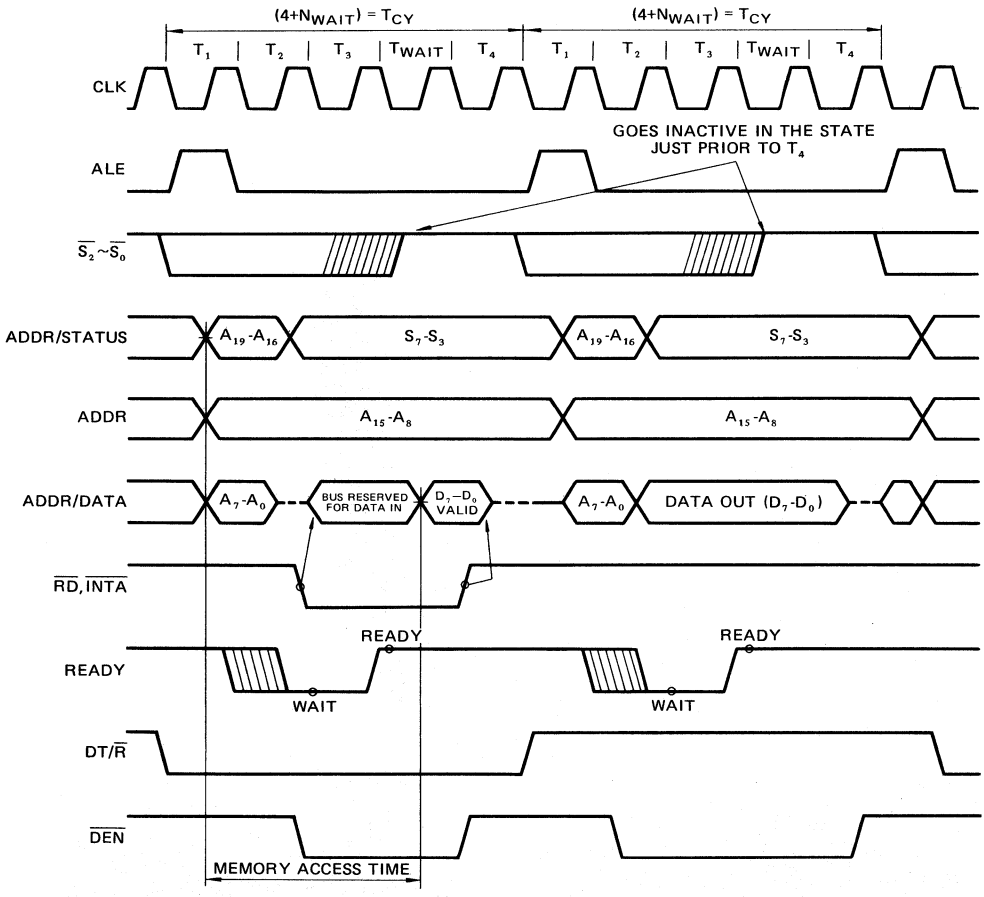
Fig. 7 – FULLY BUFFERED SYSTEM EXAMPLE (MAXIMUM MODE)



BUS OPERATION

The MBL 8088 address/data bus is broken into three parts – the lower eight address/data bits (AD_0–AD_7), the middle eight address bits (A_8 – A_{15}), and the upper four address bits (A_{16} –A_{19}). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Fig. 8 – BASIC SYSTEM TIMING



Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3, and T_4. (See Fig. 8). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (Tw) are inserted between T_3 and T_4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between MBL 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the MBL 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (Low)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (High)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S_3 through S_6 are multiplexed with high order address bits and are therefore valid during T_2 through T_4, S_3 and S_4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S_4	S_3	CHARACTERISTICS
0 (Low)	0	Alternate Data (Extra Segment)
0	1	Stack
1 (High)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. S_6 is always equal to 0.

I/O ADDRESSING

In the MBL 8088, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines $A_{15}-A_0$. The address lines $A_{19}-A_{16}$ are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the Intel 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The MBL 8088 uses a full 16-bit address on its lower 16 address lines.

EXTERNAL INTERFACF

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The MBL 8088 RESET is required to be HIGH for greater than four clock cycles. The MBL 8088 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the MBL 8088 operates normally, beginning with the instruction in absolute location FFFFOH. (See Fig. 4.) The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50 μs after power up, to allow complete initialization of the MBL 8088.

If INTR is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description in the MBL 8086 Family

User's Manual. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Fig. 4), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any higher going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The MBL 8088 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (See Fig. 9), the processor executes two successive (back to back) interrupt acknowledge cycles. The MBL 8088 emits the LOCK signal (maximum mode only) from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., MBL 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

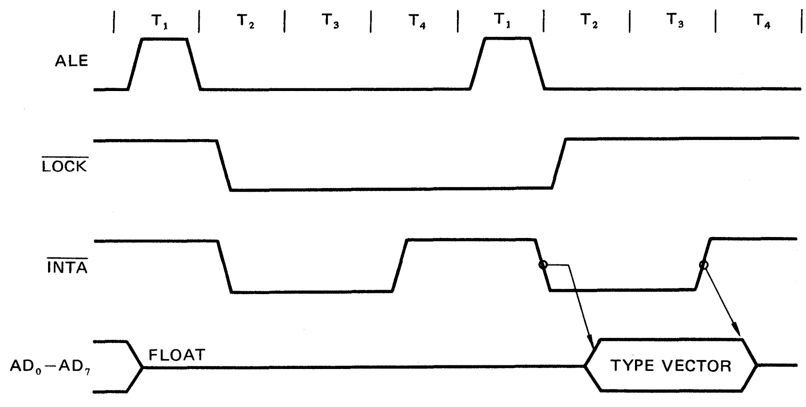
HALT

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on $IO/\overline{M}$, $DT/\overline{R}$, and $\overline{SSO}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$, and the MBL 8288 bus controller issues one ALE. The MBL 8088 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the MBL 8088 out of the HALT state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the LOCK prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the LOCK prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded, and then honored at the end of the $\overline{LOCK}$.

Fig. 9 – INTERRUPT ACKNOWLEDGE SEQUENCE



EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to interrupts, the MBL 8088 provides a single software-testable input pin (TEST). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the TEST input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the MBL 8088 3-states all output drivers. If interrupts are enabled, the MBL 8088 will recognize interrupts and process them. The WAIT instruction is then refetched, and reexecuted.

BASIC SYSTEM TIMING

In minimum mode, the NM/MX pin is strapped to V_{CC} and the processor emits bus control signals compatible with the 8085 bus structure. In maximum mode, the MN/MX pin is strapped to GND and the processor emits coded status information which the MBL 8288 bus controller uses to generate MULTIBUS* compatible bus control signals.

SYSTEM TIMING – MINIMUM SYSTEM

(See Fig. 8)

The read cycle begins in T_1 with the assertion of the address latch enable (ALE) signal. The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD_0–AD_7) at this time, into the MBL 8282/8283 latch. Address lines A_8 through A_{15} do not need to be latched because they remain valid throughout the bus cycle. From T_1 to T_4 the IO/M signal indicates a memory or I/O operation. At T_2 the address is removed from the address/data bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2. The read (RD) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (MBL 8286/8287) is required to buffer the MBL 8088 local bus, signals DT/R and DEN are provided by the MBL 8088.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/M signal is again asserted to indicate a memory or I/O write operation. In T_2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T_4. During T_2, T_3, and T_W, the processor asserts the write control signal. The write (WR) signal becomes active at the beginning of T_2, as opposed to the read, which is delayed somewhat into T_2 to provide time for the bus to float.

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The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{\text{INTA}}$) signal is asserted in place of the read ($\overline{\text{RD}}$) signal and the address bus is floated. (See Fig. 9.) In the second of two successive $\overline{\text{INTA}}$ cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e. MBL 8259A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

BUS TIMING – MEDIUM COMPLEXITY SYSTEMS

(See Fig. 10)

For medium complexity systems, the MN/$\overline{\text{MX}}$ pin is connected to GND and the MBL 8288 bus controller is added to the system, as well as an MBL 8282/8283 latch for latching the system address, and an MBL 8286/8287 transceiver to allow for bus loading greater than the MBL 8088 is capable of handling. Signals ALE, $\overline{\text{DEN}}$, and DT/$\overline{\text{R}}$ are generated by the MBL 8288 instead of the processor in this configuration, although their timing remains relatively the same. The MBL 8088 status outputs ($\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$) provide type of cycle information and become MBL 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The MBL 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The MBL 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The MBL 8286/8287 transceiver receives the usual T and $\overline{\text{OE}}$ inputs from the MBL 8288's DT/$\overline{\text{R}}$ and $\overline{\text{DEN}}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{\text{INTA}}$ cycle, can derive from an MBL 8259A located on either the local bus or the system bus. If the master MBL 8259A priority interrupt controller is positioned on the local bus, a TTL gate is required to disable the MBL 8286/8287 transceiver when reading from the master MBL 8259A during the interrupt acknowledge sequence and knowledge sequence and software "poll".

THE MBL 8088 COMPARED TO THE MBL 8086

The MBL 8088 CPU is an 8-bit processor designed around the MBL 8086 internal structure. Most internal functions of the MBL 8088 are identical to the equivalent MBL 8086 functions. The MBL 8088 handles the external bus the same way the MBL 8086 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the MBL 8088 and MBL 8086 are outlined below. The engineer who is unfamiliar with the MBL 8086 is referred to the MBL 8086 Family User's Manual, Chapters 2 and 4, for function description and instruction set information.

Internally, there are three differences between the MBL 8088 and the MBL 8086. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the MBL 8088, whereas MBL 8086 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The MBL 8088 BIU will fetch a new instruction to load into the queue each time there is a 1 byte hole (space available) in the queue. The MBL 8086 waits until a 2-byte space is available.
- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the MBL 8088 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

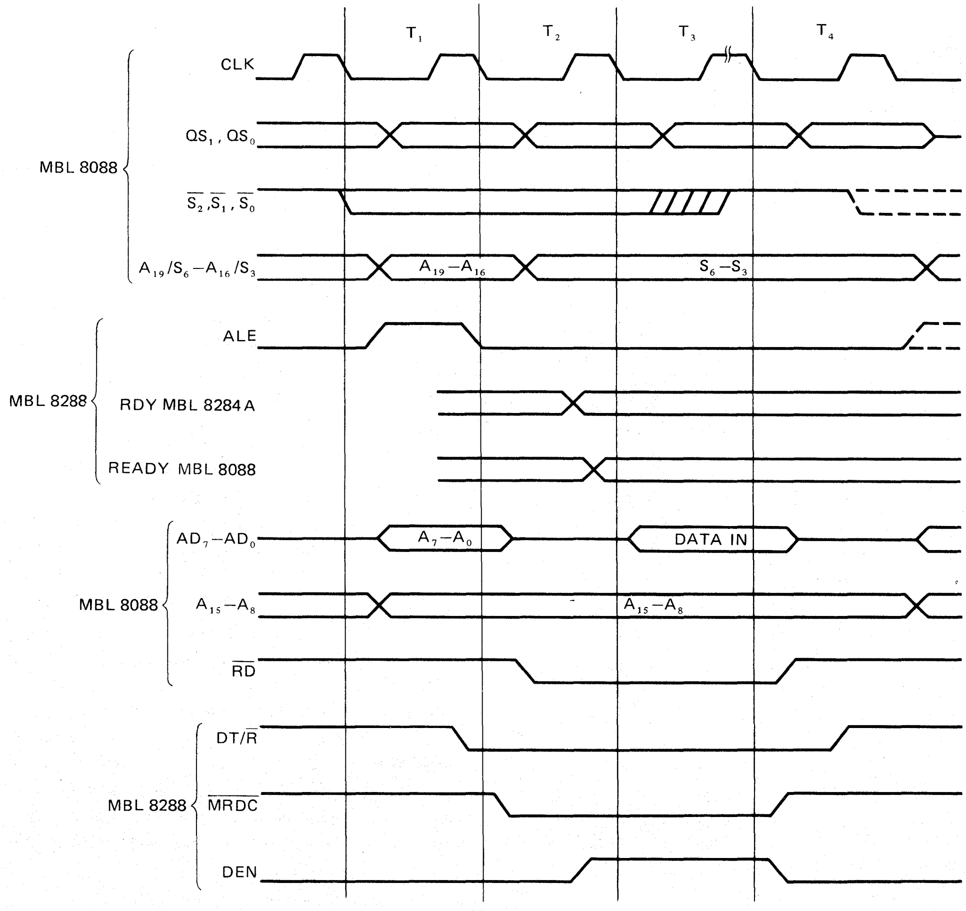
The MBL 8088 and MBL 8086 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an MBL 8088 or an MBL 8086.

The hardware interface of the MBL 8088 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A_8–A_{15} – These pins are only address outputs on the MBL 8088. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{\text{BHE}}$ has no meaning on the MBL 8088 and has been eliminated.

- $\overline{SSO}$ provides the $\overline{SO}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{R}$, IO/$\overline{M}$, and $\overline{SSO}$ provide the complete bus status in minimum mode.
- IO/$\overline{M}$ has been inverted to be compatible with the MCS-85* bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

Fig. 10 – MEDIUM COMPLEXITY SYSTEM TIMING



*Trade Mark of Intel Corporation, USA

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5 to +7V
Power Dissipation	2.5 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (MBL 8088: V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

(MBL 8088-2: V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)
(MBL 8088-1: V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
I_{CC}	Power Supply Current: MBL 8088 MBL 8088-2 MBL 8088-1		340 350 360	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
V_{CL}	Clock Input Low Voltage	-0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Input Buffer (All input except AD_0–AD_7 $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0–AD_7 $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz

A.C. CHARACTERISTICS (MBL 8088: V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

(MBL 8088-2: V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)
(MBL 8088-1: V_{CC} = 5 V ± 5% T_A = 0°C to 70°C)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

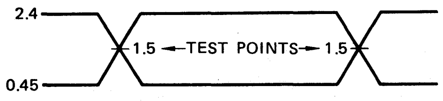
Symbol	Parameter	MBL 8088		MBL 8088-2		MBL 8088-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	100	500	ns	
TCLCH	CLK Low Time	118		68		53		ns	
TCHCL	CLK High Time	69		44		39		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0 V to 3.5 V
TCL2CL2	CLK Fall Time		10		10		10	ns	From 3.5 V to 1.0 V
TDVCL	Data in Setup Time	30		20		5		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into MBL 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into MBL 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into MBL 8088	118		68		53		ns	
TCHRYX	READY Hold Time into MBL 8088	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		-8		-10		ns	
THVCH	HOLD Setup Time	35		20		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8 V to 2.0 V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0 V to 0.8 V

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

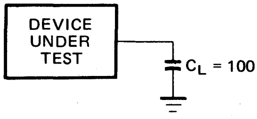
Symbol	Parameter	MBL 8088		MBL 8088-2		MBL 8088-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	10	110	10	60	10	50	ns	C_L=20–100pF for all MBL 8088 Outputs in addition to interna internal loads
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	10		ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		TCLCH−10		ns	
TCLLH	ALE Active Delay		80		50		40	ns	
TCHLL	ALE Inactive Delay		85		55		45	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	60	10	50	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH−30		TCLCH−30		TCLCH−25		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	10	50	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	10	45	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	10	50	ns	
TAZRL	Address Float to READ Active	0		0		0		ns	
TCLRL	RD Active Delay	10	165	10	100	10	70	ns	
TCLRH	RD Inactive Delay	10	150	10	80	10	60	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL−45		TCLCL−40		TCLCL−35		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	10	60	ns	
TRLRH	RD Width	2TCLCL−75		2TCLCL−50		2TCLCL−40		ns	
TWLWH	WR Width	2TCLCL−60		2TCLCL−40		2TCLCH−35		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−40		TCLCH−35		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8 V to 2.0 V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0 V to 0.8 V

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". THE CLOCK IS DRIVEN AT 4.3V AND 0.25V TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0".

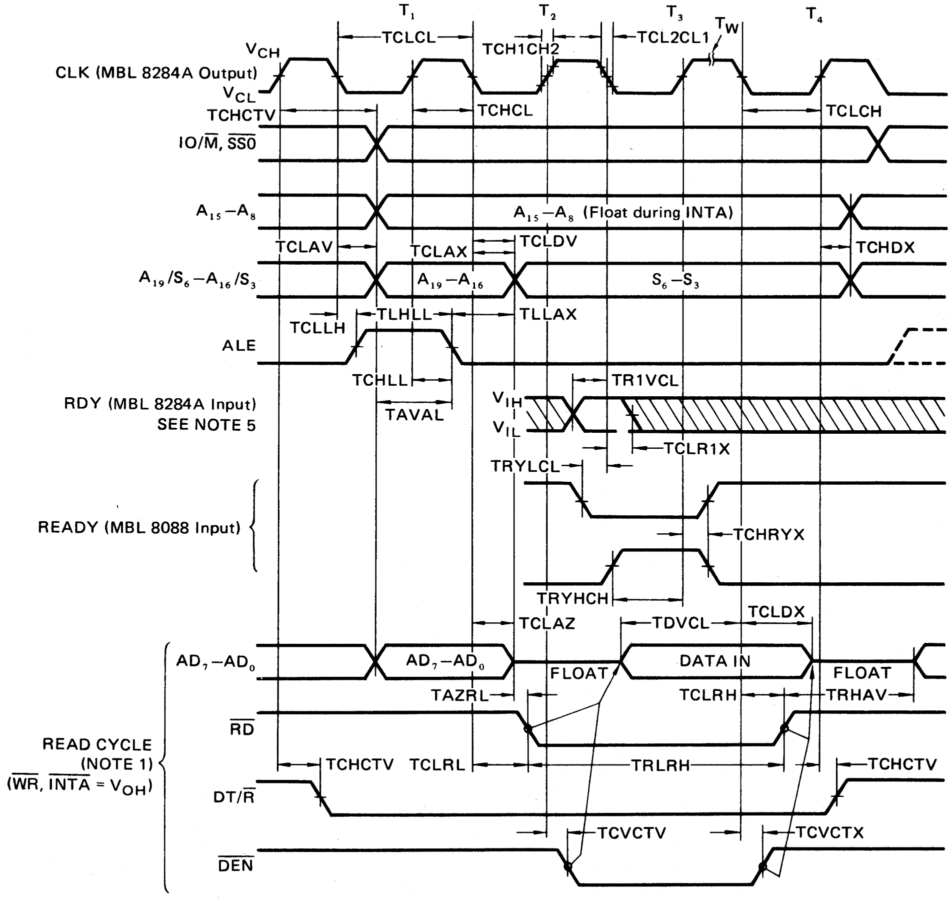
A.C. TESTING LOAD CIRCUIT



C_L: INCLUDES JIG CAPACITANCE

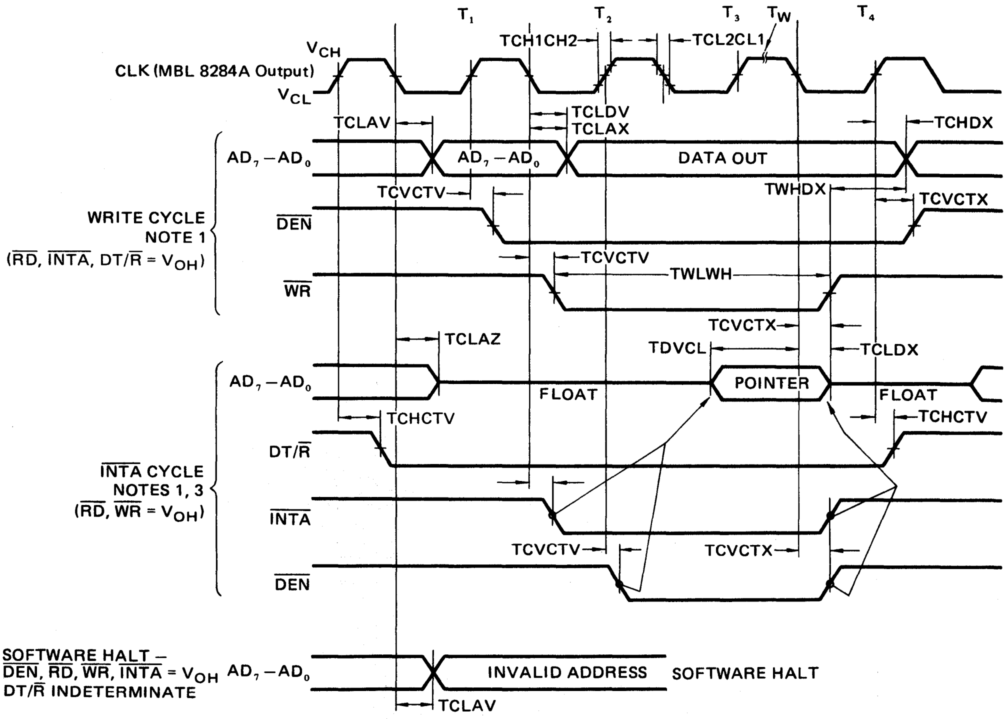
WAVEFORMS

BUS TIMING – MINIMUM MODE SYSTEM



WAVEFORMS (Continued)

BUS TIMING – MINIMUM MODE SYSTEM (Continued)



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE MBL 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT MBL 8284A ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

A.C. CHARACTERISTICS (Continued)

MAX MODE SYSTEM (USING MBL 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	MBL 8088		MBL 8088-2		MBL 8088-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	100	500	ns	
TCLCH	CLK Low Time	118		68		53		ns	
TCHCL	CLK High Time	69		44		39		ns	
TCH1CH2	CLK Rise Time		10		10		10	ns	From 1.0 V to 3.5 V
TCL2CL1	CLK Fall Time		10		10		10	ns	From 3.5 V to 1.0 V
TDVCL	Data in Setup Time	30		20		5		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into MBL 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into MBL 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into MBL 8088	118		68		53		ns	
TCHRYX	READY Hold Time into MBL 8088	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 2)	-8		-8		-10		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (See Note 2)	30		15		15		ns	
TGVCH	RQ/GT Setup Time	30		15		12		ns	
TCHGX	RQ Hold Time into MBL 8086	40		30		20		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8 V to 2.0 V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0 V to 0.8 V

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

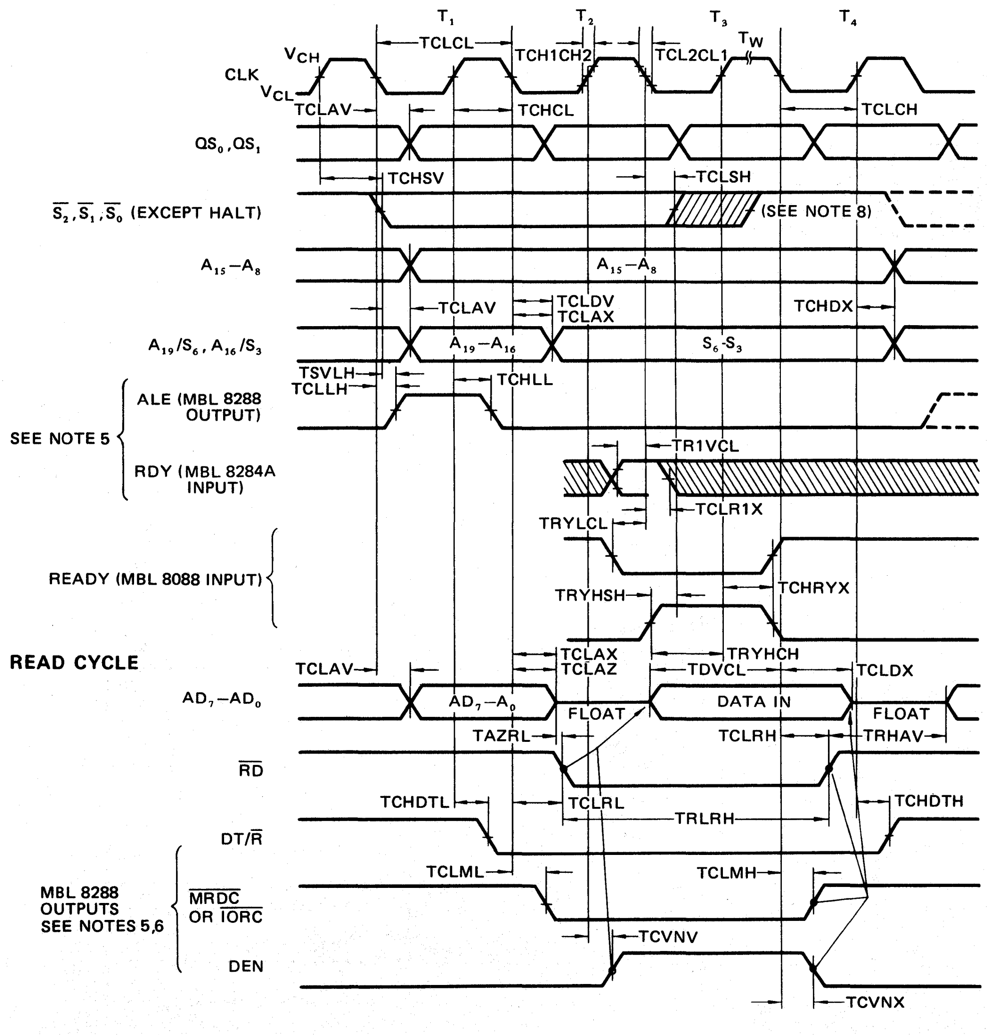
Symbol	Parameter	MBL 8088		MBL 8088-2		MBL 8088-1 (Preliminary)		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TCLML	Command Active Delay (See Note 1)	10	35	10	35	10	35	ns	
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	10	35	ns	C_L=20–100pF for all MBL 8088 Outputs in addition to internal loads
TRYHSH	READY Active to Status Passive (See Note 3)		110		65		45	ns	
TCHSV	Status Active Delay	10	110	10	60	10	45	ns	
TCLSH	Status Inactive Delay	10	130	10	70	10	55	ns	
TCLAV	Address Valid Delay	10	110	10	60	10	50	ns	
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	10	40	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15		15	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	10	50	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		0		ns	
TCLRL	RD Active Delay	10	165	10	100	10	70	ns	
TCLRH	RD Inactive Delay	10	150	10	80	10	60	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL–45		TCLCL–40		TCLCL–35		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30		30	ns	
TCLGL	GT Active Delay		85		50	0	45	ns	
TCLGH	GT Inactive Delay		85		50	0	45	ns	
TRLRH	RD Width	2TCLCL–75		2TCLCL–50		2TCLCL–40		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8 V to 2.0 V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0 V to 0.8 V

NOTES:

1. Signal at MBL 8284A or MBL 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T_2 state (8 ns into T_3 state).

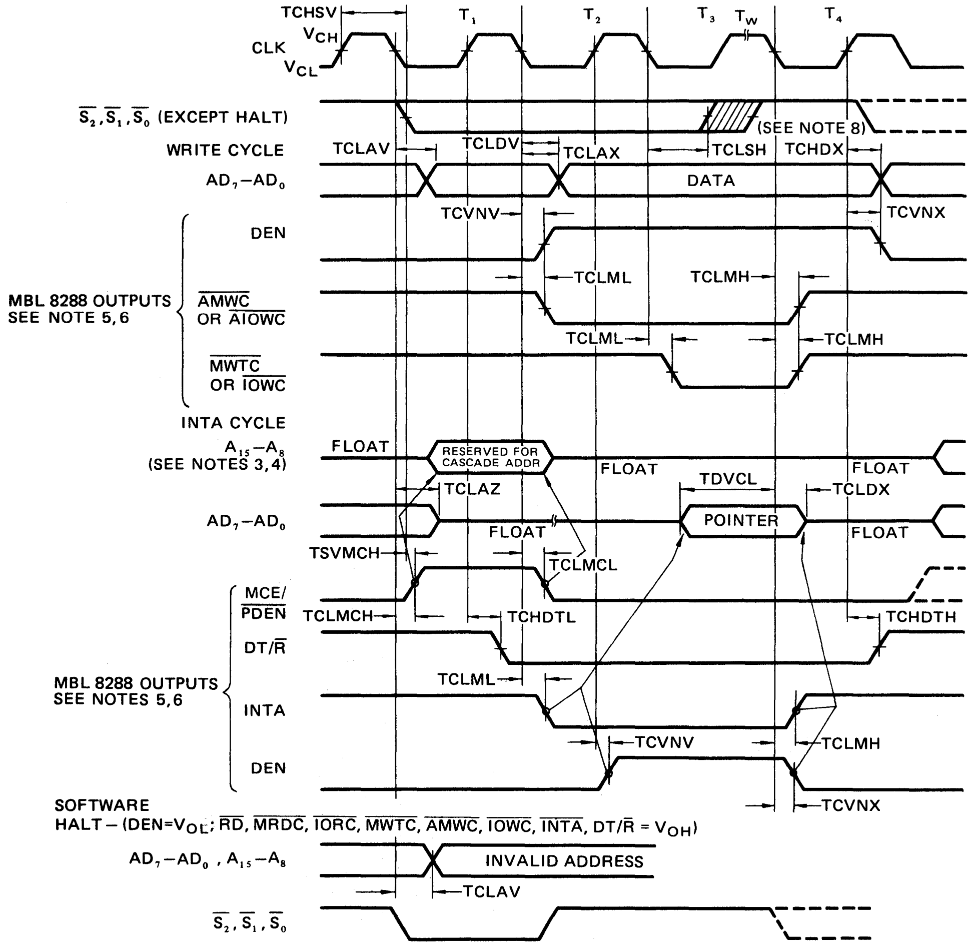
WAVEFORMS (Continued)

BUS TIMING—MAXIMUM MODE SYSTEM (USING MBL 8288)



WAVEFORMS (Continued)

BUS TIMING–MAXIMUM MODE SYSTEM (USING MBL 8288)

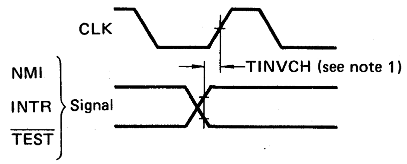


NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. CASCADE ADDRESS IS VALID BETWEEN FIRST AND SECOND $\overline{\text{INTA}}$ CYCLES.
4. TWO $\overline{\text{INTA}}$ CYCLES RUN BACK-TO-BACK. THE MBL 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH $\overline{\text{INTA}}$ CYCLES. CONTROL FOR POINTER ADDRESS IS SHOWN FOR SECOND $\overline{\text{INTA}}$ CYCLE.
5. SIGNALS AT MBL 8284A OR MBL 8288 ARE SHOWN FOR REFERENCE ONLY.
6. THE ISSUANCE OF THE MBL 8288 COMMAND AND CONTROL SIGNALS ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ AND DEN) LAGS THE ACTIVE HIGH MBL 8288 CEN.
7. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
8. STATUS INACTIVE IN STATE JUST PRIOR TO T_4.

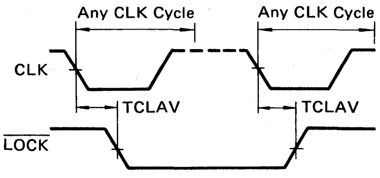
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION

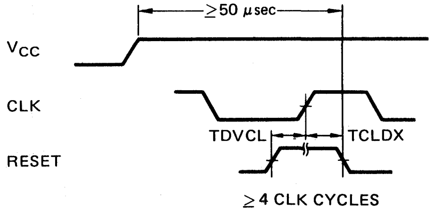


NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

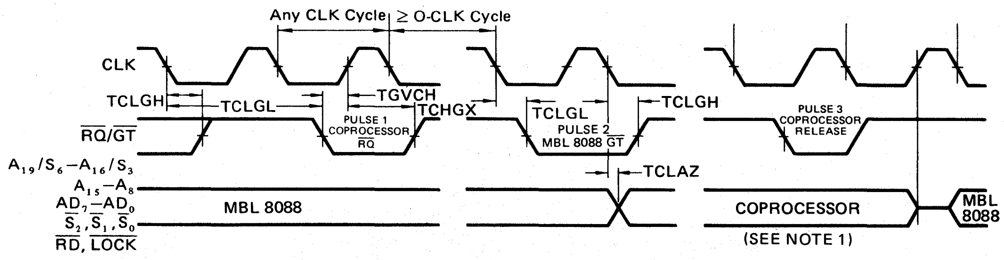
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING



REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE: 1. THE COPROCESSOR MAY NOT DRIVE THE BUSSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

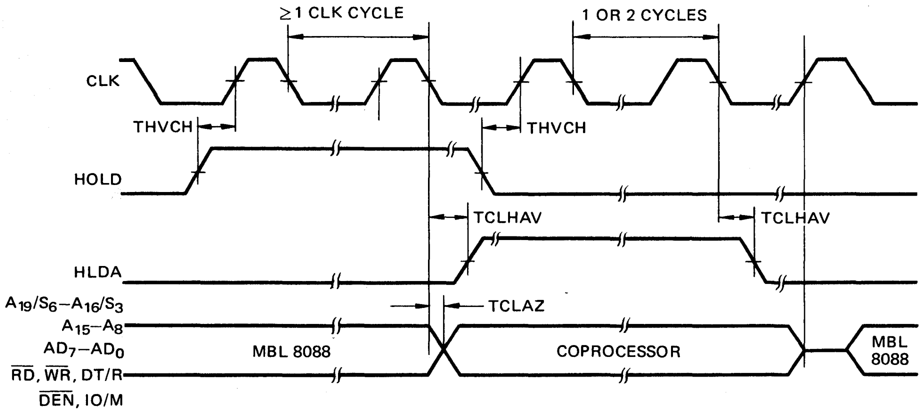


TABLE 2 – INSTRUCTION SET SUMMARY*

DATA TRANSFER				
MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate to register	1 0 1 1 w reg	data	data if w=1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			
ARITHMETIC				
ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w=1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w=1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w=1	
SBB = Subtract with borrow				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w=1	

DEC = Decrement:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG=Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w=01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w=1	
AAS =ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS =Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL =Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL=Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM=ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV =Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD =ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert byte to word	1 0 0 1 1 0 0 0			
CWD =Convert word to double word	1 0 0 1 1 0 0 1			
LOGIC				
NOT =Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR =Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL =Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate through carry flag right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1	
TEST = And function to flags. no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w=1	
STRING MANIPULATION				
REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w			
STOS = Store byte/wd from AL/A	1 0 1 0 1 0 1 w			

*Mnemonics © Intel Corporation, 1978

TABLE 2 – INSTRUCTION SET SUMMARY (Continued)*

CONTROL TRANSFER

CALL = Call:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	
JMP = Unconditional Jump:			
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1		
Within seg, adding immed, to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JMAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO = Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS = Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp
INT = Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET = Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CLC = Clear carry	1 1 1 1 1 0 0 0	
CMC = Complement carry	1 1 1 1 0 1 0 1	
STC = Set carry	1 1 1 1 1 0 0 1	
CLD = Clear direction	1 1 1 1 1 1 0 0	
STD = Set direction	1 1 1 1 1 1 0 1	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	
STI = Set interrupt	1 1 1 1 1 0 1 1	
HLT = Halt	1 1 1 1 0 1 0 0	
WAIT = Wait	1 0 0 1 1 0 1 1	
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	
NOP = No operation	1 0 0 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG
SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

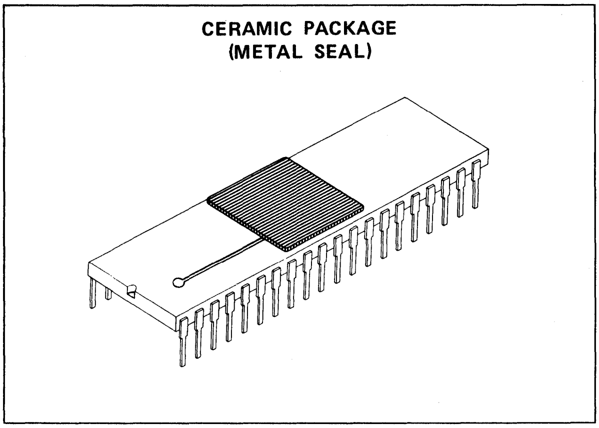
REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

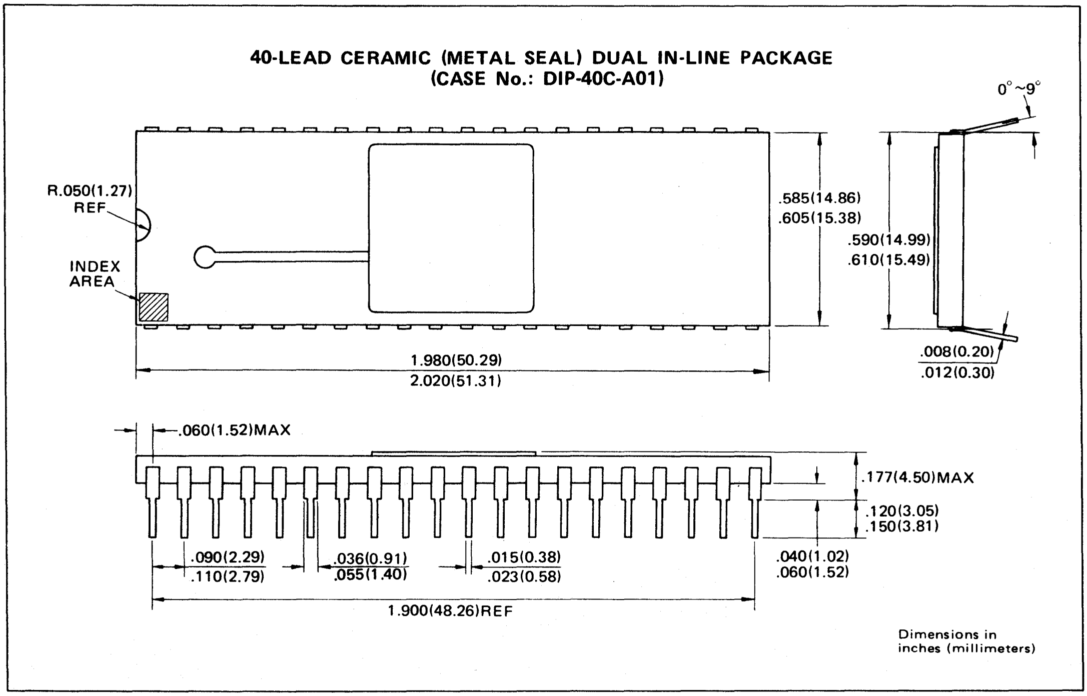
Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

PACKAGE ILLUSTRATION

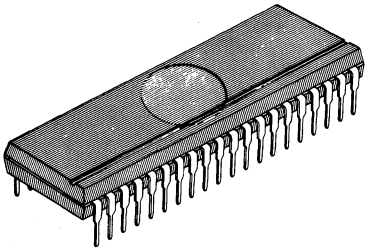


PACKAGE DIMENSIONS (Suffix: -C)



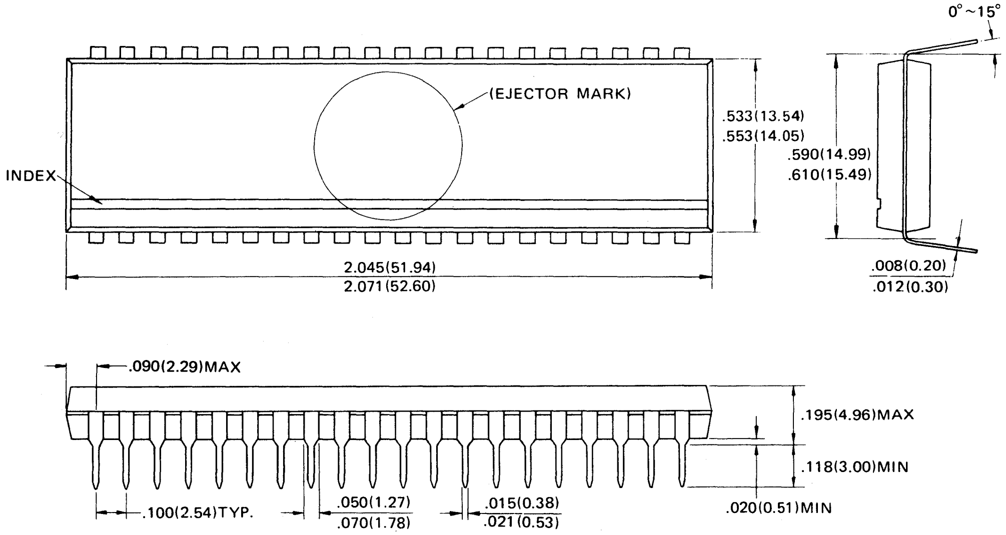
PACKAGE ILLUSTRATION

PLASTIC PACKAGE



PACKAGE DIMENSIONS (Suffix: -P)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in
inches (millimeters)

FUJITSU

NMOS 8&16-BIT I/O PROCESSOR

MBL 8089 MBL 8089-2

April 1985
Edition 3.0

NMOS 8 & 16-BIT I/O PROCESSOR

The Fujitsu MBL 8089 is a revolutionary concept in microprocessor input/output processing. Packaged in a 40-pin DIP package. MBL 8089 is a high performance processor implemented in N-channel, depletion load silicon gate technology (NMOS). The MBL 8089's instruction set and capabilities are optimized for high speed, flexible and efficient I/O handling. It allows easy interface of Fujitsu's 16-bit MBL 8086 and 8-bit MBL 8088 microprocessors with 8- and 16-bit peripherals. In the REMOTE configuration, MBL 8089 bus is user definable allowing it to be compatible with any 8/16-bit Fujitsu microprocessor, interfacing easily to the Fujitsu multiprocessor system bus standard MULTIBUS*.

The MBL 8089 performs the function of an intelligent DMA controller for the MBL 8086, 88 family and with its processing power, can remove I/O overhead from the MBL 8086 or MBL 8088. It may operate completely in parallel with a CPU, giving dramatically improved performance in I/O intensive applications. MBL 8089 provides two I/O channels, each supporting a transfer rate up to 1.25 Mbyte/sec (2.00 Mbyte/sec) at the standard clock frequency of 5 MHz(8 MHz). Memory based communication between the IOP and CPU enhances system flexibility and encourages software modularity, yielding more reliable, easier to develop systems.

- **High Speed DMA Capabilities Including I/O to Memory, Memory to I/O, Memory to Memory, and I/O to I/O**
- **MBL 8086, MBL 8088 Compatible: Removes I/O Overhead from CPU in iAPX 86/11 or 88/11 Configuration**
- **Allows Mixed Interface of 8- & 16-Bit Peripherals, to 8- & 16-Bit Processor Busses**
- **1 Mbyte Addressability**
- **Memory Based Communication with CPU**
- **Supports LOCAL or REMOTE I/O Processing**
- **Flexible, Intelligent DMA Functions Including Translation, Search, Word Assembly/Disassembly**
- **MULTIBUS* Compatible System Interface**
- **Two Clock Rates:**
  5 MHz for MBL 8089
  8 MHz for MBL 8089-2
- **40-pin Ceramic DIP (Suffix -C)**

Fig. 1 – BLOCK DIAGRAM

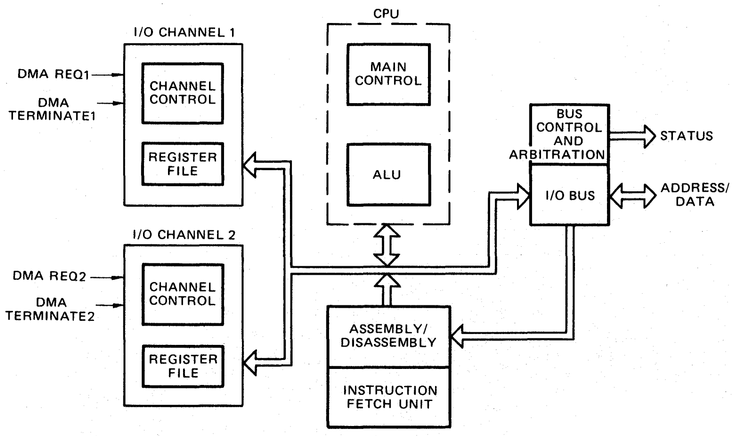


Fig. 2 – PIN CONFIGURATION

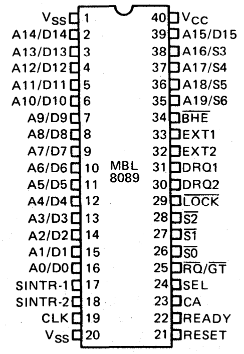


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Table 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
A0–A15/ D0–D15	I/O	**Multiplexed Address and Data Bus:** The functions of these lines are defined by the state of $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ lines. The pins are floated after reset and when the bus is not acquired. A8–A15 are stable on transfers to a physical 8-bit data bus (same bus as MBL 8088), and are multiplexed with data on transfers to a 16-bit physical bus.
A16–A19/ S3–S6	O	**Address and Status:** Multiplexed most significant address lines and status information. The address lines are active only when addressing memory. Otherwise, the status lines are active and are encoded as shown below. The pins are floated after reset and when the bus is not acquired. S6 S5 S4 S3 1 1 0 0 DMA cycle on CH1 1 1 0 1 DMA cycle on CH2 1 1 1 0 Non-DMA cycle on CH1 1 1 1 1 Non-DMA cycle on CH2
$\overline{BHE}$	O	**Bus High Enable:** The Bus High Enable is used to enable data operations on the most significant half of the data bus (D8–D15). The signal is active low when a byte is to be transferred on the upper half of the data bus. The pin is floated after reset and when the bus is not acquired. $\overline{BHE}$ does not have to be latched.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	O	**Status:** These are the status pins that define the IOP activity during any given cycle. They are encoded as shown below: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ 0 0 0 Instruction fetch; I/O space 0 0 1 Data fetch; I/O space 0 1 0 Data store; I/O space 0 1 1 Not used 1 0 0 Instruction fetch; System Memory 1 0 1 Data fetch; System Memory 1 1 0 Data store; System Memory 1 1 1 Passive The status lines are utilized by the bus controller and bus arbiter to generate all memory and I/O control signals. The signals change during T4 if a new cycle is to be entered while the return to passive state in T3 or T_W indicates the end of a cycle. The pins are floated after system reset and when the bus is not acquired.
READY	I	**Ready:** The ready signal received from the addressed device indicates that the device is ready for data transfer. The signal is active high and is synchronized by the MBL 8284A clock generator.

Symbol	Type	Name and Function
$\overline{LOCK}$	O	**Lock:** The lock output signal indicates to the bus arbiter that the bus is needed for more than one continuous cycle. It is set via the channel control register, and during the TSL instruction. The pin floats after reset and when the bus is not acquired. This output is active low.
RESET	I	**Reset:** The receipt of a reset signal causes the IOP to suspend all its activities and enter an idle state until a channel attention is received. The signal must be active for at least four clock cycles.
CLK	I	**Clock:** Clock provides all timing needed for internal IOP operation.
CA	I	**Channel Attention:** Gets the attention of the IOP. Upon the falling edge of this signal, the SEL input pin is examined to determine Master/Slave or CH1/CH2 information. This input is active high.
SEL	I	**Select:** The first CA received after system reset informs the IOP via the SEL line, whether it is a Master or Slave (0/1 for Master/Slave respectively) and starts the initialization sequence. During any other CA the SEL line signifies the selection of CH1/CH2. (0/1 respectively.)
DRQ1-2	I	**Data Request:** DMA request inputs which signal the IOP that a peripheral is ready to transfer/receive data using channels 1 or 2 respectively. The signals must be held active high until the appropriate fetch/stroke is initiated.
$\overline{RQ}/\overline{GT}$	I/O	**Request Grant:** Request Grant implements the communication dialogue required to arbitrate the use of the system bus (between IOP and CPU, LOCAL mode) or I/O bus when two IOPs share the same bus (REMOTE mode). The $\overline{RQ}/\overline{GT}$ signal is active low. An internal pull-up permits $\overline{RQ}/\overline{GT}$ to be left floating if not used.
SINTR1-2	O	**Signal Interrupt:** Signal interrupt outputs from channels 1 and 2 respectively. The interrupts may be sent directly to the CPU or through the MBL 8259A interrupt controller. They are used to indicate to the system the occurrence of user defined events.
EXT1-2	I	**External Terminate:** External terminate inputs for channels 1 and 2 respectively. The EXT signals will cause the termination of the current DMA transfer operation if the channel is so programmed by the channel control register. The signal must be held active high until termination is complete.
V_{CC}		**Voltage:** +5 volt power input.
V_{SS}		**Ground.**

FUNCTIONAL DESCRIPTION

The MBL 8089 IOP has been designed to remove I/O processing, control and high speed transfers from the central processing unit. Its major capabilities include that of initializing and maintaining peripheral components and supporting versatile DMA. This DMA function boasts flexible termination conditions (such as external terminate, mask compare, single transfer and byte count expired). The DMA function of the MBL 8089 IOP uses a two cycle approach where the information actually flows through the MBL 8089 IOP. This approach to DMA vastly simplifies the bus timings and enhances compatibility with memory and peripherals, in addition to allowing operations to be performed on the data as it is transferred. Operations can include such constructs as translate, where the MBL 8089 automatically vectors through a lookup table and mask compare, both on the "fly".

The MBL 8089 is functionally compatible with Fujitsu's MBL 8086, MBL 8088 family. It supports any combination of 8/16-bit busses. In the REMOTE mode it can be used to complement other Intel processor families. Hardware and communication architecture are designed to provide simple mechanisms for system upgrade.

The only direct communication between the IOP and CPU is handled by the Channel Attention and interrupt lines. Status information, parameters and task programs are passed via blocks of shared memory, simplifying hardware interface and encouraging structured programming.

The MBL 8089 can be used in applications such as file and buffer management in hard disk or floppy disk control. It can also provide for soft error recovery routines and scan control. CRT control, such as cursor control and auto scrolling, is simplified with the MBL 8089. Keyboard control, communication control and general I/O are just a few of the typical applications for the MBL 8089.

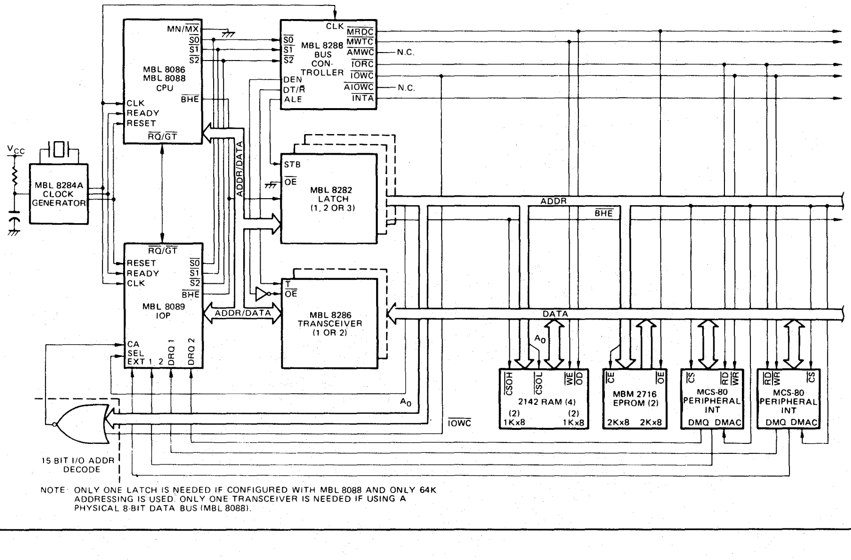
Remote and Local Modes

Shown in Figure 3 is the MBL 8089 in a LOCAL configuration. The MBL 8086 (or MBL 8088) is used in its maximum mode. The MBL 8089 and MBL 8086 reside on the same local bus, sharing the same set of system buffers. Peripheral located on the system bus can be addressed by either the MBL 8086 or the MBL 8089. The MBL 8089 requests the use of the LOCAL bus by means of the $\overline{RQ}/\overline{GT}$ line. This performs a similar function to that of HOLD and HLDA on the Intel 8085A, 8080A and MBL 8086 minimum mode but is implemented on one physical line. When the MBL 8086 relinquishes the system bus, the MBL 8089 used the same bus control, latches and transceiver components to generate the system address, control and data lines. This mode allows a more economical system configuration at the expense of reduced CPU thruput due to IOP bus utilization.

A typical REMOTE configuration is shown in Figure 4. In this mode, the IOP's bus is physically separated from the system bus by means of system buffers/latches. The IOP maintains its own local bus and can operate out of local or system memory. The system bus interface contains the following components:

- Up to three MBL 8282 buffer/latches to latch the address to the system bus.
- Up to two MBL 8286 devices bidirectionally buffer the system data bus.

Fig. 3 – TYPICAL iAPX 86/11, 88/11 CONFIGURATION WITH MBL 8089 IN LOCAL MODE, MBL 8088, MBL 8086 IN MAX MODE



NOTE: ONLY ONE LATCH IS NEEDED IF CONFIGURED WITH MBL 8088 AND ONLY 64K ADDRESSING IS USED. ONLY ONE TRANSCEIVER IS NEEDED IF USING A PHYSICAL 8-BIT DATA BUS (MBL 8088).

- An MBL 8288 bus controller supplies the control signals necessary for buffer operation as well as $\overline{\text{MRDC}}$ (Memory Read) and $\overline{\text{MWTC}}$ (Memory Write) signals.
- An MBL 8289 bus arbiter performs all the functions necessary to arbitrate the use of the system bus. This is used in place of the $\overline{\text{RQ}}/\overline{\text{GT}}$ logic in the LOCAL mode. This arbiter decodes type of cycle information from the MBL 8089 status lines to determine if the IOP desires to perform a transfer over the "common" or system bus.

The peripheral device PER1 and PER2 are supported on their own data and address bus, the MBL8089 communicates with the peripherals without affecting system bus operation. Optional buffers may be used on the local bus when capacitive loading conditions so dictate. I/O programs and RAM buffers may also reside on the local bus to further reduce system bus utilization.

COMMUNICATION MECHANISM

Fundamentally, communication between the CPU and IOP is performed through messages prepared in shared memory. The CPU can cause the MBL 8089 to execute a program by placing it in the MBL 8089's memory space and/or directing the MBL 8089's attention to it by asserting a hardware Channel Attention (CA) signal to the IOP, activating the proper I/O channel. The SEL Pin indicates to the IOP which channel is being addressed. Communication from the IOP to the processor can be performed in a simillar manner via a system interrupt (SINTR-1,2), if the CPU has enabled interrupts for this purpose. Additionally, the MBL 8089 can store messages in memory regarding its status and the status of any peripherals. This communication mechanism is supported by a hierarchical data structure to provide a maximum amount of flexibility of memory use with the added capability of handling multiple IOP's.

Illustrated in Figure 5 is an overview of the communication data structure hierarchy that exists for the MBL 8089 I/O processor. Upon the first CA from RESET, if the IOP is initialized as the BUS MASTER, 5 bytes of information are read into the MBL 8089 starting at location FFFF6 (FFFF6, FFFF8-FFFFB) where the type of system bus (16-bit or 8-bit) and pointers to the system configuration block are obtained. This is the only fixed location the MBL 8089 accesses. The remaining addresses are obtained via the data structure hierarchy. The MBL 8089 determines addresses in the same manner as does the MBL 8086; i.e., a 16-bit relocation pointer is offset left 4 bits and added to the 16-bit address offset, obtaining a 20-bit address. Once these 20-bit addresses are formed, they are stored as such as all the MBL 8089 address registers are 20 bits long. After the system configuration pointer address is formed, the MBL 8089 IOP accesses the system configuration block.

Fig. 4 – TYPICAL REMOTE CONFIGURATION

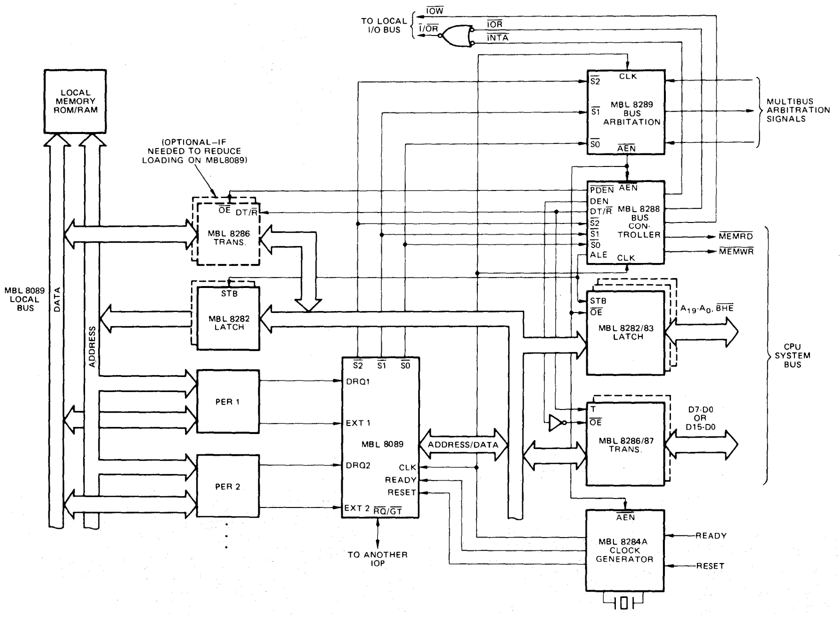
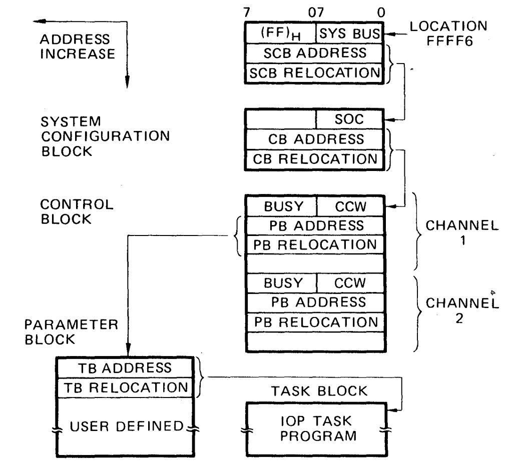


Fig. 5 – COMMUNICATION DATA STRUCTURE HIERARCHY



The System Configuration Block (SCB), used only during startup, points to the Control Block (CB) and provides IOP system configuration data via the SOC byte. The SOC byte initializes IOP I/O bus width to 8/16, and defines one of two IOP $\overline{RQ}/\overline{GT}$ operating modes. For $\overline{RQ}/\overline{GT}$ mode 0, the IOP is typically initialized as SLAVE and has its $\overline{RQ}/\overline{GT}$ line tied to a MASTER CPU (typical LOCAL configuration). In this mode, the CPU normally has control of the bus, grants control to the IOP as needed, and has the bus restored to it upon IOP task completion (IOP request—CPU grant—IOP done). For $\overline{RQ}/\overline{GT}$ mode 1, useful only in remote mode between two IOPs, MASTER/SLAVE designation is used only to initialize bus control: from then on, each IOP requests and grants as the bus is needed (IOP1 request—IOP2 grant—IOP2 request—IOP1 grant). Thus, each IOP retains bus control until the other requests it. The completion of initialization is signalled by the IOP clearing the BUSY flag in the CB. This type of startup allows the user to have the startup pointers in ROM with the SCB in RAM. Allowing the SCB to be in RAM gives the user the flexibility of being able to initialize multiple IOPs.

The Control Block furnishes bus control initialization for the IOP operation (CCW or Channel Control Word) and provides pointers to the Parameter Block or "data" memory for both channels 1 and 2. The CCW is retrieved and analyzed upon all CA's other than the first after a reset. The CCW byte is decoded to determine channel operation.

The Parameter Block contains the address of the Task Block and acts as a message center between the IOP and CPU. Parameters or variable information is passed from the CPU to its IOP in this block to customize the software interface to the peripheral device. It is also used for transferring data and status information between the IOP and CPU.

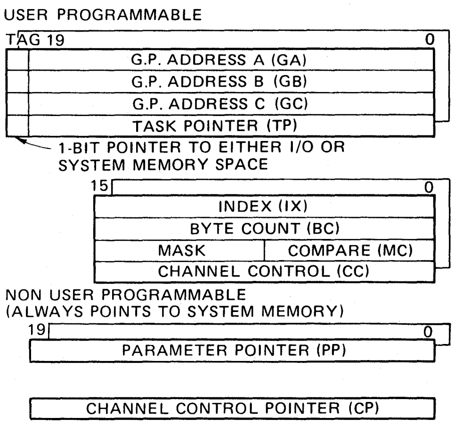
The Task Block contains the instructions for the respective channel. This block can reside on the local bus of the IOP, allowing the IOP to operate concurrently with the CPU, or reside in system memory.

The advantage of this type of communication between the processor, IOP and peripheral, is that it allows for a very clean method for the operating system to handle I/O routines. Canned programs or "Task Blocks" allow for execution of general purpose I/O routines with the status and peripheral command information being passed via the Parameter Block ("data" memory). Task Blocks (or "program" memory) can be terminated or restarted by the CPU, if need be. Clearly, the flexibility of this communication lends itself to modularity and applicability to a large number of peripheral devices and upward compatibility to future end user systems and microprocessor familes.

Register Set

The MBL 8089 maintains separate registers for its two I/O channels as well as some common registers (see Figure 6). There are sufficient registers for each channel to sustain its own DMA transfers, and process its own instruction stream. The basic DMA pointer registers (GA, GB – 20 bits each), can point either the system bus or local bus, DMA source or destination, and can be autoincremented. A third register set (GC) can be used to allow translation during the DMA process through a lookup table it points to. Additionally, registers are provided for a masked compare during the data transfer and can be set up to act as one of the termination conditions. Other registers are also provided. Many of these registers can be used as general purpose registers during program execution, when the IOP is not performing DMA cycles.

Fig. 6 – REGISTER MODEL



Bus Operation

The MBL 8089 utilizes the same bus structure as the MBL 8086, MBL 8088 in their maximum mode configurations (see Figure 7).The address is time multiplexed with the data on the first 16/8 lines. A16 through A19 are time multiplexed with four status lines S3-S6. For MBL 8089 cycles, S4 and S3 determined what type of cycle (DMA versus non-DMA) is being performed on channels 1 or 2. S5 and S6 are a unique code assigned to the MBL 8089 IOP, enabling the user to detect which processor is performing a bus cycle in a multiprocessing environment. The first three status lines, $\overline{S0}$-$\overline{S2}$, are used with an MBL 8288 bus controller to determine if an instruction fetch or data transfer is being performed in I/O or system memory space.

DMA transfers require at least two bus cycles with each bus cycle requiring a minimum of four clock cycles. Additional clock cycles are added if wait states are required. This two cycle approach simplifies considerably the bus timings in burst DMA. The MBL 8089 optimizes the transfer between two different bus widths by using three bus cycles versus four to transfer 1 word. More than one read (write) is performed when mapping an 8-bit bus onto a 16-bit bus (vice versa). For example, a data transfer from an 8-bit peripheral to a 16-bit physical location in memory is performed by first doing two reads, with word assembly within the IOP assembly register file and then one write.

As can be expected, the data bandwidth of the IOP is a function of the physical bus width of the system and I/O busses. Table 2 gives the bandwidth, latency and bus utilization of the MBL 8089. The system bus is assumed to be 16-bits wide with either an 8-bit peripheral (under byte column) or 16-bit peripheral (word column) being shown.

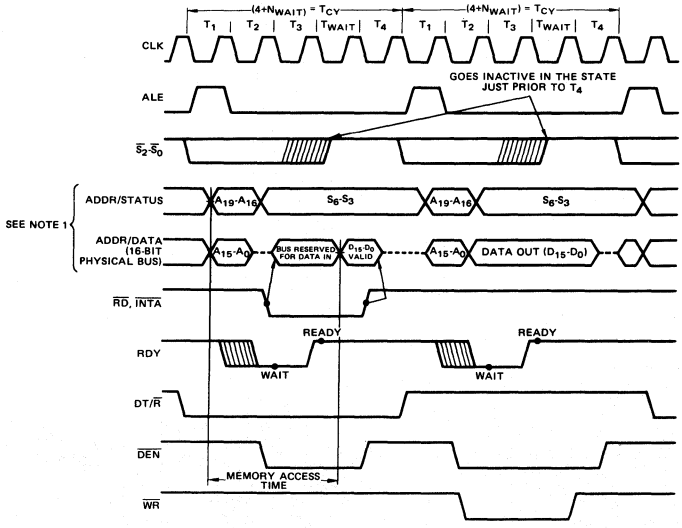
The latency refers to the worst case response time by the IOP to a DMA request, without the bus arbitration times. Notice that the word transfer allows 50% more bandwidth. This occurs since three bus cycles are required to map 8-bit data into a 16-bit location, versus two for a 16-bit to 16-bit transfer. Note that it is possible to fully saturate the system bus in the LOCAL mode whereas in the REMOTE mode this is reduced to a maximum of 50%.

Table 2 – ACHIEVABLE MBL 8089 OPERATIONS WITH 16-BIT SYSTEM BUS

	MBL 8089 (5MHz)				MBL 8089-2 (8MHz)			
	Local		Remote		Local		Remote	
	Byte	Word	Byte	Word	Byte	Word	Byte	Word
Bandwidth	830 KB/S	1250 KB/S	830 KB/S	1250 KB/S	1328 KB/S	2000 KB/S	1328 KB/S	2000 KB/S
Latency	1.0/2.4μsec*	1.0/2.4μsec*	1.0/2.4μsec*	1.0/2.4μsec*	0.625/1.5μsec**	0.625/1.5μsec**	0.625/1.5μsec**	0.625/1.5μsec**
System Bus Utilization	2.4μsec/ Transfer	1.6μsec/ Transfer	0.8μsec/ Transfer	0.8μsec/ Transfer	1.5μsec/ Transfer	1.0μsec/ Transfer	0.5μsec/ Transfer	0.5μsec/ Transfer

* 2.4μsec if interleaving with other channel and no wait states. 1μse if channel is waiting for request.
** 1.5μsec if interleaving with other channel and no wait states. 0.625μsec if channel is waiting for request.

Fig. 7 — MBL 8089 BUS OPERATION



NOTE 1: $\overline{BHE}$ IS STABLE (i.e., NON MULTIPLEXED) THROUGHOUT EACH TRANSFER CYCLE. A_8-A_{15} ARE ALSO STABLE ON TRANSFERS TO A PHYSICAL 8-BIT BUS.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . –65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . -0.5 to +7V
Power Dissipation . . . . 2.5 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400 µA
I_{CC}	Power Supply Current		350	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	µA	$0V < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±10	µA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
V_{CL}	Clock Input Low Voltage	-0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Input Buffer (All Input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz

A.C. CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to 70°C)

MBL 8089/8086 AND MBL 8089-2/8086-2 MAX MODE SYSTEM (USING MBL 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	MBL 8089		MBL 8089-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
TCHCL	CLK High Time	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into MBL 8284A (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into MBL 8284A (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into MBL 8089	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
TCHRYX	READY Hold Time into MBL 8089	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	-8		-8		ns	
TINVCH	Setup Time Recognition (DRQ 1,2, RESET, Ext 1,2) (See Note 2)	30		15		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30		15		ns	
TCAHCAL	CA Width	95		75		ns	
TSLVCAL	SEL Setup Time	75		55		ns	
TCALSLX	SEL Hold Time	0		0		ns	
TCHGX	$\overline{GT}$ Hold Time into MBL 8089	40		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

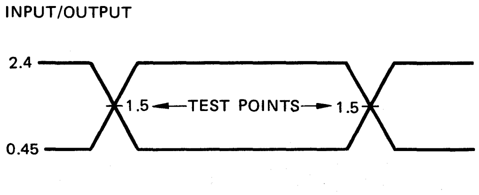
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	MBL 8089		MBL 8089-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLML	Command Active Delay (See Note 1)	10	35	10	35	ns	C_L = 80pF
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	ns	C_L = 150pF
TRYHSH	READY Active to Status Passive (See Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30	ns	
TCLGL	$\overline{RQ}$ Active Delay	0	85	0	50	ns	C_L = 100pF
TCLGH	$\overline{RQ}$ Inactive Delay		85		50	ns	Note 5; C_L = 30pF
TCLSRV	SINTR Valid Delay		150		100	ns	C_L = 100pF
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

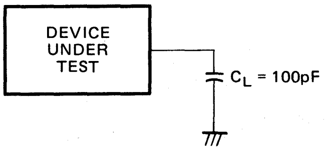
NOTES:
1. Signal at MBL 8284A or MBL 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and TW states.
4. Applies only to T2 state.
5. Applies only if $\overline{RQ}/\overline{GT}$ Mode 1 C_L = 30 pF, 2.7 kΩ pull up to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". THE CLOCK IS DRIVEN AT 4.3V AND 0.25V. TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0".

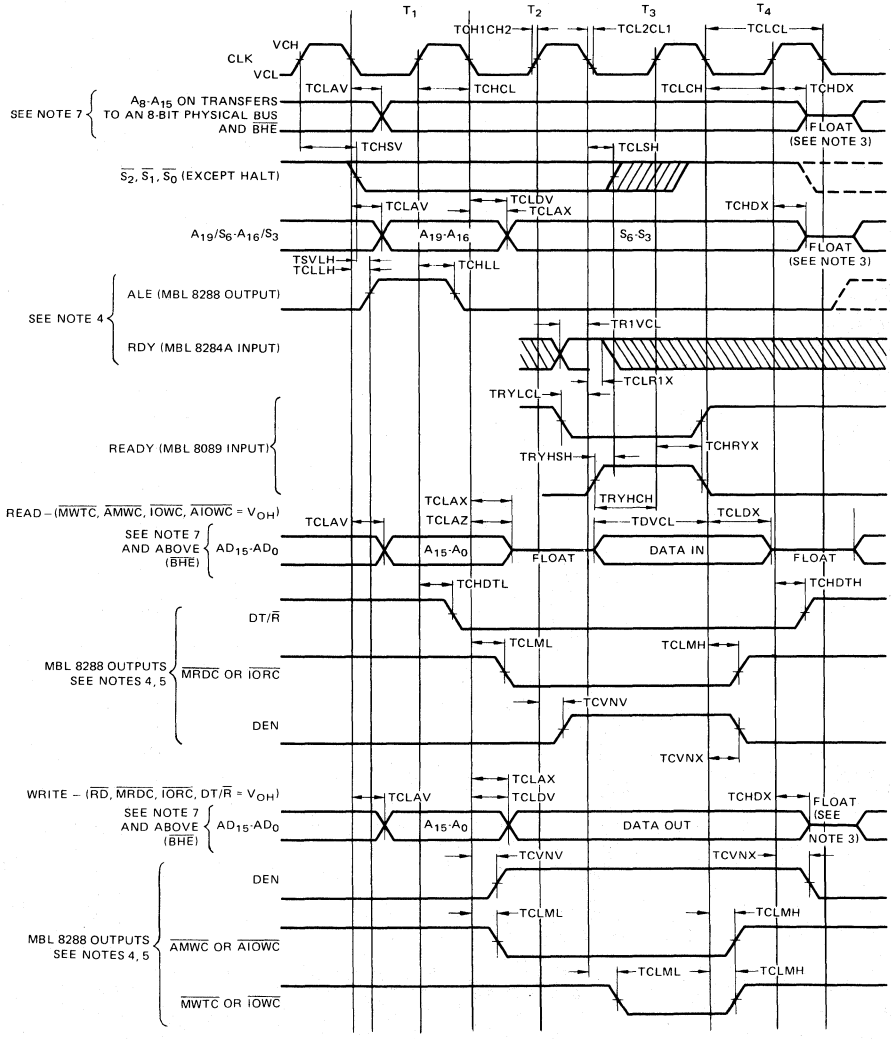
A.C. TESTING LOAD CIRCUIT



C_L = 100pF
C_L INCLUDES JIG CAPACITANCE

WAVEFORMS

MBL 8089 BUS TIMING USING MBL 8288

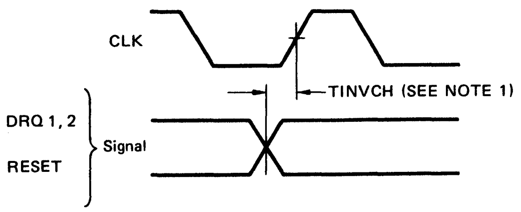


NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINE STATES ARE TO BE INSERTED.
3. FOLLOWING A WRITE CYCLE DATA REMAINS VALID ON THE MBL 8089 LOCAL BUS UNTIL A LOCAL BUS MASTER DECIDES TO RUN ANOTHER BUS CYCLE. THE LOCAL BUS IS FLOATED BY THE MBL 8089 WHEN THE MBL 8089 ENTERS A REQUEST BUS ACKNOWLEDGE STATE.
4. SIGNALS AT MBL 8284A OR MBL 8288 ARE SHOWN FOR REFERENCE ONLY.
5. THE ISSUANCE OF THE MBL 8288 COMMAND AND CONTROL SIGNALS ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ AND DEN) LAGS THE ACTIVE HIGH MBL 8288 CEN.
6. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
7. A_8-A_{15} ARE STABLE ON TRANSFERS TO AN 8 BIT PHYSICAL DATA BUS, i.e. A_8-A_{15} DON'T FLOAT ON A READ FROM AN 8 BIT PHYSICAL BUS OR MULTIPLEX WITH DATA ON A WRITE TO AN 8 BIT PHYSICAL BUS $\overline{BHE}$ IS STABLE (NON MULTIPLEXD) FOR ALL TRANSFERS.

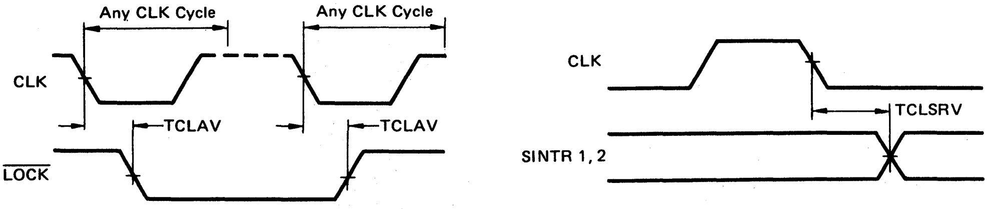
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION



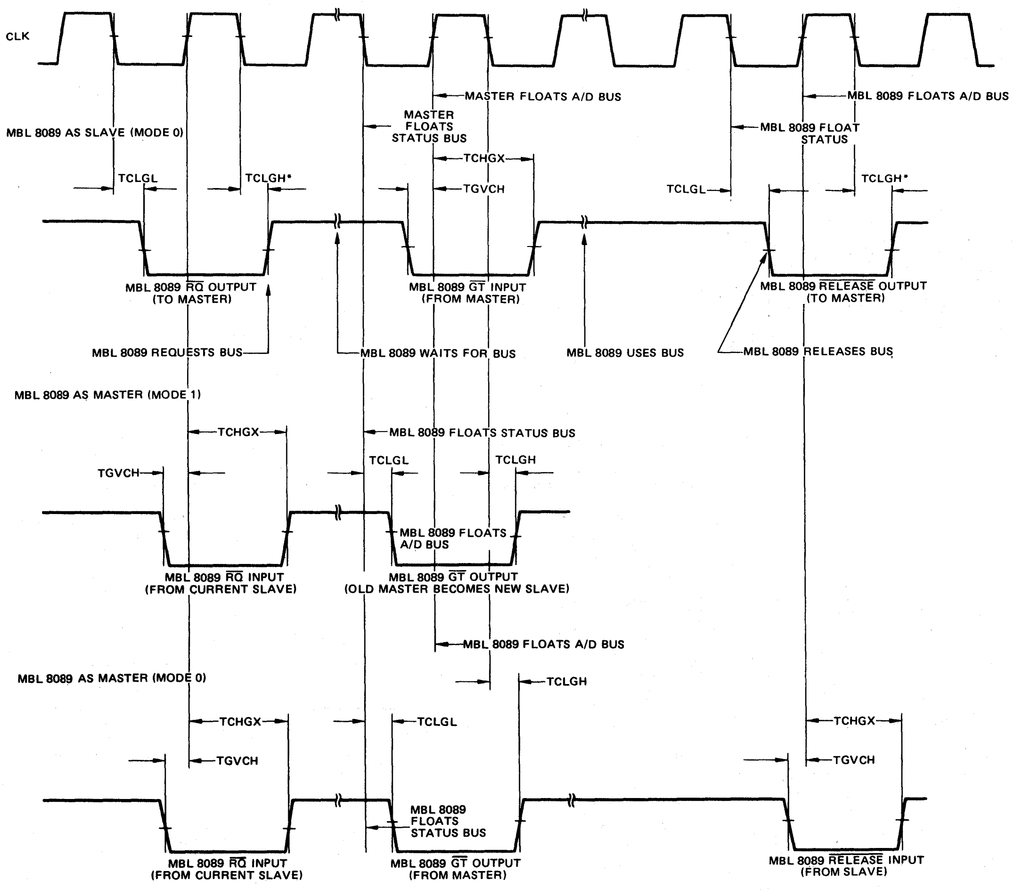
NOTES:
1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK.
2. ALL INPUTS EXCEPT CA ARE LATCHED ON A CLK EDGE. THE CA INPUT IS NEGATIVE EDGE TRIGGERED.
3. DRQ BECOMING ACTIVE GREATER THAN 30 ns AFTER THE RISING EDGE OF CLK WILL GUARANTEE NON-RECOGNITION UNTIL THE NEXT RISING CLOCK EDGE.

BUS LOCK SIGNAL TIMING AND SINTR TIMING



WAVEFORMS (Continued)

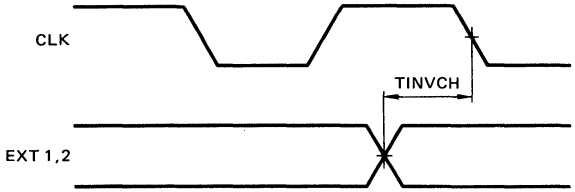
REQUEST/GRANT SEQUENCE TIMING


CLK
MBL 8089 AS SLAVE (MODE 0)
MASTER FLOATS A/D BUS
MASTER FLOATS STATUS BUS
MBL 8089 FLOATS A/D BUS
MBL 8089 FLOAT STATUS
TCLGL
TCLGH*
TCHGX
TGVCH
TCLGL
TCLGH*
MBL 8089 $\overline{RQ}$ OUTPUT (TO MASTER)
MBL 8089 $\overline{GT}$ INPUT (FROM MASTER)
MBL 8089 $\overline{RELEASE}$ OUTPUT (TO MASTER)
MBL 8089 REQUESTS BUS
MBL 8089 WAITS FOR BUS
MBL 8089 USES BUS
MBL 8089 RELEASES BUS
MBL 8089 AS MASTER (MODE 1)
TCHGX
MBL 8089 FLOATS STATUS BUS
TGVCH
TCLGL
TCLGH
MBL 8089 FLOATS A/D BUS
MBL 8089 $\overline{RQ}$ INPUT (FROM CURRENT SLAVE)
MBL 8089 $\overline{GT}$ OUTPUT (OLD MASTER BECOMES NEW SLAVE)
MBL 8089 FLOATS A/D BUS
MBL 8089 AS MASTER (MODE 0)
TCLGH
TCHGX
TCLGL
TGVCH
TCHGX
TGVCH
MBL 8089 FLOATS STATUS BUS
MBL 8089 $\overline{RQ}$ INPUT (FROM CURRENT SLAVE)
MBL 8089 $\overline{GT}$ OUTPUT (FROM MASTER)
MBL 8089 $\overline{RELEASE}$ INPUT (FROM SLAVE)

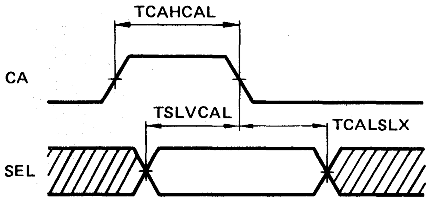
* CPU provides active pull-up.

WAVEFORMS (Continued)

EXTERNAL TERMINATE SETUP TIMING



SEL SETUP AND TIMING



MBL 8089 INSTRUCTION SET SUMMARY†

Data Transfers

POINTER INSTRUCTIONS			OPCODE	
			7 0	7 0
LPD	P, M	Load Pointer PPP from Addressed Location	P P P 0 0 A A 1	1 0 0 0 1 0 M M
LPDI	P, I	Load Pointer PPP Immediate 4 Bytes	P P P 1 0 0 0 1	0 0 0 0 1 0 0 0
MOVP	M, P	Store Contents of Pointer PPP in Addressed Location	P P P 0 0 A A 1	1 0 0 1 1 0 M M
MOVP	P, M	Restore Pointer	P P P 0 0 A A 1	1 0 0 0 1 1 M M
MOVE DATA			OPCODE	
MOV	M, M	Move from Source to Destination Source —	0 0 0 0 0 A A W	1 0 0 1 0 0 M M
		Destination —	0 0 0 0 0 A A W	1 1 0 0 1 1 M M
MOV	R, M	Load Register RRR from Addressed Location	R R R 0 0 A A W	1 0 0 0 0 0 M M
MOV	M, R	Store Contents of Register RRR in Addressed Location	R R R 0 0 A A W	1 0 0 0 0 1 M M
MOVI	R	Load Register RRR Immediate (Byte) Sign Extend	R R R wb 0 0 W	0 0 1 1 0 0 0 0
MOVI	M	Move Immediate to Addressed Location	0 0 0 wb A A W	0 1 0 0 1 1 M M

Control Transfer

CALLS			OPCODE	
			7 0	7 0
*CALL		Call Unconditional	1 0 0 dd A A W	1 0 0 1 1 1 M M
JUMP			OPCODE	
JMP		Unconditional	1 0 0 dd 0 0 W	0 0 1 0 0 0 0 0
JZ	M	Jump on Zero Memory	0 0 0 dd A A W	1 1 1 0 0 1 M M
JZ	R	Jump on Zero Register	R R R dd 0 0 0	0 1 0 0 0 1 0 0
JNZ	M	Jump on Non-Zero Memory	0 0 0 dd A A W	1 1 1 0 0 0 M M
JNZ	R	Jump on Non-Zero Register	R R R dd 0 0 0	0 1 0 0 0 0 0 0
JBT		Test Bit and Jump if True	B B B dd A A 0	1 0 1 1 1 1 M M
JNBT		Test Bit and Jump if Not True	B B B dd A A 0	1 0 1 1 1 0 M M
JMCE		Mask/Compare and Jump on Equal	0 0 0 dd A A 0	1 0 1 1 0 0 M M
JMCNE		Mask/Compare and Jump on Non-Equal	0 0 0 dd A A 0	1 0 1 1 0 1 M M

Arithmetic and Logic Instructions

INCREMENT, DECREMENT			OPCODE	
			7 0	7 0
INC	M	Increment Addressed Location	0 0 0 0 0 A A W	1 1 1 0 1 0 M M
INC	R	Increment Register	R R R 0 0 0 0 0	0 0 1 1 1 0 0 0
DEC	M	Decrement Addressed Location	0 0 0 0 0 A A W	1 1 1 0 1 1 M M
DEC	R	Decrement Register	R R R 0 0 0 0 0	0 0 1 1 1 1 0 0

† Mnemonics © Intel, 1980

Arithmetic and Logic Instructions

		ADD	OPCODE	
			7 0	7 0
ADDI	M, I	ADD Immediate to Memory	0 0 0 wb A A W	1 1 0 0 0 0 M M
ADDI	R, I	ADD Immediate to Register	R R R wb 0 0 W	0 0 1 0 0 0 0 0
ADD	M, R	ADD Register to Memory	R R R 0 0 A A W	1 1 0 1 0 0 M M
ADD	R, M	ADD Memory to Register	R R R 0 0 A A W	1 0 1 0 0 0 M M
		AND	**OPCODE**	
ANDI	M, I	AND Memory with Immediate	0 0 0 wb A A W	1 1 0 0 1 0 M M
ANDI	R, I	AND Register with Immediate	R R R wb 0 0 W	0 0 1 0 1 0 0 0
AND	M, R	AND Memory with Register	R R R 0 0 A A W	1 1 0 1 1 0 M M
AND	R, M	AND Register with Memory	R R R 0 0 A A W	1 0 1 0 1 0 M M
		OR	**OPCODE**	
ORI	M, I	OR Memory with Immediate	0 0 0 wb A A W	1 1 0 0 0 1 M M
ORI	R, I	OR Register with Immediate	R R R wb A A W	0 0 1 0 0 1 0 0
OR	M, R	OR Memory with Register	R R R 0 0 A A W	1 1 0 1 0 1 M M
OR	R, M	OR Register with Memory	R R R 0 0 A A W	1 0 1 0 0 1 M M
		NOT	**OPCODE**	
NOT	R	Complement Register	R R R 0 0 0 0 0	0 0 1 0 1 1 0 0
NOT	M	Complement Memory	0 0 0 0 0 A A W	1 1 0 1 1 1 M M
NOT	R, M	Complement Memory, Place in Register	R R R 0 0 A A W	1 0 1 0 1 1 M M

BIT Manipulation and Test Instructions

	BIT MANIPULATION	OPCODE	
		7 0	7 0
SET	Set the Selected Bit	B B B 0 0 A A 0	1 1 1 1 0 1 M M
CLR	Clear the Selected Bit	B B B 0 0 A A 0	1 1 1 1 1 0 M M
	TEST	**OPCODE**	
TSL	Test and Set Lock	0 0 0 1 1 A A 0	1 0 0 1 0 1 M M

Control

	CONTROL	OPCODE	
		7 0	7 0
HLT	Halt Channel Execution	0 0 1 0 0 0 0 0	0 1 0 0 1 0 0 0
SINTR	Set Interrupt Service Flip Flop	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0
NOP	No Operation	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
XFER	Enter DMA Transfer	0 1 1 0 0 0 0 0	0 0 0 0 0 0 0 0
WID	Set Source, Destination Bus Width; S, D 0=8, 1=16	1 S D 0 0 0 0 0	0 0 0 0 0 0 0 0

*AA Field in call instruction can be 00, 01, 10 only.
**OPCODE is second byte fetched.

All instructions consist of at least 2 bytes, while some instructions may use up to 3 additional bytes to specify literals and displacement data. The definition of the various fields within each instruction is given below:

7			0	7	0
R R R	w b	A A	W	OPCODE	M M
P P P B B B					

MM Base Pointer Select	
00	GA; general purpose A
01	GB; general purpose B
10	GC; general purpose C
11	PP; parameter pointer

RRR Register Field

The RRR field specifies a 16-bit register to be used in the instruction. If GA, GB, GC or TP are referenced by the RRR field, the upper 4 bits of the registers are loaded with the sign bit (Bit 15). PPP registers are used as 20-bit address pointers.

RRR				
000	r0	GA	;	general purpose A
001	r1	GB	;	general purpose B
010	r2	GC	;	general purpose C
011	r3	BC	;	byte count
100	r4	TP	;	task block pointer
101	r5	IX	;	index register
110	r6	CC	;	channel control (mode)
111	r7	MC	;	mask/compare

See Notes 1, 2.

PPP				
000	p^0	GA	;	general purpose A
001	p^1	GB	;	general purpose B
010	p^2	GC	;	general purpose C
100	p^4	TP	;	task block pointer

Note 1. Logical and arithmetic instructions should not be used to update the CC register (i.e. – only MOV and MOVI instructions should be used.)

2. A 20-bit register (GA, GB, GC or TP) that is initialized as a 16-bit I/O space pointer must be saved at even addresses when using MOVP or CALL instructions.

Notes:

BBB Bit Select Field

The bit select field replaces the RRR field in bit manipulation instructions and is used to select a bit to be operated on by those instructions. Bit 0 is the least significant bit.

wb

01 1 byte literal
10 2 byte (word) literal

dd

01 1 byte displacement
10 2 byte (word) displacement.

AA Field

00 The selected pointer contains the operand address.
01 The operand address is formed by adding an 8-bit, unsigned, offset contained in the instruction to the selected pointer. The contents of the pointer are unchanged.
10 The operand address is formed by adding the contents of the index register to the selected pointer. Both registers remain unchanged.
11 Same as 10 except the index register is post auto-incremented (by 1 for 8-bit transfer, by 2 for 16-bit transfer)

W Width Field

0 The selected operand is 1 byte long.
1 The selected operand is 2 bytes long.

Additional Bytes

OFFSET	:	8-bit unsigned offset.
SDISP	:	8/16-bit signed displacement.
LITERAL	:	8/16-bit literal. (32 bits for LDPI).

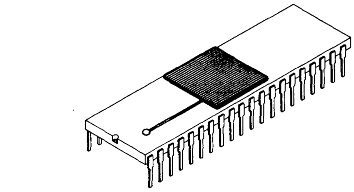
The order in which the above optional bytes appear in IOP instructions is given below:

OFFSET	LITERAL	SDISP

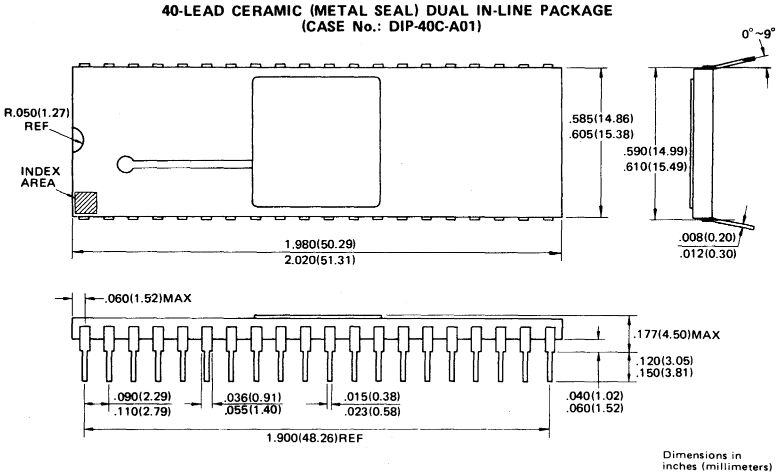
Offsets are treated as unsigned numbers. Literals and displacements are sign extended (2's complement).

PACKAGE ILLUSTRATION

CERAMIC PACKAGE
(METAL SEAL)



PACKAGE DIMENSIONS
(Suffix : -C)



FUJITSU

NMOS PROGRAMMABLE INTERRUPT CONTROLLER

MBL 8259A
MBL 8259A-2

July 1986
Edition 2.2

NMOS PROGRAMMABLE INTERRUPT CONTROLLER

The MBL8259A Programmable Interupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.
The MBL8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimizatic for a variety of system requirements.

- **MBL 8086, MBL 8088 Compatible**
- **MCS-80*, MCS-85* Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single + 5V Supply (No Clocks)**
- **Two Package Options:**
  –28-Pin Ceramic DIP (Suffix: -C)
  –28-Pin Plastic DIP (Suffix: -P)

Fig. 1 – BLOCK DIAGRAM

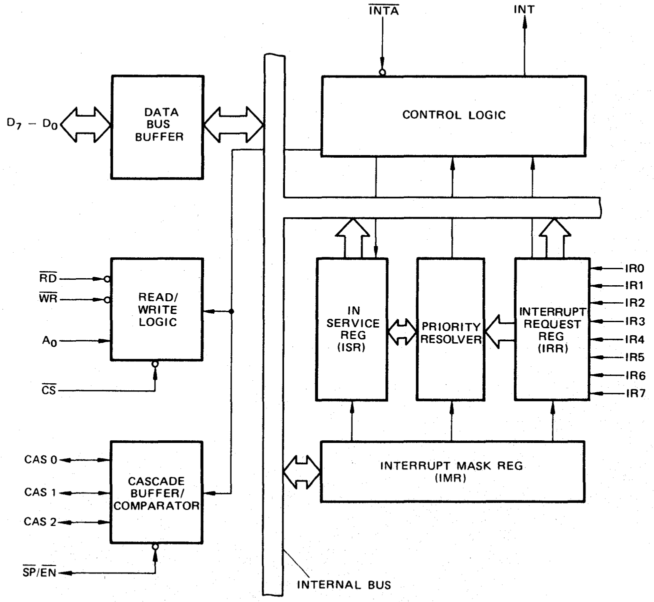
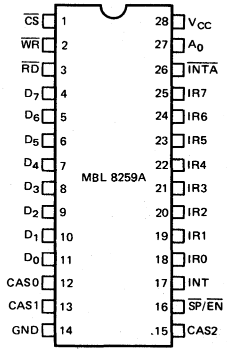


Fig. 2 – PIN CONFIGURATION



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PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

Symbc	Pin No.	Type	Name and Function
V_{CC}	28	I	**Supply:** +5V Supply.
GND	14	I	**Ground**
$\overline{CS}$	1	I	**Chip Select:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the MBL 8259A $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	O	**Write:** A low on this pin when $\overline{CS}$ is low enables the MBL 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**Read:** A low on this pin when $\overline{CS}$ is low enables the MBL 8259A to release status onto the data bus for the CPU.
D_7–D_0	4–11	I/O	**Bldirectional Data Bus:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12,13,15	I/O	**Cascade Lines:** The CAS lines form a private MBL 8259A bus to control a multiple MBL 8259A structure. These pins are outputs for a master MBL 8259A and inputs for a slave MBL 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**Slave Program/Enable Buffer:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master ($\overline{SP}$=1) or slave ($\overline{SP}$=0).
INT	17	O	**Interrupt:** This pin goes high wheaever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**Interrupt Request:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode). Unused IR pins should externally be pulled down not to be left open because the IR inputs contain internal pull-up resistors.
$\overline{INTA}$	26	I	**Interrupt Acknowledge:** This pin is used to enable MBL 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU. When the MBL 8259A is connected to the MBL 80186/80188 or Intel 80186/80188, an external pull-up resistor is required on the $\overline{INTA}$ pins.
A_0	27	I	**A0 Address Line:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the MBL 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address line (A_1 for MBL 8086/8088).

FUNCTIONAL DESCRIPTION

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughout.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continues polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is the highest importance (priority), ascertains whether the incoming request has higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The MBL 8259A

The MBL 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other MBL 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the MBL 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Fig. 3a—POLLED METHOD

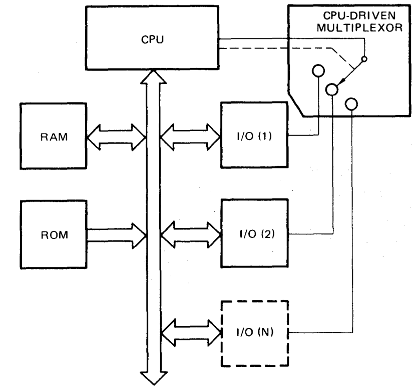
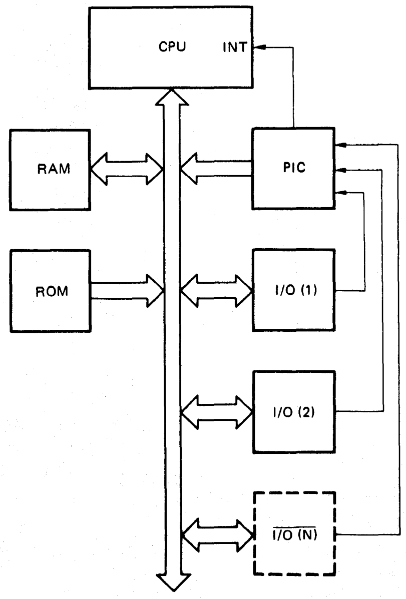


Fig. 3b—INTERRUPT METHOD



INTERRRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register(ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{\text{INTA}}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with Intel's 8080A and 8085A and MBL 8086 input levels.

$\overline{\text{INTA}}$ (INTERRUPT ACKNOWLEDGE)

$\overline{\text{INTA}}$ pulses will cause the MBL 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (µPM) of the MBL 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the MBL 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the MBL 8259A to be transferred onto the Data Bus.

$\overline{\text{CS}}$ (CHIP SELECT)

A LOW on this input enables the MBL 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{\text{WR}}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the MBL 8259A.

$\overline{\text{RD}}$ (READ)

A LOW on this input enables the MBL 8259A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the Data Bus.

Fig. 4a–MBL 8259A BLOCK DIAGRAM

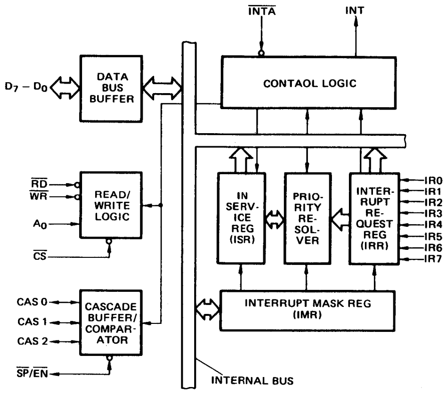
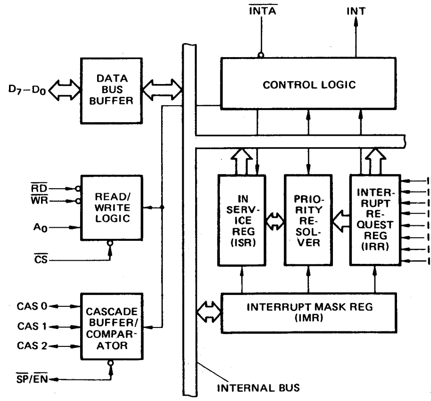


Fig. 4b–MBL 8259A BLOCK DIAGRAM



A_0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all MBL 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the MBL 8259A is used as a master and are inputs when the MBL 8259A is used as a slave. As a master, the MBL 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses. (See section "Cascading the MBL 8259A".)

INTERRUPT SEQUENCE

The powerful features of the MBL 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80*/85* system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The MBL 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The MBL 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the MBL 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the MBL 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the MBL 8259A. In the $\overline{\text{AEOI}}$ mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an MBL 8086 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The MBL 8259A does not drive the Data Bus during this cycle.
5. The MBL 8086 will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the MBL 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the $\overline{\text{AEOI}}$ mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the MBL 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

Fig. 4c—MBL 8259A BLOCK DIAGRAM

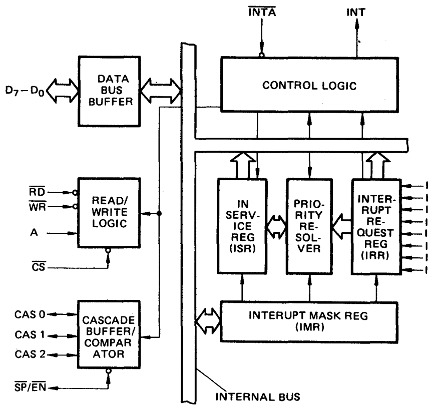
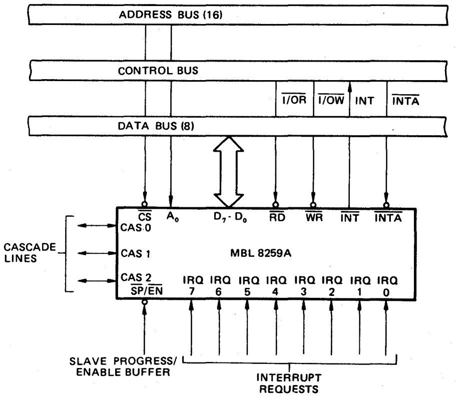


Fig. 5—MBL 8259A INTERFACE TO STANDARD SYSTEM BUS



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INTERRUPT SEQUENCE OUTPUTS

MCS-80*/MCS-85*

This sequence is timed by three INTA pulses. During the first INTA pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second INTA pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5—A_7 are programmed, while A_0—A_4 are automatically inserted by the MBL 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0—A_5 are automatically inserted.

Content of Second Interrupt Vactor Byte

IR	Interval=4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval=8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8—A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

MBL 8086/MBL 8088

MBL 8086 mode is similar to MCS-80* mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80*/85* systems in that the MBL 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in MBL 8086 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5—A_{11} are unused in MBL 8086 mode):

Content of Interrupt Vector Byte for MBL 8086 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

MBL 80186/MBL 80188

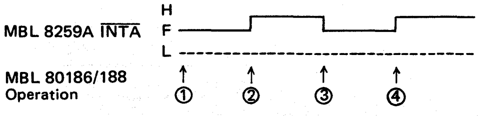
MBL 80186 mode is the same as MBL 8086 mode. However, it is noticed that an external pull-up resistor is required on the INTA pin of the MBL 8259A when it is connected to the MBL 80186/188 or Intel 80186/188.

When the INTA input pin of the MBL 8259A is connected to the INT2/INTA0 or INT3/INTA1 input/output pin of the MBL 80186/188 without an external pull-up resistor, the INTA pin floats after the MBL80186/188 is reset, because the INT2/INTA0 and INT3/INTA1 pins are floated (in the input state) by reset. Besides, the INTA pin is pulledup high after the INT2/INTA0 and INT3/INTA1 pins are set in the output state by software, because they output a high level in the output state when they are not activated.

In this case, a sequence of a processor's reset and setting the INT2/INTA0 or INT3/INTA1 in the output state generates a spurious negative pulse, and the MBL 8259A may recognize this pulse as an INTA pulse when the floating level is near to low level.

To avoid this problem, an external pull-up resistor must be connected on the INTA pin, so that the INTA pin is held high even after processor's reset.

MBL 8259A'S INTA LEVEL (WITHOUT EXTERNAL PULL-UP RESISTOR)



Notes: H = High level, F = Floating, L = Low level

①, ③ : Processor's reset (INT2/INTA0 and INT3/INTA1 in input state)

②, ④ : Processor's setting INT2/INTA0 and INT3/INTA1 in output state (not activated)

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PROGRAMMING THE MBL 8259A

The MBL 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each MBL 8259A in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. *Operation Command Words (OCWs):* These are the command words which command the MBL 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the MBL 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWs)

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode**, no Auto-EOI, MCS-80/85* system).

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

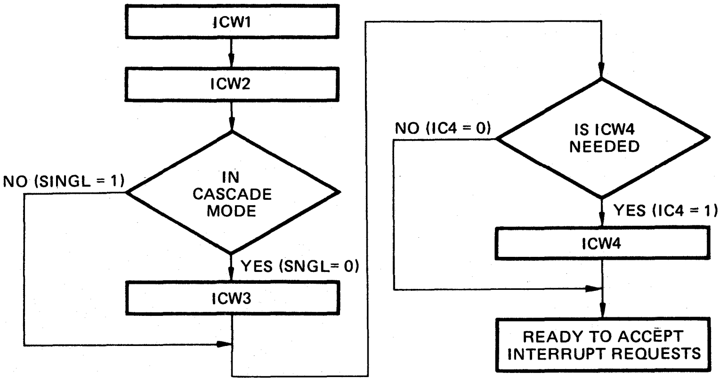
A_5-A_{15}: *Page starting address of service routines.* In an MCS-80*/85* system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the MBL 8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the MBL 8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MBL 8086 system $A_{15}-A_{11}$ are inserted in the five most significant bits of the vectoring byte and the MBL 8259A sets the three least significant bits according to the interrupt level. $A_{10}-A_5$ are ignored and ADI (Address interval) has no effect.

Fig. 6—INITIALIZATION SEQUENCE



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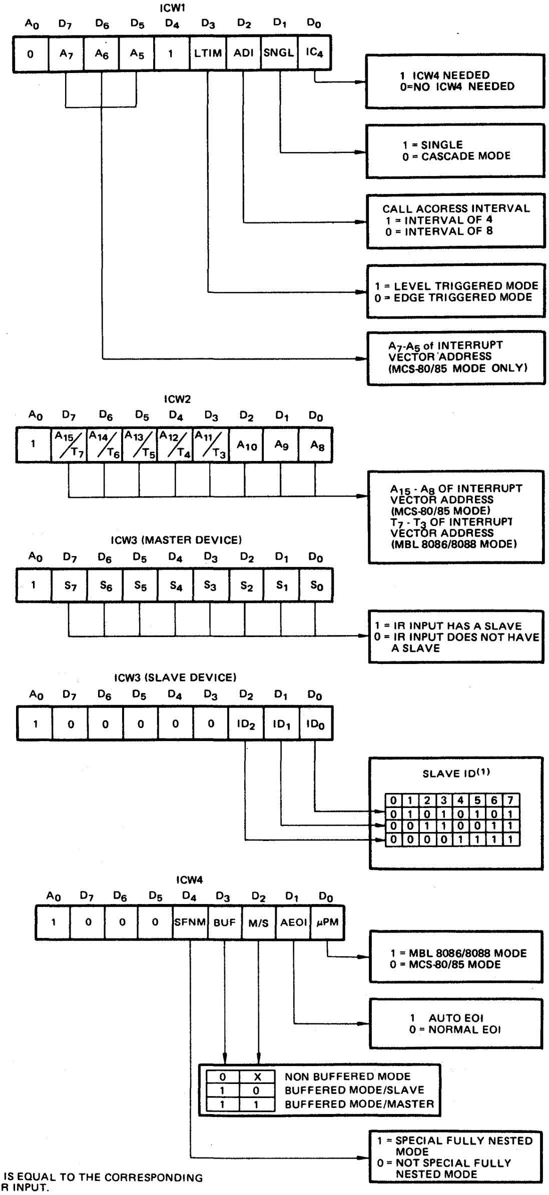
** Note: Master/Slave in ICW4 is only used in the buffered mode.

Fig. 7—INITIALIZATION COMMAND WORD FORMAT


ICW1
A0 D7 D6 D5 D4 D3 D2 D1 D0
0 A7 A6 A5 1 LTIM ADI SNGL IC4
1 ICW4 NEEDED
0=NO ICW4 NEEDED
1 = SINGLE
0 = CASCADE MODE
CALL ACORESS INTERVAL
1 = INTERVAL OF 4
0 = INTERVAL OF 8
1 = LEVEL TRIGGERED MODE
0 = EDGE TRIGGERED MODE
A7-A5 of INTERRUPT VECTOR ADDRESS (MCS-80/85 MODE ONLY)
ICW2
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 A15/T7 A14/T6 A13/T5 A12/T4 A11/T3 A10 A9 A8
A15 - A8 OF INTERRUPT VECTOR ADDRESS (MCS-80/85 MODE)
T7 - T3 OF INTERRUPT VECTOR ADDRESS (MBL 8086/8088 MODE)
ICW3 (MASTER DEVICE)
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 S7 S6 S5 S4 S3 S2 S1 S0
1 = IR INPUT HAS A SLAVE
0 = IR INPUT DOES NOT HAVE A SLAVE
ICW3 (SLAVE DEVICE)
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 ID2 ID1 ID0
SLAVE ID(1)
ICW4
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 SFNM BUF M/S AEOI μPM
1 = MBL 8086/8088 MODE
0 = MCS-80/85 MODE
1 AUTO EOI
0 = NORMAL EOI
1 = SPECIAL FULLY NESTED MODE
0 = NOT SPECIAL FULLY NESTED MODE

SLAVE ID(1)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

0	X	NON BUFFERED MODE
1	0	BUFFERED MODE/SLAVE
1	1	BUFFERED MODE/MASTER

NOTE 1: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

LTIM: If LTIM = 1, then the MBL 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI=1 then interval=4; ADI=0 then interval=8.

SNGL: Single.Means that this is the only MBL 8259A in the system. If SNGL = 1, no ICW3 will be issued.

IC4: If this bit is set, ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one MBL 8259A in the system and cascading is used, in which case SNGL=0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP=1, or in buffered mode when M/S=1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85* system) and will enable the corresponding slave to release bytes 2 and 3 (for MBL 8086 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$=0, or If BUF=1 and M/S=0 in ICW4) bits 2–0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for MBL 8086) are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM=1 the special fully nested mode is programmed.

BUF: If BUF=1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S=1 means the MBL 8259A is programmed to be a master, M/S=0 means the MBL 8259A is programmed to be a slave. If BUF=0, M/S has no function.

AEOI: If AEOI=1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM=0 sets the MBL 8259A for MCS-80*/85*system operation, μPM=1 sets the MBL 8259A for MBL 8086/8088 system operation.

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the MBL 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the MBL 8259A operation, a selection of algorithms can command the MBL 8259A to operate in various modes through the Operation Command Words (OCWs)

OPERATION CONTROL WORDS (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

0	R	SL	EOI	0	0	L2	L1	L0

OCW3

0	0	ESMM	SMM	0	1	P	RR	RIS

OPERATION CONTROL WORD 1 (OCWs)

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). M_7–M_0 represent the eight mask bits. M=1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI – These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

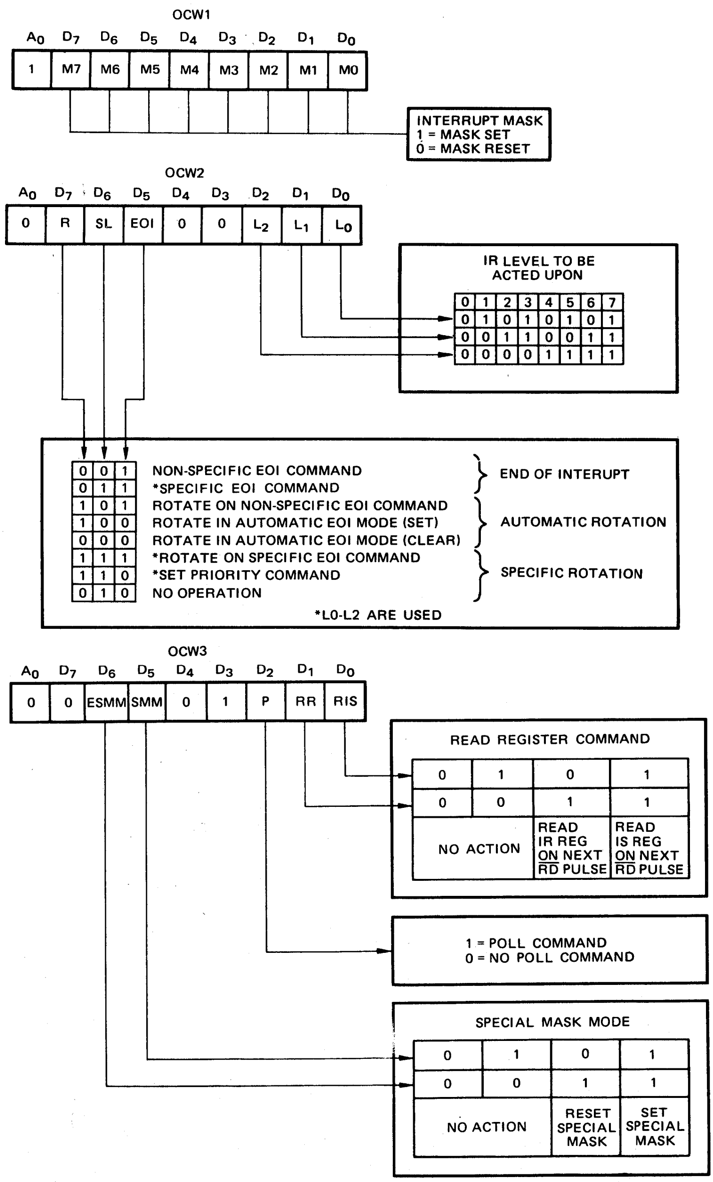
L_2, L_1, L_0–These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM – Enable Special Mask Mode. When this bit is set to 1, it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0 the SMM bit becomes a "don't care".

SMM – Special Mask Mode. If ESMM=1 and SMM=1 the MBL 8259A will enter Special Mask Mode. If ESMM=1 and SMM=0 the MBL 8259A will revert to normal mask mode. When ESMM=0, SMM has no effect.

Fig. 8—OPERATION COMMAND WORD FORMAT



OCW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M7	M6	M5	M4	M3	M2	M1	M0

INTERRUPT MASK
1 = MASK SET
0 = MASK RESET

OCW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	R	SL	EOI	0	0	L_2	L_1	L_0

IR LEVEL TO BE ACTED UPON

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

R	SL	EOI		
0	0	1	NON-SPECIFIC EOI COMMAND	END OF INTERUPT
0	1	1	*SPECIFIC EOI COMMAND	
1	0	1	ROTATE ON NON-SPECIFIC EOI COMMAND	AUTOMATIC ROTATION
1	0	0	ROTATE IN AUTOMATIC EOI MODE (SET)	
0	0	0	ROTATE IN AUTOMATIC EOI MODE (CLEAR)	
1	1	1	*ROTATE ON SPECIFIC EOI COMMAND	SPECIFIC ROTATION
1	1	0	*SET PRIORITY COMMAND	
0	1	0	NO OPERATION	

*L0-L2 ARE USED

OCW3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	ESMM	SMM	0	1	P	RR	RIS

READ REGISTER COMMAND

RIS	0	1	0	1
RR	0	0	1	1
	NO ACTION		READ IR REG ON NEXT $\overline{RD}$ PULSE	READ IS REG ON NEXT $\overline{RD}$ PULSE

1 = POLL COMMAND
0 = NO POLL COMMAND

SPECIAL MASK MODE

SMM	0	1	0	1
ESMM	0	0	1	1
	NO ACTION		RESET SPECIAL MASK	SET SPECIAL MASK

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service Register (ISR0-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the training edge of the last $\overline{\text{INTA}}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

END OF INTERRUPT (EOI)

The In-Service (IS) bit can be reset either automatically following the training edge of the last in sequence $\overline{\text{INTA}}$ pulse (when AEOI bit in ICW4 is set) or by a command word that must be issued to the MBL 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the MBL 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the MBL 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the MBL 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the MBL 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI=1 in ICW4, then the MBL 8259A will operated in AEOI mode continuously until reprogrammed by ICW4. In this mode the MBL 8259A will automatically perform a non-specific EOI operation at the training edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85*, second in MBL 8086/8088). Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single MBL 8259A.

The AEOI mode can only be used in a master MBL 8259A and not a slave.

AUTOMATIC ROTATION
(Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0
	Lowest Priority							Highest Priority
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	0	0	0	0	0
			Highest Priority	Lowest Priority				
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0) and cleared by (R=0, SL=0, EOI=0).

SPECIFIC ROTATION
(Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and L0-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking and IR channel does not affect the other channels operation.

* Trade Mark of Intel Corporation

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e. while executing a service routine), the MBL 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: ESMM = 1, SMM = 1, and cleared where ESMM = 1, SMM = 0.

POLL COMMAND

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is Issued by setting P = "1" in OCW3. The MBL 8259A treats the next $\overline{RD}$ pulse to the MBL 8259A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

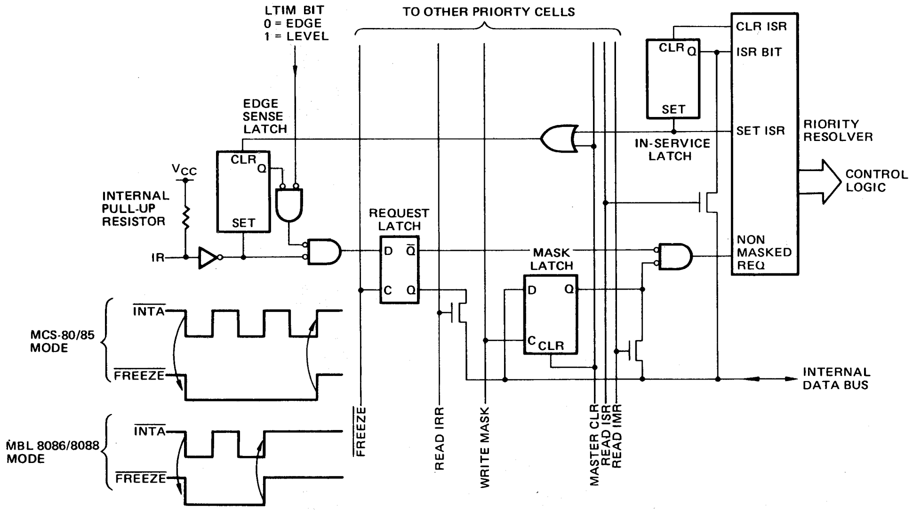
The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
1	–	–	–	–	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.
1: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

Fig. 9—PRIORITY CELL—SIMPLIFIED LOGIC DIAGRAM



NOTES:
1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. $\overline{FREEZE}$ IS ACTIVE DURING $\overline{INTA}$ AND POLL SEQUENCES ONLY
3. TRUTH TABLE FOR D-LATCH

C	D	Q	OPERATION
1	Di	Di	FOLLOW
0	X	Qn-1	HOLD

READING THE MBL 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register (IMR): 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=0.)

The ISR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the MBL 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the MBL 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0=1 (OCW1).

Polling overrides status read when P=1, RR=1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

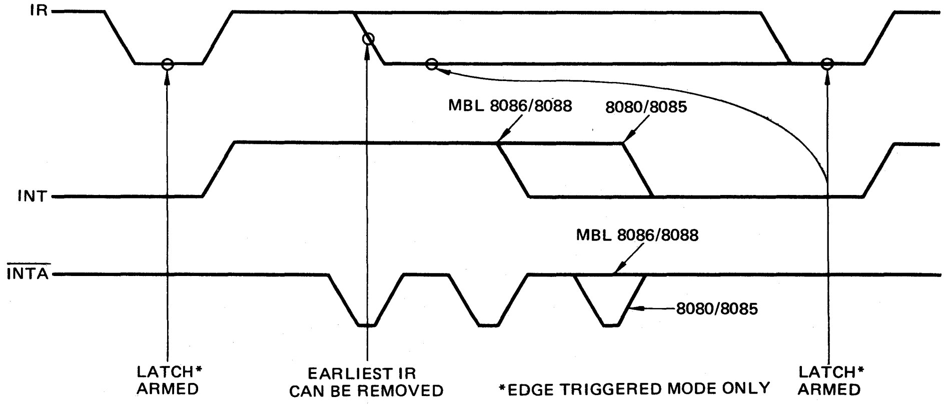
If LTIM='0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM='1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuity of the MBL 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first $\overline{INTA}$. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

Fig. 10—IR TRIGGERING TIMING REQUIREMENTS



THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the MBL 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the MBL 8259A to send an enable signal on $\overline{\text{SP}}/\overline{\text{EN}}$ to enable the buffers. In this mode, whenever the MBL 8259A's data bus outputs are enabled, the $\overline{\text{SP}}/\overline{\text{EN}}$ output becomes active.

This modification forces the use of software programming to determine whether the MBL 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master of a slave.

CASCADE MODE

The MBL 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

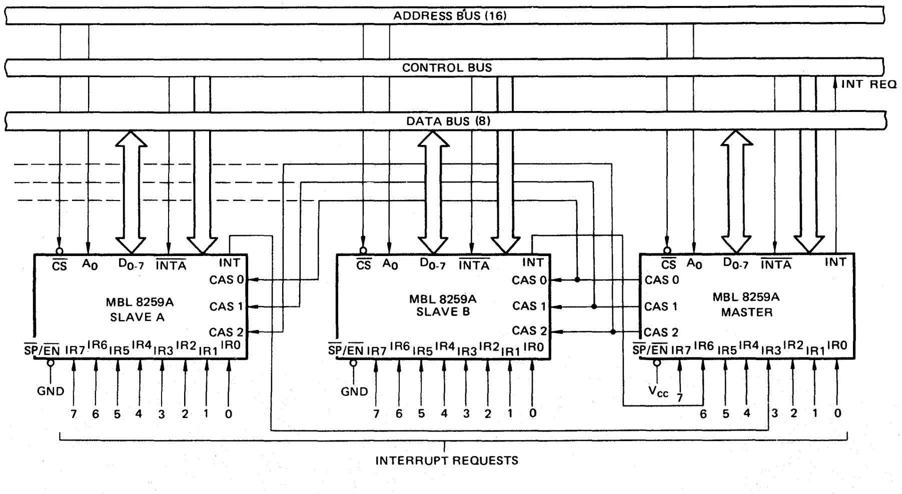
The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{\text{INTA}}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{\text{INTA}}$. (Byte 2 only for MBL 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{\text{INTA}}$ pulse to the trailing edge of the third pulse. Each MBL 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ($\overline{\text{CS}}$) input of each MBL 8259A.

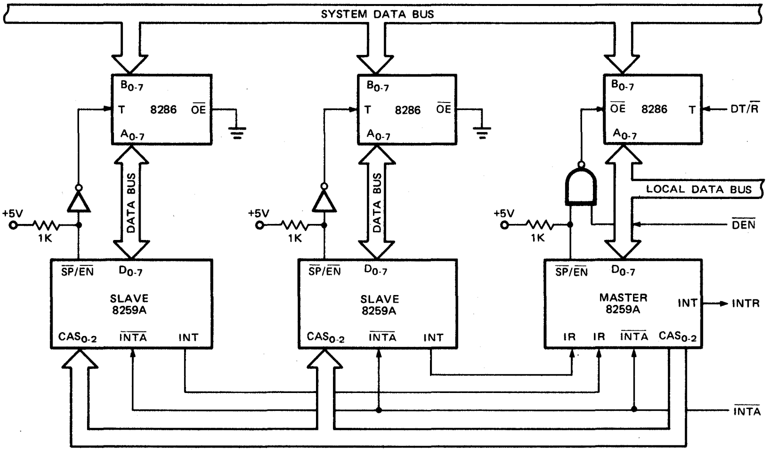
The cascade lines of the Master MBL 8259A are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

Fig. 11 – CASCADING THE MBL 8259A (22 INTERRUPT LEVELS)



Special consideration should be taken when mixed interrupt requests are assigned to a master 8259A; that is, when some of the master's IR inputs are used for slave interrupt requests and some are used for individual interrupt requests. In this type of structure, the master's IR0 must not be used for a slave. This is because when an IR input that isn't initialized as a slave receives an interrupt request, the CAS0-2 lines won't be activated, thus staying in the default condition addressing for IR0 (slave IR0). If a slave is connected to the master's IR0 when a non-slave interrupt occurs on another master IR input, erroneous conditions may result. Thus IR0 should be the last choice when assigning slaves to IR inputs.
(© Intel Corporation, 1979)

Fig. 12 – CASCADE-BUFFERED MODE EXAMPLE



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ABSOLUTE MAXIMUM RATING*

Ambient Temperature Under Blas	0°C to 70°C
Storage Temperature	-55°C to +150°C
Voltage on Any Pin with Respect ot Ground	-0.5V to +7V
Power Dissipation	1 W

*NOTE:- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = -100μA
		2.4		V	I_{OH} = -400μA
I_{LI}	Input Load Current	-10	+10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LOL}	Output Leakage Current	-10	+10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		-300	μA	V_{IN} = 0V
			10	μA	V_{IN} = V_{CC}

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

TIMING REQUIREMENTS

Symbol	Parameter	MBL 8259A		MBL 8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	0		0		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	0		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	235		160		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$↓	0		0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	0		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	290		190		ns	
TDVWH	Data Setup to $\overline{WR}$↑	240		160		ns	
TWHDX	Data Hold after $\overline{WR}$↑	0		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slvae Only)	55		40		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		190		ns	
*TCHCL	End of Command to next Command (Not same command type)	500		500		ns	
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.						

*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. Intel 8085A = 1.6μs, Intel 8085A-2 = 1μs, MBL 8086 = 1μs, MBL 8086-2 = 625 ns)

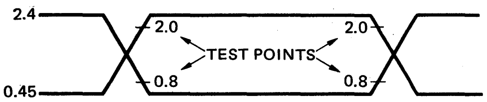
NOTE: This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

Symbol	Parameter	MBL 8259A		MBL 8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TRLDV	Data Valid from $\overline{RD}/\overline{INTA}$↓		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}/\overline{INTA}$↑	10	100	10	85	ns	C of Data Bus Max. text C = 100pF Min. text C = 15pF
TJHIH	Interrupt Output Delay		350		300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$↓ (Master Only)		565		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		125		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		150		150	ns	
TAHDV	Data Valid from Stable Address		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		200	ns	

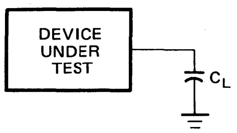
A.C. TESTING INPUT/OUTPUT WAVEFORM

INPUT/OUTPUT



AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

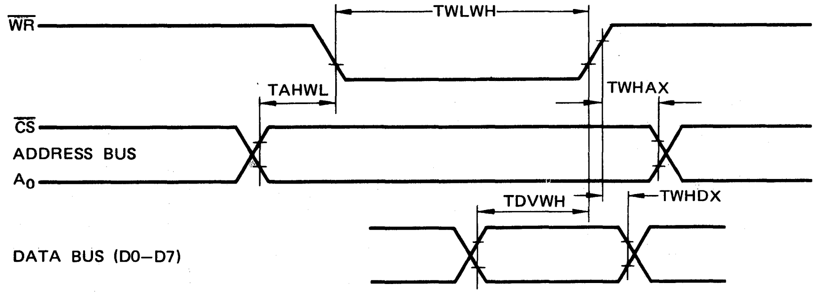
A.C. TESTING LOAD CIRCUIT



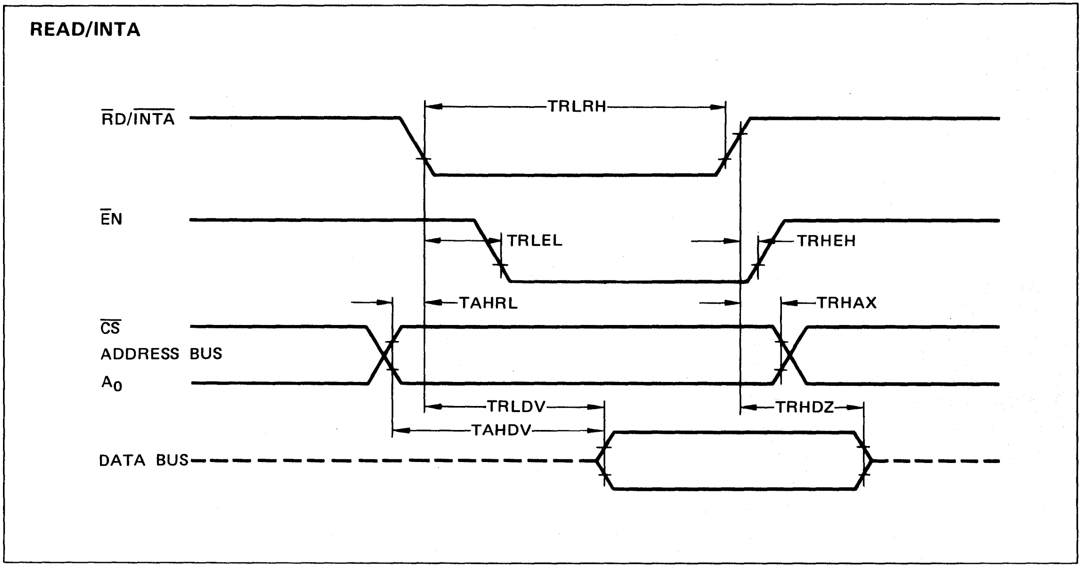
C_L= 100_{pF}
(C_L INCLUDES JIG CAPACITANCE)

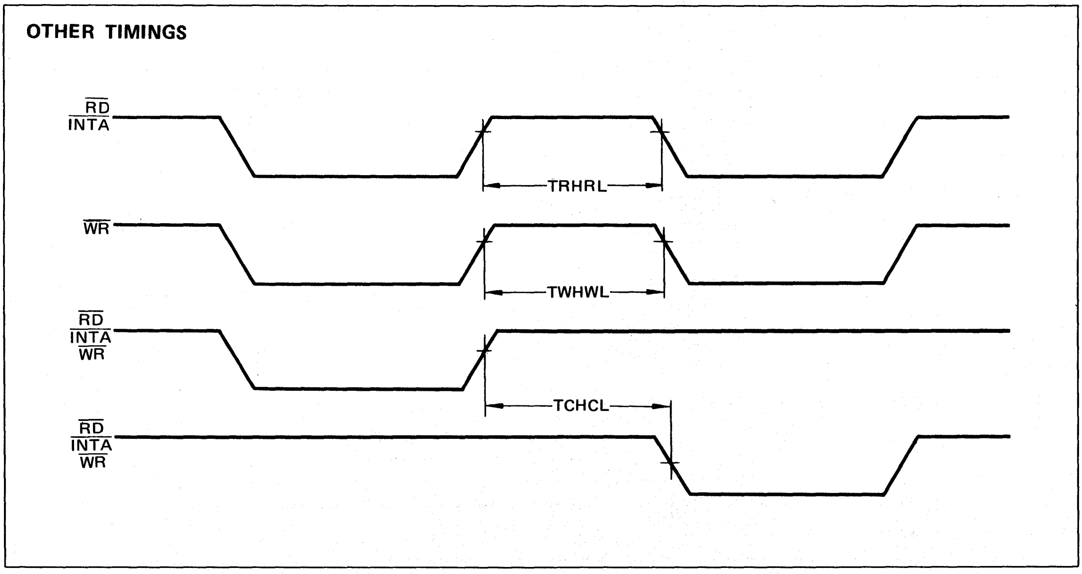
WAVEFORMS

WRITE

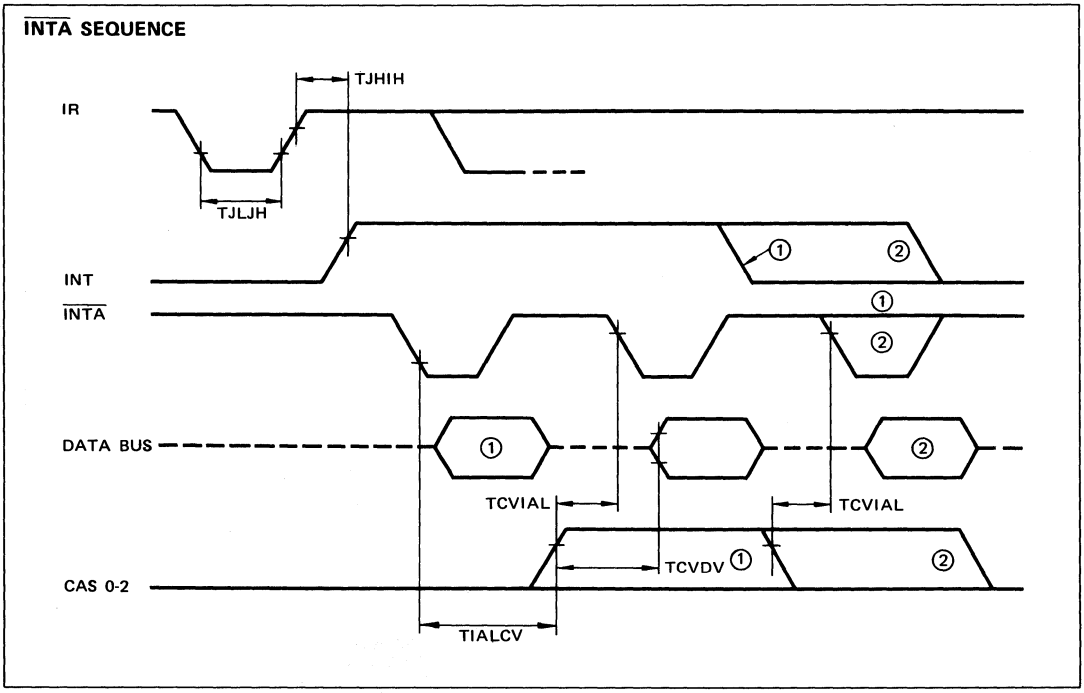


WAVEFORMS (Continued)





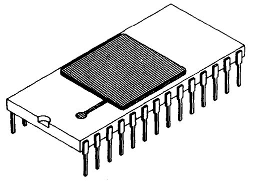
WAVEFORMS (Continued)



NOTES: Interrupt output must remain HIGH at least until leading edge of first $\overline{\text{INTA}}$.
① MBL 8086/8088 system mode: at first $\overline{\text{INTA}}$ the Data Bus is not active.
② 8080/8085 system mode: only.

PACKAGE ILLUSTRATION

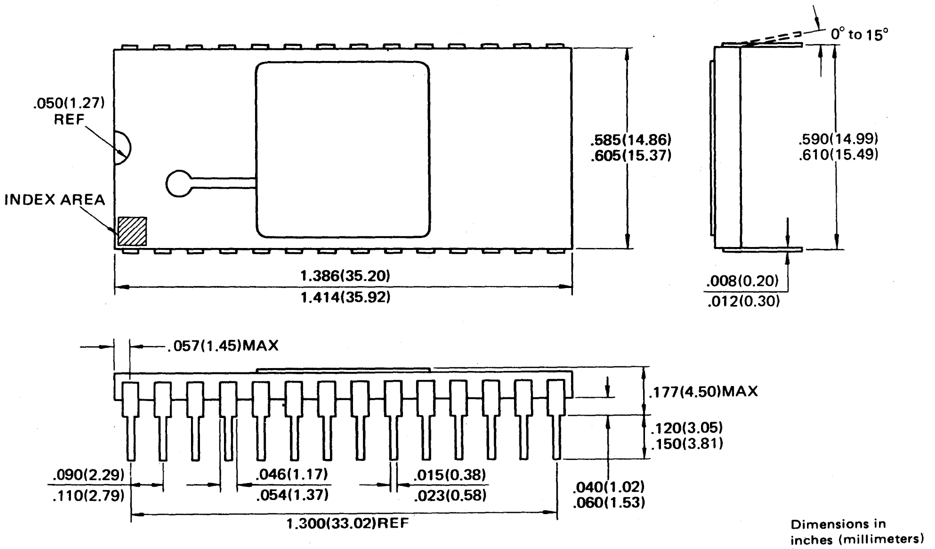
CERAMIC DIP
(Metal Seal)



PLASTIC DIMENSIONS

CERAMIC DIP(Suffix: -C)

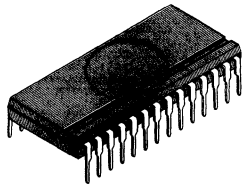
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No. : DIP-28C-A01)



Dimensions in
inches (millimeters)

PACKAGE ILLUSTRATION

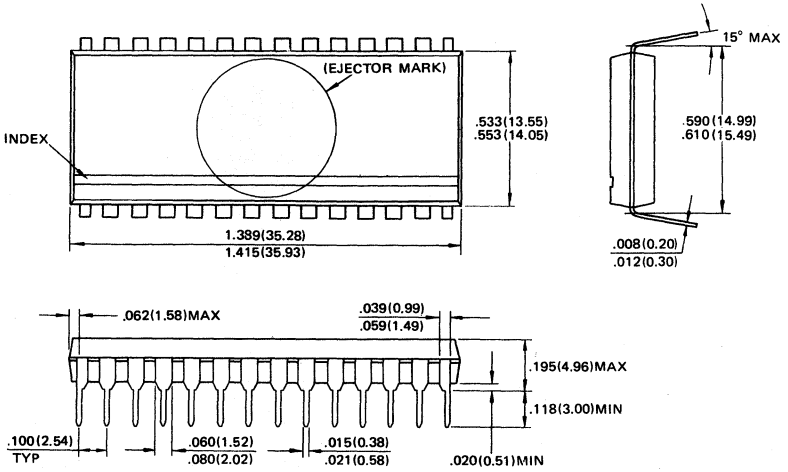
PLASTIC DIP
(Plastic Molding)



PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



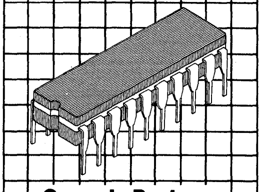
Dimensions in
inches (millimeters)

MBL8282 MBL8283
Bipolar Octal Latch

November 1986
Edition 4.0

Description

The MBL8282 and MBL8283 are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers or multiplexers. The MBL8283 inverts the input data at its outputs while the MBL8282 does not. Thus, all of the principle peripherals and input/output functions of a microcomputer system can be implemented with these devices.

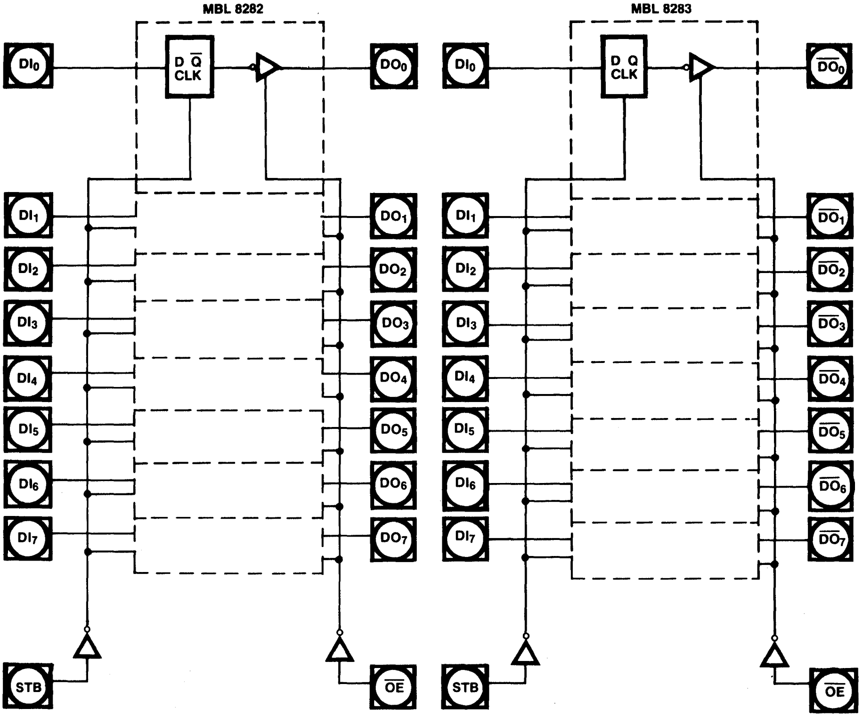


Ceramic Package DIP-20C-C01

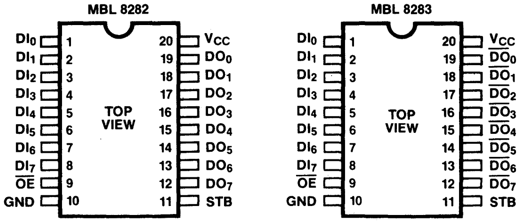
Features

- **Address Latch for MBL8086, MBL8088, MBL8089, MCS-80*, MCS-85*, MCS-48* Families**
- **High Output Drive Capability for Driving System Data Bus**
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Transparent during Active Strobe**
- **3-State Outputs**
- **20-Pin DIP Package**
- **No Output Low Noise when Entering or Leaving High Impedance State**

Logic Diagrams



Pin Configurations



Functional Description

The MBL8282 and MBL8283 are 8-bit latches with 3-state output buffers. Data having satisfied the setup time requirements is clocked into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent. Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

Pin Description

Pin	Description
STB	STROBE (Input). STB is an input control pulse used to strobe data at the data input pins (A_0-A_7) into the data latches. This signal is active to HIGH to allow data in. The data is latched during the HIGH to LOW transition of STB.
$\overline{OE}$	OUTPUT ENABLE (Input) $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches to be sent to the data output pins (B_0-B_7). $\overline{OE}$ being inactive HIGH forces the output buffers to their high impedance state.
DI_0-DI_7	DATA INPUT PINS (Input). Data present at these pins is clocked into the data input latches when STB is strobed.
DO_0-DO_7 (MBL 8282) $\overline{DO}_0$-$\overline{DO}_7$ (MBL8283)	DATA OUTPUT PINS (Output). When $\overline{OE}$ is low, the data in the data latches appears as inverted (MBL8283) or non-inverted (MBL8282) data on the data output pins.

Absolute Maximum Ratings*

Parameter	Rating	Unit
Temperature Under Bias	0° to 70°	°C
Storage Temperature	-65° to +150°	°C
Supply Voltage	-0.5 to +7.0	V
All Input Voltages	-0.5 to +7.0	V
All Output Voltages (3-State Output)	+5.5	V
Power Dissipation	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_C	Input Clamp Voltage		-1	V	I_C = -5 mA
I_{CC}	Power Supply Current		160	mA	
I_F	Forward Input Current		-0.2	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	V_R = 5.25V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 32 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -5 mA
I_{OFF}	Output Off Current		±50	μA	V_{OFF} = 0.45V to 5.25V
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = 5.0V See Note 1
V_{IH}	Input High Voltage	2.0		V	V_{CC} = 5.0V See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

Note:
1. Output Loading I_{OL} = 32mA, I_{OH} = -5mA, C_L = 300pF.

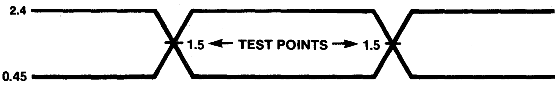
A.C. Characteristics

(V_{CC} = 5V ±10%, T_A = 0°C to 70°C, Loading: Outputs— I_{OL} = 32mA, I_{OH} = -5mA, C_L = 300pF)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TIVOV	Input to Output Delay				(See Note 1)
	—Inverting (MBL8283)	5	22	ns	
	—Non-Inverting (MBL8282)	5	30	ns	
TSHOV	STB to Output Delay				
	—Inverting (MBL8283)	10	40	ns	
	—Non-Inverting (MBL8282)	10	45	ns	
TEHOZ	Output Disable Time	5	18	ns	
TELOV	Output Enable Time	10	30	ns	
TIVSL	Input to STB Setup Time	0		ns	
TSLIX	Input to STB Hold Time	25		ns	
TSHSL	STB High Time	15		ns	
TILIH, TOLOH	Input, Output Rise Time		20	ns	From 0.8V to 2.0V
TIHIL, TOHOL	Input, Output Fall Time		12	ns	From 2.0V to 0.8V

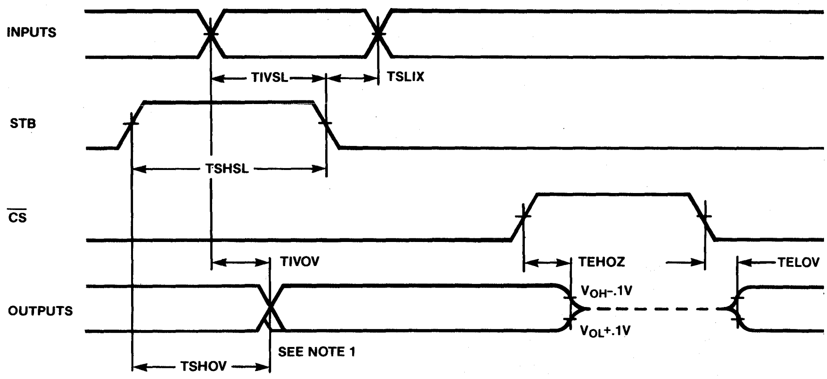
Note:
1. See waveforms and test load circuit on following page.

A.C. Testing Input/ Output Waveform



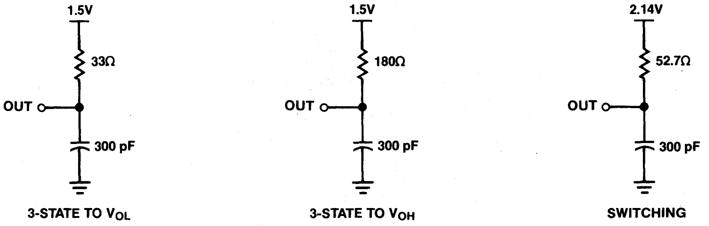
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0". INPUT RISE AND FALL TIMES ARE MEASURED FROM).8V TO 2.0V AND ARE DRIVEN AT 5±2ns.

Waveforms

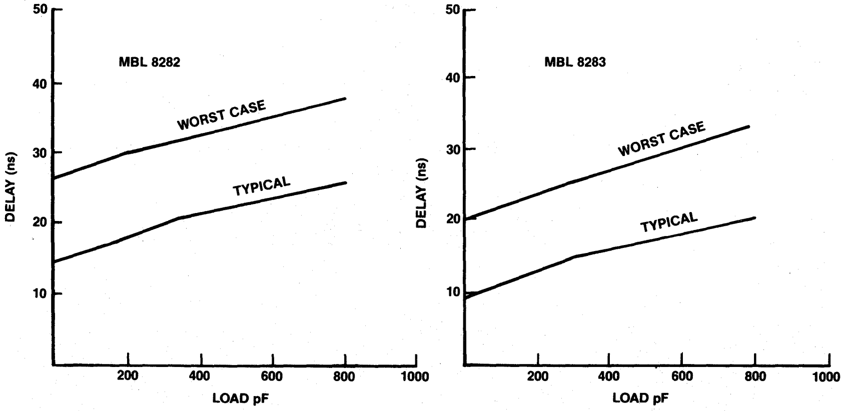


NOTE: 1. FOR MBL 8283 ONLY—OUTPUT MAY BE MOMENTARILY INVALID FOLLOWING THE HIGH GOING STB TRANSITION.
2. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

Output Test Load Circuits



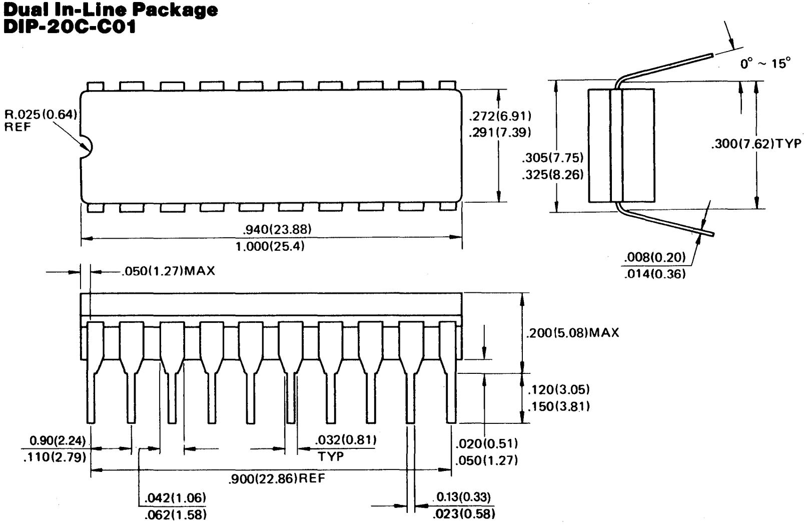
Output Delay vs. Capacitance



Package Dimensions

Dimensions in inches (millimeters)

20-Lead Ceramic Dual In-Line Package DIP-20C-C01



FUJITSU

BIPOLAR CLOCK GENERATOR/DRIVER

MBL 8284A MBL 8284A-1

April 1986
Edition 4.0

BIPOLAR CLOCK GENERATOR AND DRIVER FOR MBL 8086/8088/8089

- **Generates the System Clock for the MBL 8086/8088/8089 Processors:**
  5MHz and 8MHz with MBL 8284A
  10MHz with MBL 8284A-1
- **Uses a Crystal or a TTL Signal for Frequency Source**
- **Provides Local READY and Multibus* READY Synchronization**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Capable of Clock Synchronization with Other MBL 8284As**
- **Single +5V Power Supply**
- **18-Pin Cerdip (Suffix: -CZ)**

Fig. 1 BLOCK DIAGRAM

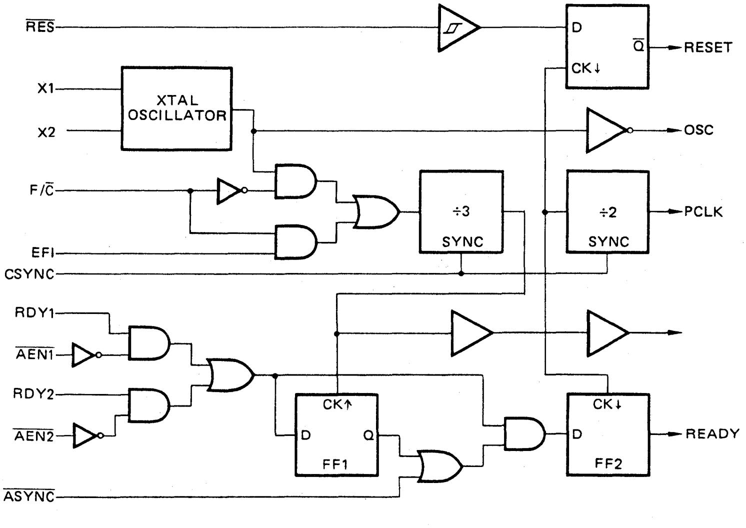
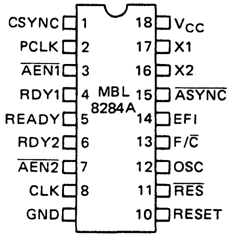


Fig. 2 – PIN CONFIGURATION



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PIN DESCRIPTION

TABLE 1 – PIN DISCRIPTION

Symbol	Type	Name and Function
$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$	I	**Address Enable:** $\overline{\text{AEN}}$ is an active LOW signal. $\overline{\text{AEN}}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{\text{AEN1}}$ validates RDY1 while $\overline{\text{AEN2}}$ validates RDY2. Two $\overline{\text{AEN}}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{\text{AEN}}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**Bus Ready:** (Transfer Complete), RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{\text{AEN1}}$ while RDY2 is qualified by $\overline{\text{AEN2}}$.
$\overline{\text{ASYNC}}$	I	**Ready Synchronization Select:** $\overline{\text{ASYNC}}$ is an input which defines the synchronization mode of the READY logic. When $\overline{\text{ASYNC}}$ is low, two stages of READY synchronization are provided. When $\overline{\text{ASYNC}}$ is left open (internal pull-up resistor is provided.) or HIGH a single stage of READY synchronization is provided.
READY	O	**Ready:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{\text{C}}$	I	**Frequency/Crystal Select:** F/$\overline{\text{C}}$ is a strapping option. When strapped LOW, F/$\overline{\text{C}}$ permits the processor's clock to be generated by the crystal. When F/$\overline{\text{C}}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**External Frequency:** When F/$\overline{\text{C}}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	**Processor Clock:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{\text{RES}}$	I	**Reset In:** $\overline{\text{RES}}$ is an active LOW signal which is used to generate RESET. The MBL 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**Reset:** RESET is an active HIGH signal which is used to reset the MBL 8086 family processors, its timing characteristics are determined by $\overline{\text{RES}}$.
CSYNC	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple MBL 8284A to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**Ground.**
V_{CC}		**Power:** +5V supply.

FUNCTIONAL DESCRIPTION

GENERAL

The MBL 8284A is a single chip clock generator/driver for the MBL 8086/MBL 8088/MBL 8089 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS* "Ready" synchronization and reset logic. Refer to Figure 1 for Block Diagram and Figure 2 for Pin Configuration.

OSCILLATOR

The oscillator circuit of the MBL 8284A is designed primarily for use with an external series resonant, fundamental mode, crystal from which the basic operating frequency is derived.
The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors (R_1 = R_2 = 510Ω) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

For systems which have a V_{CC} ramp time ⩾ 1V/ms and/or have inherent board capacitance between X1 or X2, exceeding 10pF (not including MBL 8284A pin capacitance), the two 510Ω resistors should be used. This circuit provides optimum stability for the oscillator in such extreme conditions. It is advisable to limit stray capacitances to less than 10pF on X1 and X2 to minimize deviation from operating at the fundamental frequency. For notes of using MBL 8284A, see page 10.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another MBL 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the MBL 8284A. This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the MBL 8086/MBL 8088/MBL 8089 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK, PCLK has a 50% duty cycle.

RESET LOGIC

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the MBL 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

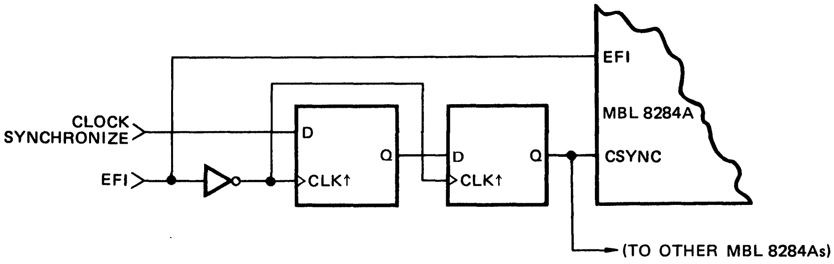
When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

* Trade Mark of Intel Corporation, USA

Fig. 3 – CSYNC SYNCHRONIZATION



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Supply Voltages	-0.5V to +7.0V
All Input and Output Voltages	-0.5V to V_{CC}
Power Dissipation	1.0 W

* NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Test Conditions
I_F	Forward Input Current	$\overline{\text{ASYNC}}$ Other Inputs		-1.3 -0.5	mA mA	V_F = 0.45V V_F = 0.45V
I_R	Reverse Input Current	$\overline{\text{ASYNC}}$ Other Inputs		50 50	μA μA	$V_R = V_{CC}$ V_R = 5.25V
V_C	Input Forward Clamp Voltage			-1.0	V	I_C = -5mA
I_{CC}	Power Supply Current			162	mA	
V_{IL}	Input LOW Voltage			0.8	V	
V_{IH}	Input HIGH Voltage		2.0		V	
V_{IHR}	Reset Input HIGH Voltage		2.6		V	
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 5mA
V_{OH}	Output HIGH Voltage	CLK Other Outputs	4 2.4		V V	I_{OH} = -1mA I_{OH} = -1mA
$V_{IHR}-V_{ILR}$	$\overline{\text{RES}}$ Input Hysteresis		0.25		V	

A.C. CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to 70°C)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	(90% - 90%)V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	(10% - 10%)V_{IN}
t_{ELEL}	EFI Period (Note 1)	40 33		ns	For MBL 8284A For MBL 8284A-1
	XTAL Frequency	12	25 30	MHz	For MBL 8284A For MBL 8284A-1
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{\text{ASYNC}}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{\text{ASYNC}}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{\text{ASYNC}}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{\text{ASYNC}}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	10		ns	
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$		ns	
t_{I1HCL}	$\overline{\text{RES}}$ Setup to CLK	65		ns	(Note 1)
t_{CLI1H}	$\overline{\text{RES}}$ Hold to CLK	20		ns	(Note 1)

A.C. CHARACTERISTICS (Continued)

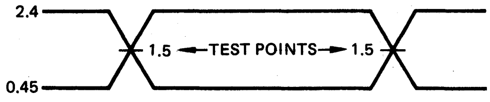
TIMING RESPONSES

Symbol	Parameter	MBL 8284A Min.	MBL 8284A-1 Min.	Max.	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125	100		ns	
t_{CHCL}	CLK HIGH Time	$(\frac{1}{3} t_{CLCL})+2$	39		ns	
t_{CLCH}	CLK LOW Time	$(\frac{2}{3} t_{CLCL})-15$	53		ns	
t_{CH1CH2}	CLK Rise Time			10	ns	From 1.0V to 3.5V
t_{CL2CL2}	CLK Fall time			10	ns	From 3.5V to 1.0V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{RYLCL}	Ready Inactive to CLK	-8	-8		ns	(Note 3)
t_{RYHCH}	Ready Active to CLK	$(\frac{2}{3} t_{CLCL})-15$	53		ns	(Note 2)
t_{CLIL}	CLK to Reset Delay			40	ns	
t_{CLPH}	CLK to PCLK HIGH Delay			22	ns	
t_{CLPL}	CLK to PCLK LOW Delay			22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	-5	-5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	-2	35	ns	
t_{OLOH}	Output Rise Time (except CLK)			20	ns	From 0.8V to 2.0V
t_{OHOL}	Output Fall Time (except CLK)			12	ns	From 2.0V to 0.8V

NOTES:

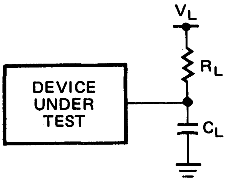
1. Setup and hold necessary only to guarantee recognition at next clock.
2. Applies only to T_3 and T_w states.
3. Applies only to T_2 states.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".timing measurements are made at 1.5V for both a logic "1" and "0". Input rise and fall times (measured between 0.8V and 2.0V) are 5±2ns.

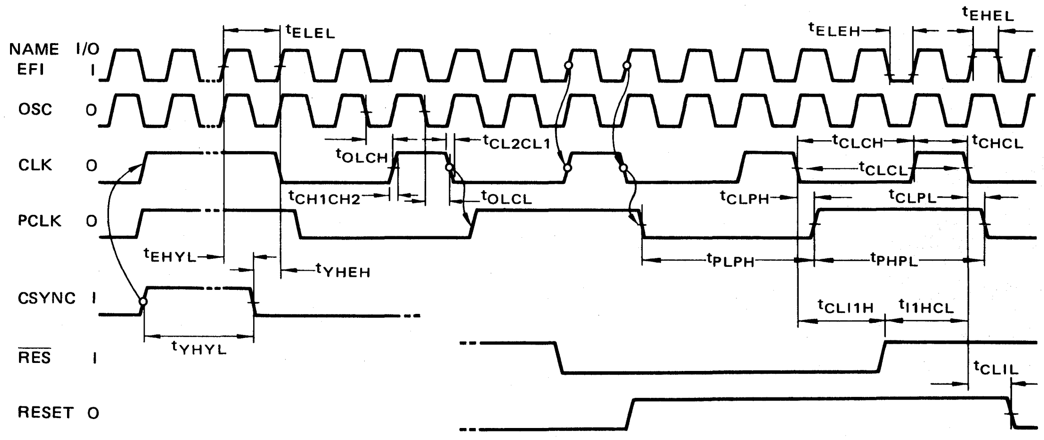
A.C. TESTING LOAD CIRCUIT



	V_L(V)	R_L(Ω)	C_L(pF)
CLK	3.41V	590	100
READY	2.08V	325	30

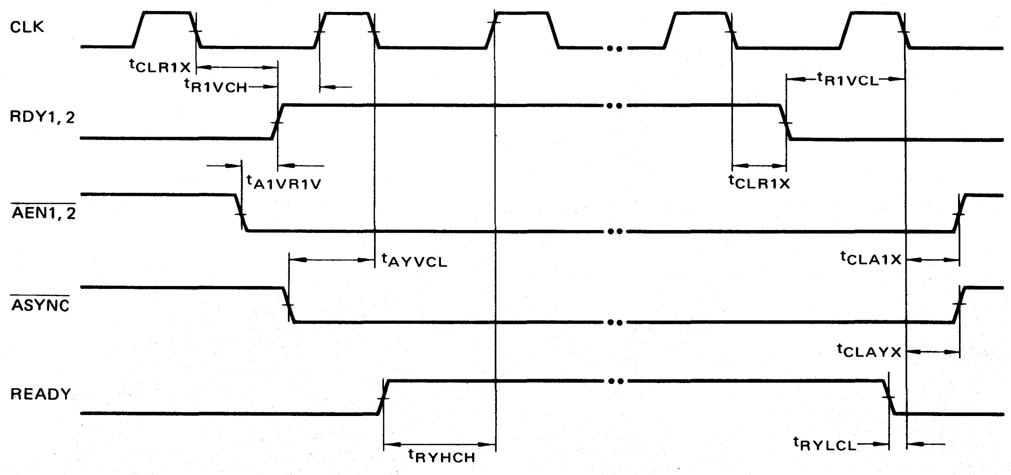
WAVEFORMS

CLOCKS AND RESET SIGNALS

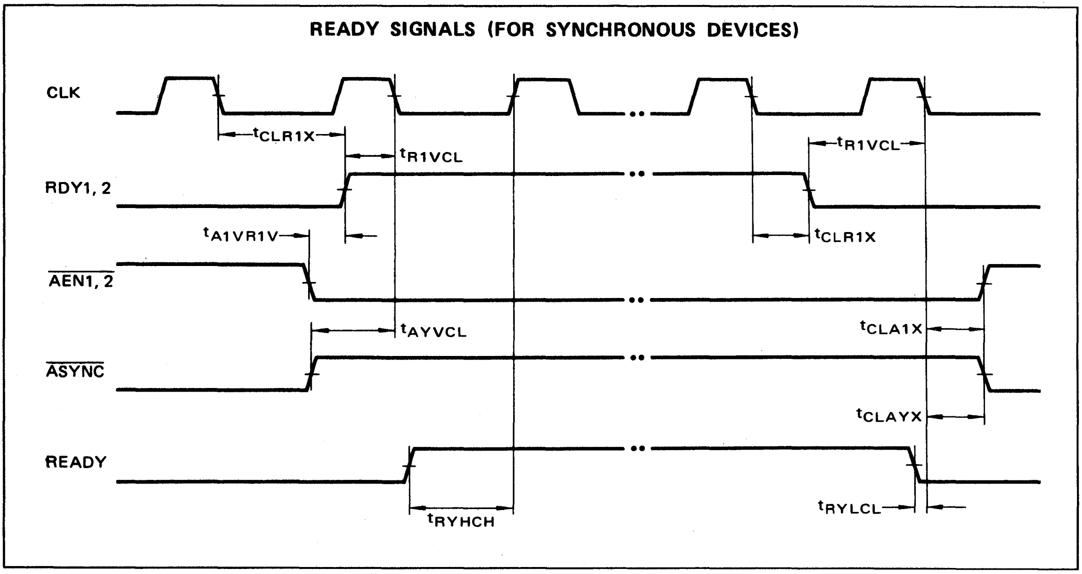


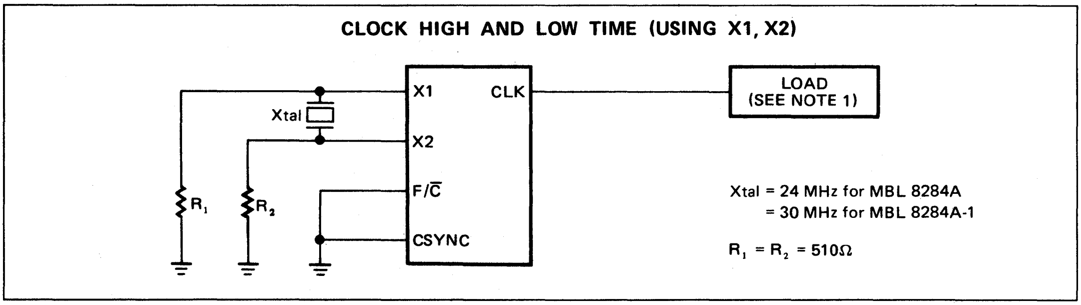
NOTE: All timing measurements are made at 1.5 volts, unless otherwise noted.

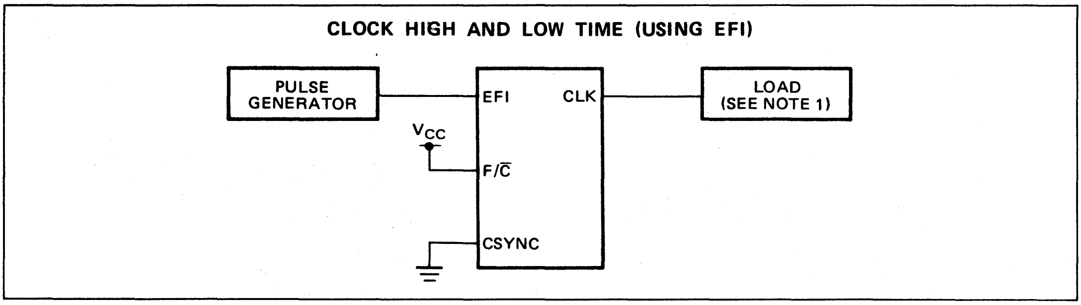
READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



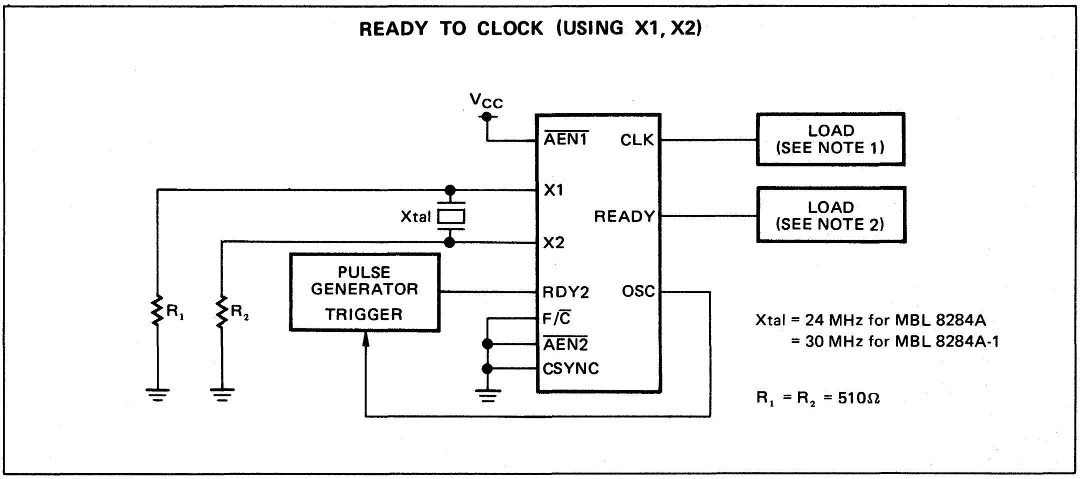
WAVEFORMS (Continued)



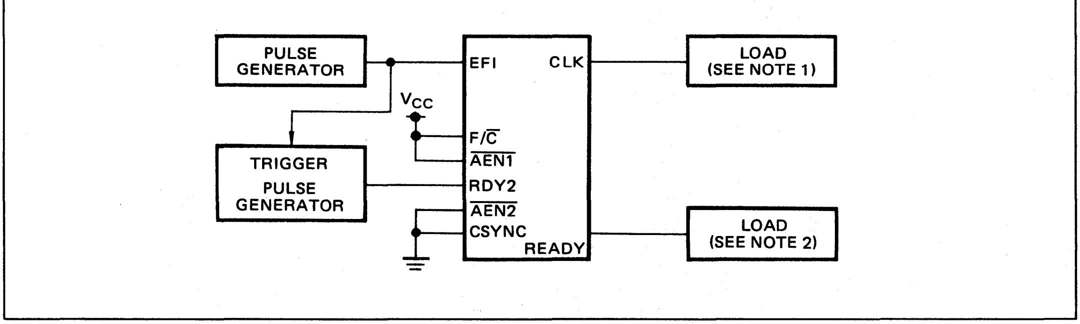




READY TO CLOCK (USING X1, X2)



READY TO CLOCK (USING EFI)



NOTES:

1. C_L = 100 pF
2. C_L = 30 pF

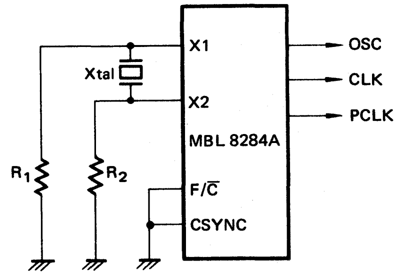
NOTES FOR USING MBL 8284A

For MBL 8284A's stable operation, the following things should be noted:

1. The fundamental mode crystal should be used.
2. Stray capacitances between X1 and X2 should be limited to less than 10pF.
3. External resistors for stable crystal oscillation should be connected as Configuration (I) or (II) shown below. Especially, for Configuration (I) circuit, the minimum frequency of crystal is limitted to 15MHz. A low frequency crystal (less than 15MHz) with Configuration (I) circuit may cause an abnormal oscillation. For more stable osciallation over the specified frequency range (12MHz to 25MHz or 30MHz), Configuration (II) circuit is recommendable.
4. The rise time of the power supply voltage V_{CC} should be more than 10ms. A steep V_{CC} rising (with the rise time less than 10ms) may cause an overtone oscillation.
5. In the power-on reset circuit shown below, the ground terminal of the external capacitor C should be grounded as near to the GND pin of MBL 8284A as possible.
6. When the crystal oscillator circuit is not used (i.e., an external clock source is used), X1 should be pulled up to V_{CC} with an approx. 1kΩ resistor and X2 should be left open. At this time, OSC output is clamped at high level.

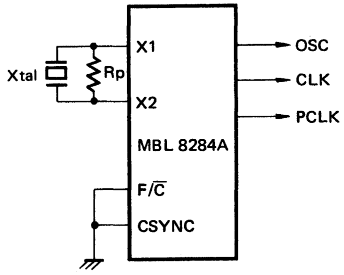
CRYSTAL OSCILLATOR CIRCUIT

• Configuration (I)



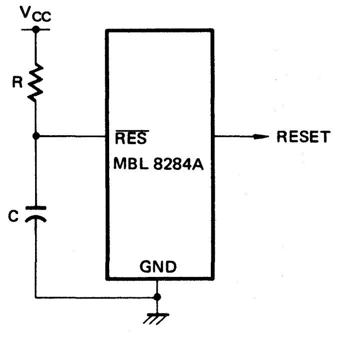
$R_1 = R_2 = 510\Omega$, Xtal = 15MHz to 25MHz (MBL 8284A)
= 15MHz to 30MHz (MBL 8284A-1)

• Configuration (II)

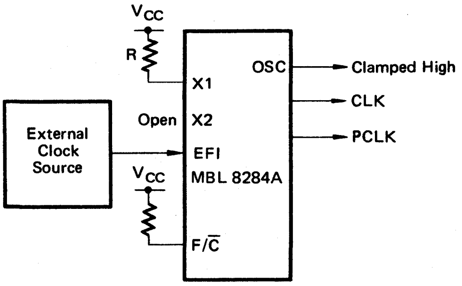


$R_p = 510\Omega$, Xtal = 12MHz to 25MHz (MBL 8284A)
= 12MHz to 30MHz (MBL 8284A-1)

POWER-ON RESET CIRCUIT



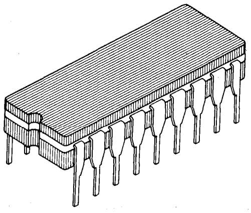
EXTERNAL CLOCK CONFIGURATION



R = 1kΩ, EFI ≤ 25MHz (MBL 8284A)
≤ 30MHz (MBL 8284A-1)

PACKAGE ILLUSTRATION

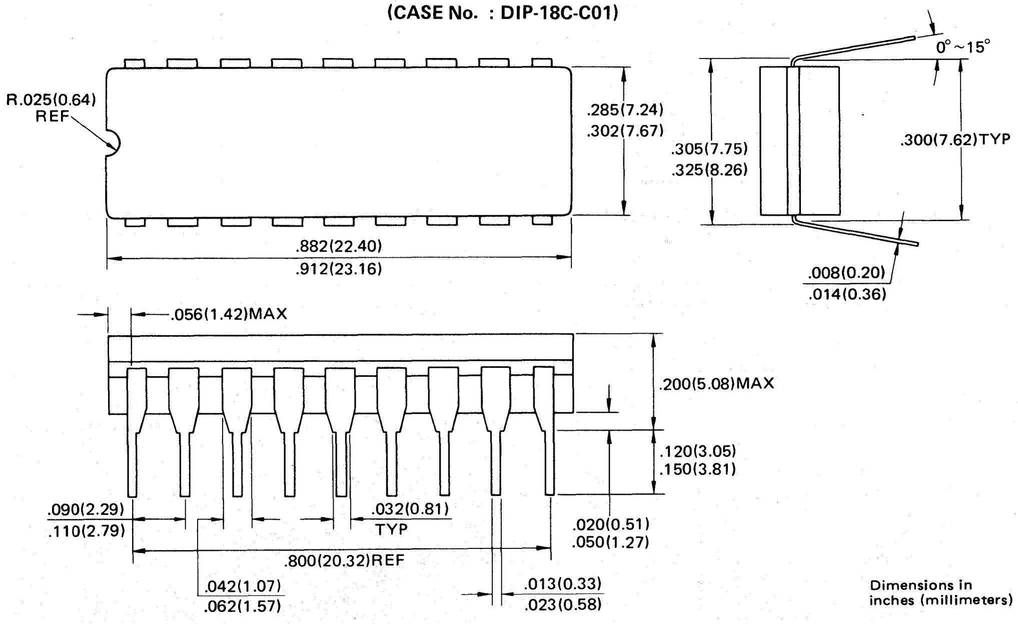
CERAMIC DIP
(CERDIP)



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: -CZ)

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



Dimensions in
inches (millimeters)

Advanced Products

FUJITSU

MBL8286 MBL8287 Bipolar Octal Bus Transceiver

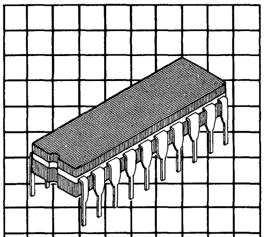
November 1986
Edition 4.0

Description

The MBL8286 and MBL8287 are 8-bit bipolar transceivers with 3-state outputs. The MBL8287 inverts the input data at its outputs while the MBL8286 does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met.

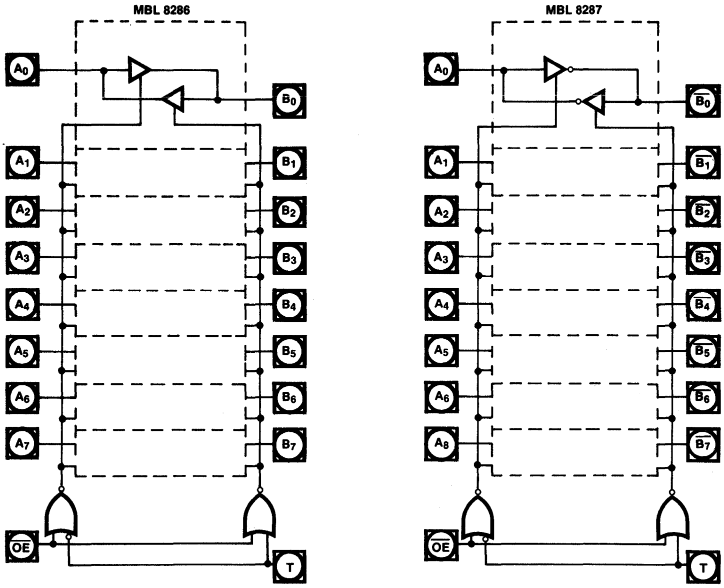
Features

- **Data Bus Buffer Driver for MBL8086, MBL8088, BML8089, MCS-80*, MCS-85*, and MCS-48* Families**
- **High Output Drive Capability for Driving System Data Bus**
- **Fully Parallel 8-Bit Transceivers**
- **3-State Outputs**
- **20-Pin DIP**
- **No Output Low Noise when Entering or Leaving High Impedance State**

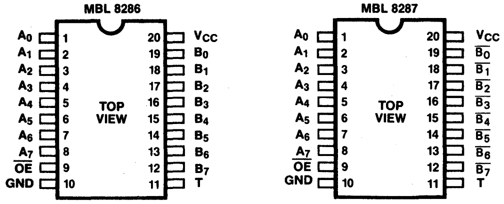


Ceramic Package DIP-20C-C01

Logic Diagrams



Pin Configurations



Pin Description

Symbol	Type	Name and Function
T	I	**Transmit:** T is an input control signal used to control the direction of the transceivers. When HIGH, it configures the transceiver's B_0-B_7 as outputs with A_0-A_7 as inputs. T LOW configures A_0-A_7 as the outputs and B_0-B_7 as the inputs.
$\overline{OE}$	O	**Output Enable:** $\overline{OE}$ is an input control signal used to enable the appropriate output driver (as selected by T) onto its respective bus. This signal is active LOW.
A_0-A_7	I/O	**Local Bus Data Pins:** These pins serve to either send data to or accept data from the processor's local bus, depending upon the state of the T pin.
B_0-B_7 (MBL8286) $\overline{B}_0$-$\overline{B}_7$ (MBL8287)	I/O	**System Bus Data Pins:** These pins serve to either send data to or accept data from the system bus, depending upon the state of the T pin.

Functional Description

The MBL8286 and MBL 8287 are 8-bit transsceivers with high impedance outputs. With T active HIGH and $\overline{OE}$ active LOW, data at the A_0-A_7 pins are sent to the B_0-B_7 pins. With T inactive low and $\overline{OE}$ active LOW, data at the B_0-B_7 pins is sent to the A_0-A_7 pins. No output low glitching will occur when the transceivers are entering or leaving the high impedance state.

Absolute Maximum Ratings

Parameter	Rating	Unit
Temperature Under Bias	0° to 70°	°C
Storage Temperature	-65° to +150°	°C
Supply Voltage	-0.5 to +7.0	V
All Output Voltages (3-State Output)	+5.5	V
All Input Voltages	-0.5 to +7.0	V
Power Dissipation	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{CC} = +5V ±10%,
T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_C	Input Clamp Voltage		-1	V	I_C = -5mA
I_{CC}	Power Supply Current—MBL8287 —MBL8286		130 160	mA mA	
I_F	Forward Input Current		-0.2	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	V_R = 5.25V
V_{OL}	Output Low Voltage—B Outputs —A Outputs		0.45 0.45	V V	I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage—B Outputs —A Outputs	2.4 2.4		V V	I_{OH} = -5 mA I_{OH} = -1 mA
I_{OFF} I_{OFF}	Output Off Current Output Off Current		I_F I_R		V_{OFF} = 0.45V V_{OFF} = 5.25V
V_{IL}	Input Low Voltage—A Side —B Side		0.8 0.9	V V	V_{CC} = 5.0V, See Note 1 V_{CC} = 5.0V, See Note 1
V_{IH}	Input High Voltage	2.0		V	V_{CC} = 5.0V, See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

Note: 1. B Outputs—I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF;
A Outputs—I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 100 pF.

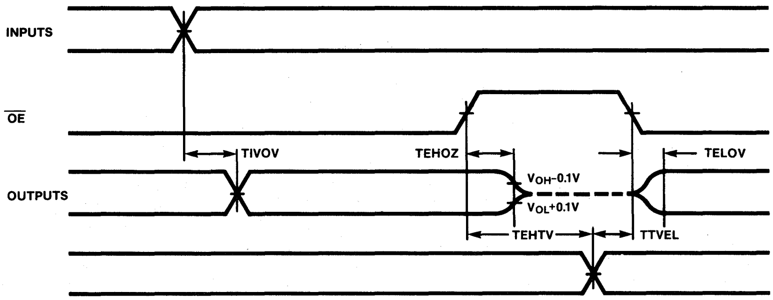
AC Characteristics

(V_{CC} = +5V ±10%,
T_A = 0°C to 70°C)
Loading:
1. B Outputs—I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF;
A Outputs—I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 100 pF.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TIVOV	Input to Output Delay Inverting —MBL8287 Non-Inverting —MBL8286	 5 5	 22 30	 ns ns	(See Note 1)
TEHTV	Transmit/Receive Hold Time	5		ns	
TTVEL	Transmit/Receive Setup	10		ns	
TEHOZ	Output Disable Time	5	18	ns	
TELOV	Output Enable Time	10	30	ns	
TILIH, TOLOH	Input/Output Rise Time		20	ns	From 0.8V to 2.0V
TIHIL, TOHOL	Input/Output FallTime		12	ns	From 2.0V to 8.0V

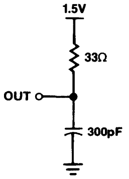
Note: 1. See the following waveforms and test load circuits.

Waveforms

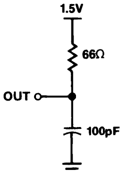


Note: All timing measurements are made at 1.5V unless otherwise noted.

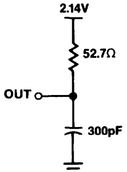
Test Load Circuits



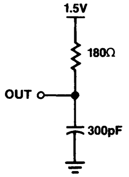
3-STATE TO V_{OL}
B OUTPUT



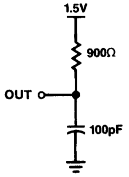
3-STATE TO V_{OL}
A OUTPUT



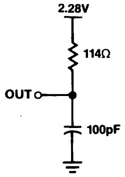
SWITCHING
B OUTPUT



3-STATE TO V_{OH}
B OUTPUT

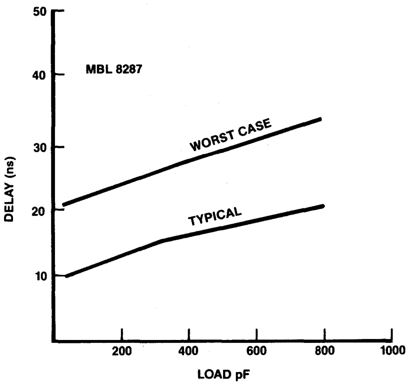


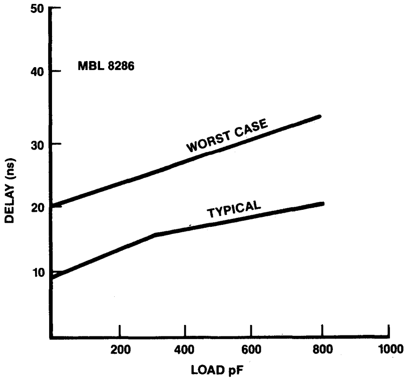
3-STATE TO V_{OH}
A OUTPUT



SWITCHING
A OUTPUT

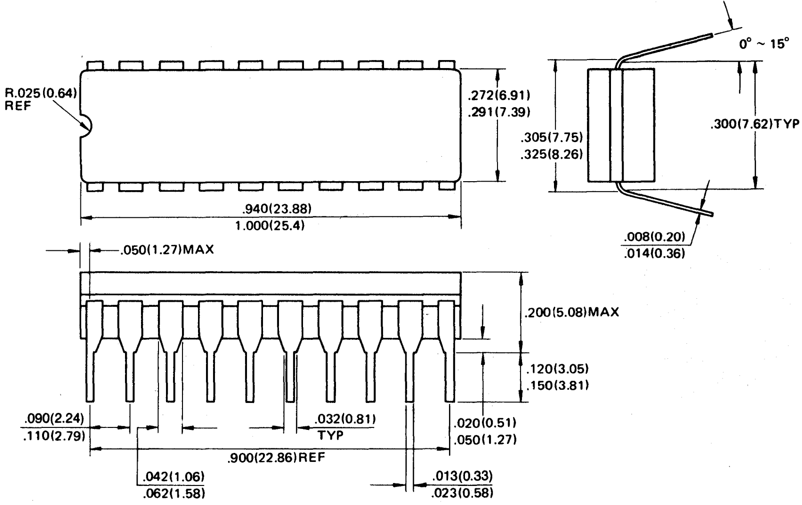
Output Delay Versus Capacitance





Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Ceramic (CERDIP) Dual In-Line Package DIP-20C-C01



FUJITSU

BUS CONTROLLER FOR MBL 8086/MBL 8088 /MBL 8089 PROCESSORS

MBL 8288

January 1985
Edition 3.0

BUS CONTROLLER
FOR MBL 8086/MBL 8088/MBL 8089 PROCESSORS

The Fujitsu MBL 8288 Bus Controller is a 20-pin bipolar component for use with medium-to-large MBL 8086/MBL 8088 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

- **Bipolar Drive Capability**
- **Provides Advanced Commands**
- **Provides Wide Flexibility in System Configurations**
- **3-State Command Output Drivers**
- **Configurable for Use with an I/O Bus**
- **Facilitates Interface to One or Two Multi-Master Busses**
- **10 MHz Clock Rate**
- **Standard 20-pin Cerdip (Suffix-CZ)**

Fig. 1 – BLOCK DIAGRAM

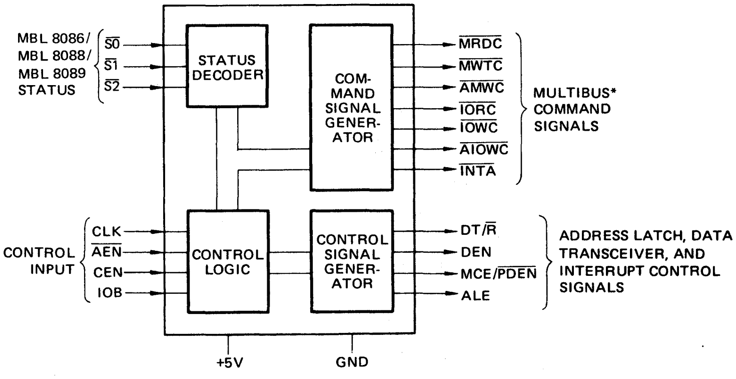
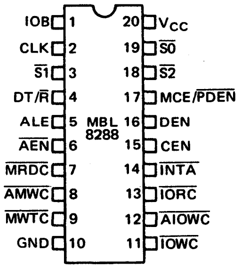


Fig. 2 – PIN ASSIGNMENT



*Trade Mark of Intel Corporation, USA.

TABLE 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
V_{CC}		**Power:** +5V supply
GND		**Ground**
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	I	**Status Input Pins:** These pins are the status input pins from the MBL 8086, MBL 8088 or MBL 8089 processors. The MBL 8288 decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Command and Control Logic.)
CLK	I	**Clock:** This is a clock signal from the MBL 8284 clock generator and serves to establish when command and control signals are generated.
ALE	O	**Address Latch Enable:** This signal serves to strobe and address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
DEN	O	**Data Enable:** This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	O	**Data Transmit/Receive:** This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (Write to I/O or memory) and a LOW indicates Receive (Read).
$\overline{AEN}$	I	**Address Enable:** $\overline{AEN}$ enables command outputs of the MBL 8288 Bus Controller at least 85 ns after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the MBL 8288 is in the I/O Bus mode (IOB tied HIGH).
CEN	I	**Command Enable:** When this signal is LOW all MBL 8288 command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	I	**Input/Output Bus Mode:** When the IOB is strapped HIGH the MBL 8288 functions in the I/O Bus mode. When it is strapped LOW, the MBL 8288 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes).
$\overline{AIOWC}$	O	**Advanced I/O Write Command:** The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	O	**I/O Write Command:** This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
$\overline{IORC}$	O	**I/O Read Command:** This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	O	**Advanced Memory Write Command:** The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction, its timing is the same as a read command signal, $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	O	**Memory Write Command:** This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	O	**Memory Read Command:** This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
$\overline{INTA}$	O	**Interrupt Acknowledge:** This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	O	This is a dual function pin. **MCE (IOB is tied LOW):** Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. **$\overline{PDEN}$ (IOB is tied HIGH):** Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

FUNCTIONAL DESCRIPTION

COMMAND AND CONTROL LOGIC

The command logic decodes the three MBL 8086, MBL 8088 or MBL 8089 CPU status lines ($\overline{\mathrm{S0}}$, $\overline{\mathrm{S1}}$, $\overline{\mathrm{S2}}$) to determine what command is to be issued.
This chart shows the meaning of each status "word".

$\overline{\mathrm{S0}}$ $\overline{\mathrm{S1}}$ $\overline{\mathrm{S2}}$	Processor State	MBL 8288 Command
0 0 0	Interrupt Acknowledge	$\overline{\mathrm{INTA}}$
0 0 1	Read I/O Port	$\overline{\mathrm{IORC}}$
0 1 0	Write I/O Port	$\overline{\mathrm{IOWC}}$, $\overline{\mathrm{AIOWC}}$
0 1 1	Halt	None
1 0 0	Code Access	$\overline{\mathrm{MRDC}}$
1 0 1	Read Memory	$\overline{\mathrm{MRDC}}$
1 1 0	Write Memory	$\overline{\mathrm{MWTC}}$, $\overline{\mathrm{AMWC}}$
1 1 1	Passive	None

The command is issued in one of two ways dependent on the mode of the MBL 8288 Bus Controller.

I/O Bus Mode – The MBL 8288 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines ($\overline{\mathrm{IORC}}$, $\overline{\mathrm{IOWC}}$, $\overline{\mathrm{AIOWC}}$, $\overline{\mathrm{INTA}}$) are always enabled (i.e., not dependent on $\overline{\mathrm{AEN}}$). When an I/O command is initiated by the processor, the MBL 8288 immediately activates the command lines using $\overline{\mathrm{PDEN}}$ and DT/$\overline{\mathrm{R}}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one MBL 8288 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{\mathrm{AEN}}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode – The MBL 8288 is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 85 ns after the $\overline{\mathrm{AEN}}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{\mathrm{AEN}}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

COMMAND OUTPUTS

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

$\overline{\mathrm{MRDC}}$	–	Memory Read Command
$\overline{\mathrm{MWTC}}$	–	Memory Write Command
$\overline{\mathrm{IORC}}$	–	I/O Read Command
$\overline{\mathrm{IOWC}}$	–	I/O Write Command
$\overline{\mathrm{AMWC}}$	–	Advanced Memory Write Command
$\overline{\mathrm{AIOWC}}$	–	Advanced I/O Write Command
$\overline{\mathrm{INTA}}$	–	Interrupt Acknowledge

$\overline{\mathrm{INTA}}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

CONTROL OUTPUTS

The control outputs of the MBL 8288 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{\mathrm{R}}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{\mathrm{PDEN}}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{\mathrm{R}}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{\mathrm{PDEN}}$ pin changes function with the two modes of the MBL 8288. When the MBL 8288 is in the IOB mode (IOB HIGH) the $\overline{\mathrm{PDEN}}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

INTERRUPT ACKNOWLEDGE AND MCE

The MCE signal is used during an interrupt acknowledge cycle if the MBL 8288 is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

ADDRESS LATCH ENABLE AND HALT

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{\mathrm{S0}}$, $\overline{\mathrm{S1}}$, $\overline{\mathrm{S2}}$) into a latch for halt state decoding.

COMMAND ENABLE
The Command Enable (CEN) input acts as a command qualifier for the MBL 8288. If the CEN pin is high the MBL 8288 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
All Output and Supply Voltages	-0.5V to +7.0V
All Input Voltages	-0.5V to +5.5V
Power Dissipation	1.5 W

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage		-1	V	I_C = -5 mA
I_{CC}	Power Supply Current		230	mA	
I_F	Forward Input Current		-0.7	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage: Command Outputs Control Outputs		 0.5 0.5	 V V	 I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage: Command Outputs Control Outputs	 2.4 2.4		 V V	 I_{OH} = -5 mA I_{OH} = -1 mA
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
I_{OFF}	Output Off Current		100	μA	V_{OFF} = 0.4 to 5.25V

A.C. CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to 70°C)

TIMING REQUIREMENTS

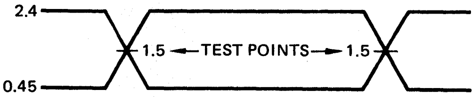
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
TCLCL	CLK Cycle Period	100		ns	
TCLCH	CLK Low Time	50		ns	
TCHCL	CLK High Time	30		ns	
TSVCH	Status Active Setup Time	35		ns	
TCHSV	Status Active Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	35		ns	
TCLSH	Status Inactive Hold Time	10		ns	

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

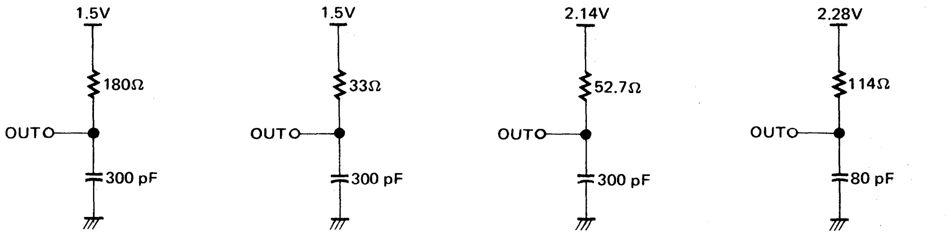
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
TCVNV	Control Active Delay	5	45	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$ } I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF Other { I_{OL} = 16 mA, I_{OH} = -1 mA, C_L = 80 pF
TCVNX	Control Inactive Delay	10	45	ns	
TCLLH, TCLMCH	ALE MCE Active Delay (from CLK)		20	ns	
TSVLH, TSVMCH	ALE MCE Active Delay (from Status)		20	ns	
TCHLL	ALE Inactive Delay	4	15	ns	
TCLML	Command Active Delay	10	35	ns	
TCLMH	Command Inactive Delay	10	35	ns	
TCHDTL	Direction Control Active Delay		50	ns	
TCHDTH	Direction Control Inactive Delay		30	ns	
TAELCH	Command Enable Time		40	ns	
TAEHCZ	Command Disable Time		40	ns	
TAELCV	Enable Delay Time	85	200	ns	
TAEVNV	AEN to DEN		20	ns	
TCEVNV	CEN to DEN, PDEN		25	ns	
TCELRH	CEN to Command		TCLML	ns	
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12	ns	From 2.0V to 0.8V

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0". Input rise and fall times are 5±2ns, (measured between 0.8V and 2.0V.)

TEST LOAD CIRCUITS – 3-STATE COMMAND OUTPUT TEST LOAD



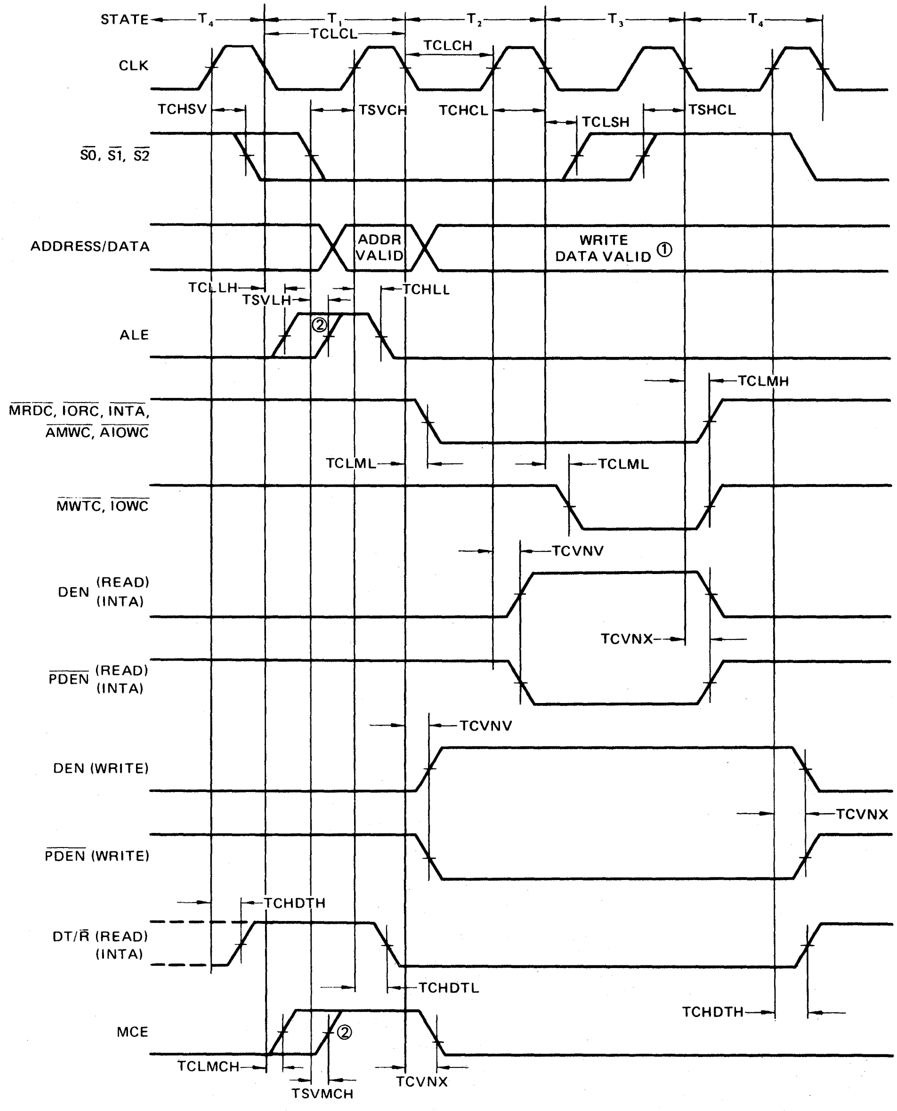
3-STATE TO HIGH

3-STATE TO LOW

COMMAND OUTPUT TEST LOAD

CONTROL OUTPUT TEST LOAD

WAVEFORMS

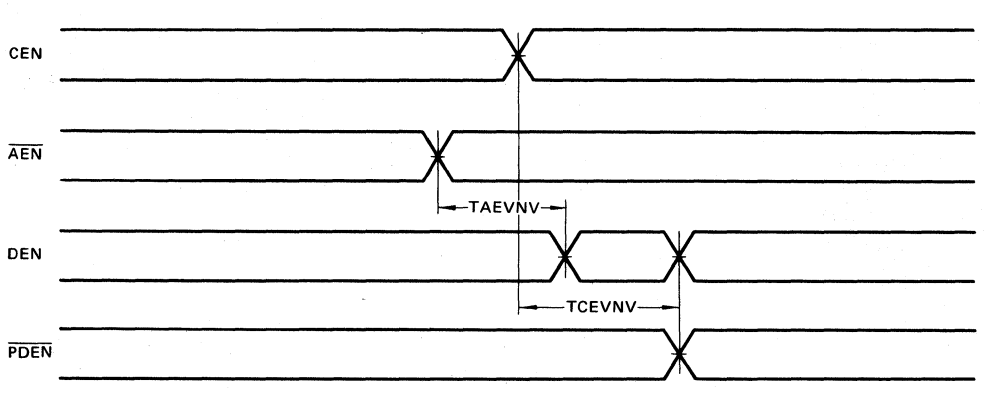


NOTES:

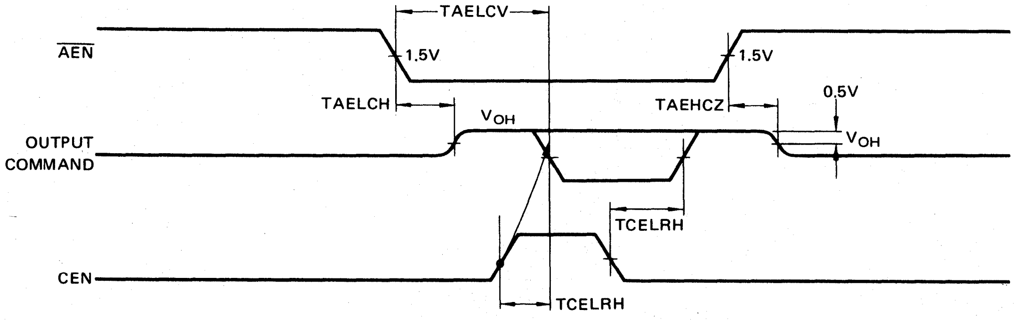
1. ADDRESS/DATA Bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3. All timing measurements are made at 1.5V unless specified otherwise.

WAVEFORMS (Continued)

DEN, $\overline{\text{PDEN}}$ QUALIFICATION TIMING

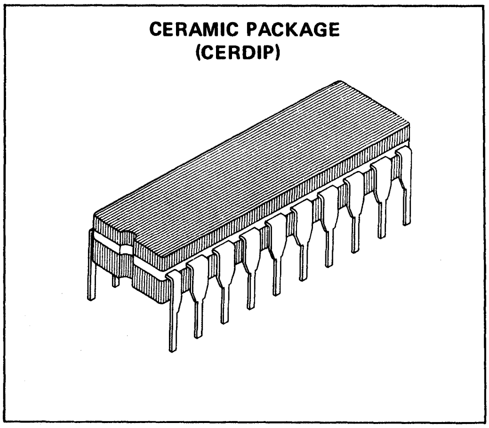


ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)



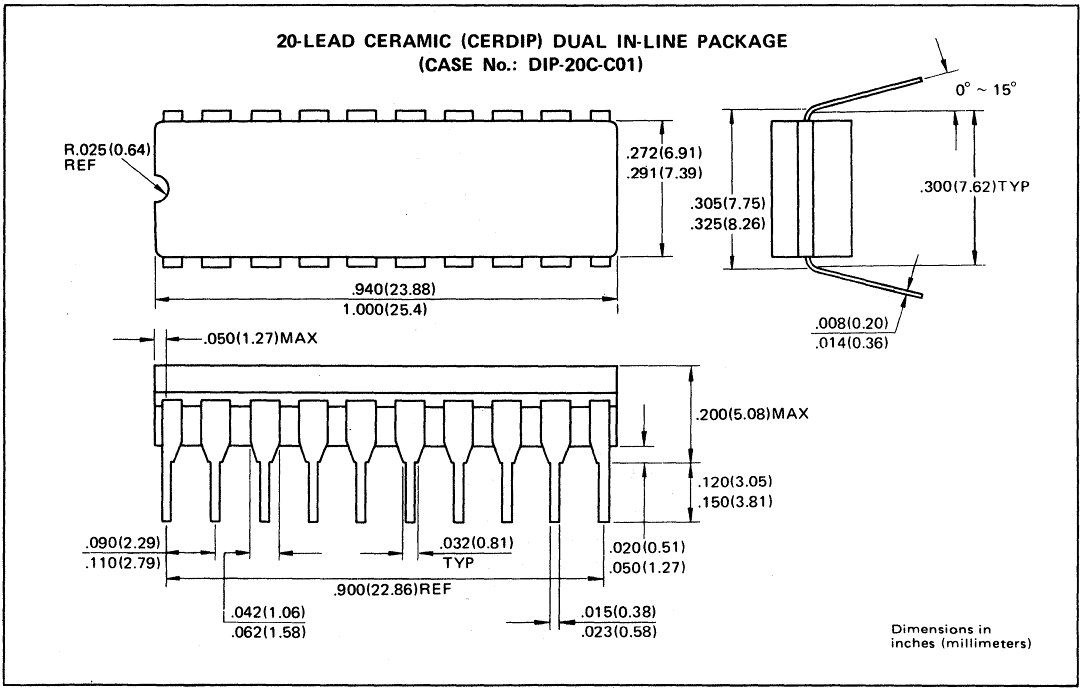
NOTE: CEN must be low or valid prior to T2 to prevent the command from being generated.

PACKAGE ILLUSTRATION



PACKAGE DIMENSIONS

(Suffix: -CZ)



FUJITSU

BIPOLAR BUS ARBITER

MBL 8289
MBL 8289-1

April 1986
Edition 4.0

BIPOLAR BUS ARBITER FOR MBL 8086/8088/80186/80188/8089

The Fujitsu MBL 8289 Bus Arbiter is a 20-pin, 5-volt-only bipolar component for use with medium to large MBL 8086/8088/80186/80188 multi-master/multiprocessing systems. The MBL 8289 provides system bus arbitration for systems with multiple bus masters, such as an MBL 8086/8088/80186/80188 CPU with MBL 8089 IOP in its REMOTE mode, while providing bipolar buffering and drive capability.

- **Provides Multi-Master System Bus Protocol**
- **Synchronizes MBL 8086/8088/80186/80188/8089 Processors with Multi-Master Bus:**
  –5MHz, 8MHz (MBL 8086/8088/8089), and 6MHz (MBL 80186/80188) with MBL 8289
  –10MHz (MBL 8086/8088) and 8MHz (MBL 80186/80188) with MBL 8289-1
- **Provides Simple Interface with MBL 8288 Bus Controllers**
- **Four Operating Modes for Flexible System Configuration**
- **Compatible with Intel Bus Standard MULTI-BUS***
- **Provides System Bus Arbitration for MBL 8089 IOP in Remote Mode**
- **Two Package Options:**
  – 20-Pin Cerdip (Suffix: -CZ)
  – 20-Pin Plastic DIP (Suffix: -P)

Fig. 1 – BLOCK DIAGRAM

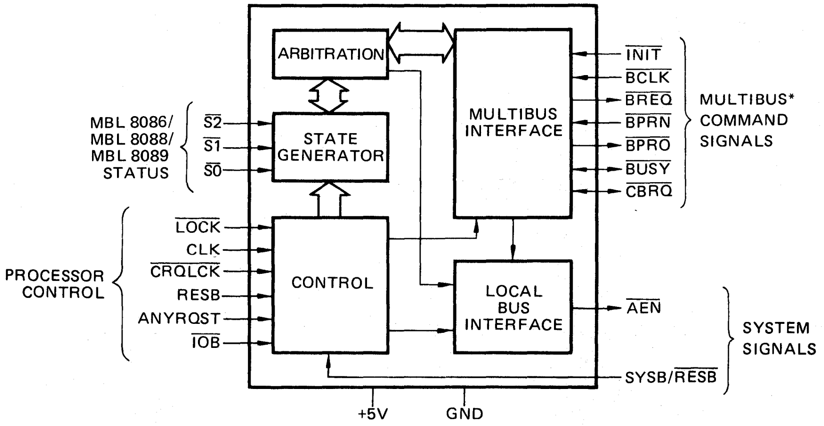


Fig. 2 – PIN CONFIGURATION

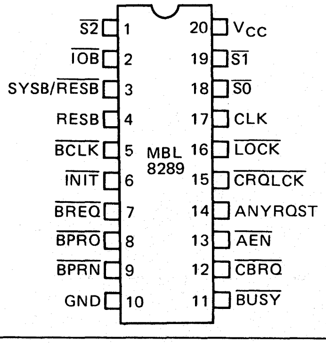
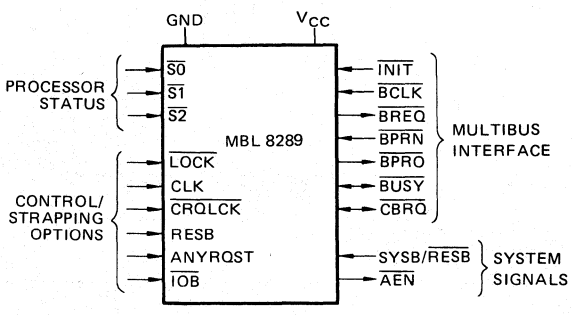


Fig. 3 – FUNCTIONAL PINOUT



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PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
V_{CC}		**Power:** +5V supply ±10%.
GND		**Ground.**
$\overline{\mathrm{S0}}, \overline{\mathrm{S1}}, \overline{\mathrm{S2}}$	I	**Status Input Pins:** The status input pins from an MBL 8086, MBL 8088, MBL 80186, MBL 80188 or MBL 8089 processor. The MBL 8289 decodes these pins to initiate bus request and surrender actions. (See Table 2.)
CLK	I	**Clock:** From the MBL 8284A clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{\mathrm{LOCK}}$	I	**Lock:** A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter,regardless of its priority.
$\overline{\mathrm{CRQLCK}}$	I	**Common Request Lock:** An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{\mathrm{CBRQ}}$ input pin.
RESB	I	**Resident Bus:** A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{\mathrm{RESB}}$ input pin. Strapped low, the SYSB/$\overline{\mathrm{RESB}}$ input is ignored.
ANYRQST	I	**Any Request:** A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table 2. If ANYRQST is strapped high and $\overline{\mathrm{CBRQ}}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{\mathrm{CBRQ}}$ low and ANYRQST high forces the MBL 8289 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs BREQ is driven false (high).
$\overline{\mathrm{IOB}}$	I	**IO Bus:** A strapping option which configures the MBL 8289 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{\mathrm{S2}}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{\mathrm{AEN}}$	O	**Address Enable:** The output of the MBL 8289 Arbiter to the processor's address latches to the MBL 8288 Bus Controller and 8284A Clock Generator. $\overline{\mathrm{AEN}}$ serves to instruct the Bus Controller and address latches when to tri-state their output drivers.
SYSB/$\overline{\mathrm{RESB}}$	I	**System Bus/Resident Bus:** An input signal when the arbiter is configured in the S.R. Mode (RESB is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from ϕ1 of T4 to ϕ1 of T2 of the processor cycle. During the period from ϕ1 of T2 to ϕ1 of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the S.R. Mode when the state of the SYSB/$\overline{\mathrm{RESB}}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{\mathrm{CBRQ}}$	I/O	**Common Bus Request:** An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{\mathrm{CBRQ}}$ pins (open-collector output) of all the MBL 8289 Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{\mathrm{CBRQ}}$ line low. Any other arbiter connected to the $\overline{\mathrm{CBRQ}}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{\mathrm{BREQ}}$ signal and surrenders the bus whenever the proper surredner conditions exist. Strapping $\overline{\mathrm{CBRQ}}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{\mathrm{INIT}}$	I	**Initialize:** An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
$\overline{\mathrm{BCLK}}$	I	**Bus Clock:** The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.

TABLE 1 – PIN DESCRIPTION (Continued)

Symbol	Type	Name and Function
$\overline{\text{BREQ}}$	O	**Bus Request:** An active low output signal in the parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{\text{BPRN}}$	I	**Bus Priority In:** The active low signal returned to the arbiter to instruct if that it may acquire the multi-master system bus on the next falling edge of BCLK. $\overline{\text{BPRN}}$ indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{\text{BPRN}}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{\text{BPRO}}$	O	**Bus Priority Out:** An active low output signal used in the serial priority resolving scheme where $\overline{\text{BPRO}}$ is daisy-chained to $\overline{\text{BPRN}}$ of the next lower priority arbiter.
$\overline{\text{BUSY}}$	I/O	**Busy:** An active low open collector multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{\text{BPRN}}$) seizes the bus and pulls $\overline{\text{BUSY}}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{\text{BUSY}}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

FUNCTIONAL DESCRIPTION

The MBL 8289 Bus Arbiter operates in conjunction with the MBL 8288 Bus Controller to interface MBL 8086/8088/80186/188 processors to a multi-master system bus (both the MBL 8086 and MBL 8088 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (MBL 8288), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the MBL 8288, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

ARBITRATION BETWEEN BUS MASTERS

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multi-master system bus is surrendered or requested under different sets of conditions.

PRIORITY RESOLVING TECHNIQUES

Since there can be many bus masters on a multi-master system bus, some means of resolving priority between bus masters simultaneously requesting the bus must be provided. The MBL 8289 Bus Arbiter provides several resolving techniques. All the techniques are based on a priority concept that at a given time one bus master will have priority above all the rest. There are provisions for using parallel priority resolving techniques, serial priority resolving techniques, and rotating priority techniques.

PARALLEL PRIORITY RESOLVING

The parallel priority resolving technique uses a separate bus request line ($\overline{\text{BREQ}}$) for each arbiter on the multi-master system bus, see Figure 4. Each $\overline{\text{BREQ}}$ line enters into a priority encoder which generates the binary address of the highest priority $\overline{\text{BREQ}}$ line which is active. The binary address is decoded by a decoder to select the corresponding $\overline{\text{BPRN}}$ (Bus Priority In) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority ($\overline{\text{BPRN}}$ true) then allows its associated bus master onto the multi-master system bus as soon as it becomes available (i.e., the bus is no longer busy). When one bus arbiter gains priority over another arbiter it cannot immediately seize the bus, it must wait until the present bus transaction is complete. Upon completing its transaction the present bus occupant recognizes that it no longer has priority and surrenders the bus by releasing $\overline{\text{BUSY}}$. $\overline{\text{BUSY}}$ is an active low "OR" tied signal line which goes to every bus arbiter on the system bus. When $\overline{\text{BUSY}}$ goes inactive (high), the arbiter which presently has bus priority ($\overline{\text{BPRN}}$ true) then seizes the bus and pulls $\overline{\text{BUSY}}$ low to keep other arbiters off of the bus. See waveform timing diagram, Figure 5. Note that all multi-master system bus transactions are synchronized to the bus clock ($\overline{\text{BCLK}}$). This allows the parallel priority resolving circuitry or any other priority resolving scheme employed to settle.

Fig. 4 – PARALLEL PRIORITY RESOLVING TECHNIQUE

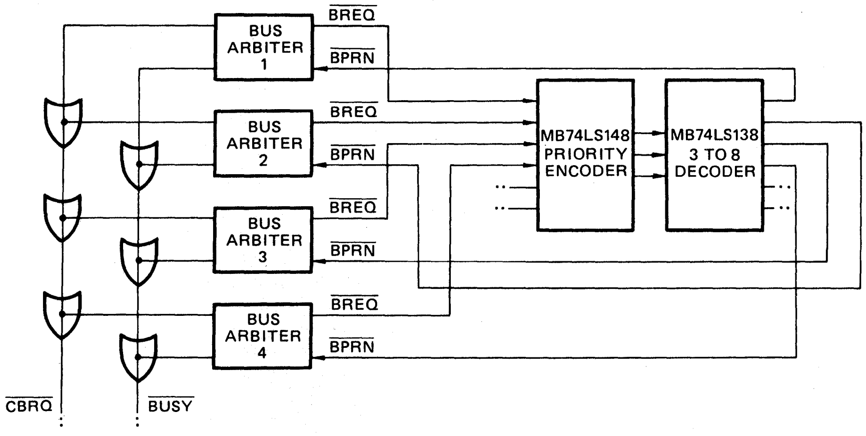
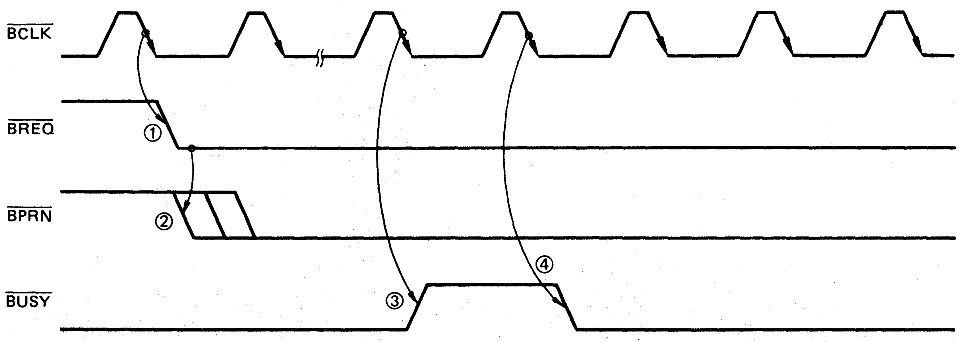


Fig. 5 – HIGHER PRIORITY ARBITER OBTAINING THE BUS FROM A LOWER PRIORITY ARBITER

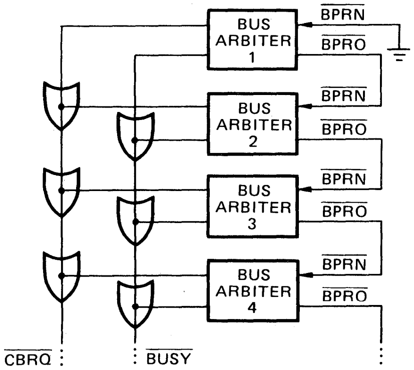


① HIGHER PRIORITY BUS ARBITER REQUESTS THE MULTI-MASTER SYSTEM BUS.
② ATTAINS PRIORITY.
③ LOWER PRIORITY BUS ARBITER RELEASES BUSY.
④ HIGHER PRIORITY BUS ARBITER THEN ACQUIRES THE BUS AND PULLS BUSY DOWN.

SERIAL PRIORITY RESOLVING

The serial priority resolving technique eliminates the need for the priority encoder-decoder arrangement by daisy-chaining the bus arbiters together, connecting the higher priority bus arbiter's $\overline{\text{BPRO}}$ (Bus Priority Out) output to the $\overline{\text{BPRN}}$ of the next lower priority. See Figure 6.

Fig. 6 – SERIAL PRIORITY RESOLVING



THE NUMBER OF ARBITERS THAT MAY BE DAISY-CHAINED TOGETHER IN THE SERIAL PRIORITY RESOLVING SCHEME IS A FUNCTION OF BCLK AND THE PROPAGATION DELAY FROM ARBITER TO ARBITER. NORMALLY, AT 10 MHz ONLY 3 ARBITERS MAY BE DAISY-CHAINED.

ROTATING PRIORITY RESOLVING

The rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically reassigned. The priority encoder is replaced by a more complex circuit which rotates priority between requesting arbiters thus allowing each arbiter an equal chance to use the multi-master system bus, over time.

WHICH PRIORITY RESOLVING TECHNIQUE TO USE

There are advantages and disadvantages for each of the techniques described above. The rotating priority resolving technique requires substantial external logic to implement while the serial technique uses no external logic but can accommodate only a limited number of bus arbiters before the daisy-chain propagation delay exceeds the multi-master's system bus clock ($\overline{\text{BCLK}}$). The parallel priority resolving technique is in general a good compromise between the other two techniques. It allows for many arbiters to be present on the bus while not requiring too much logic to implement.

MBL 8289 MODES OF OPERATION

There are two types of processors in the MBL 8086/80186 family. An Input/Output processor (the MBL 8089 IOP) and the MBL 8086/8088/80186/80188 CPUs. Consequently, there are two basic operating modes in the MBL 8289 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{\text{IOB}}$ strapping option configures the MBL 8289 Bus Arbiter into the $\overline{\text{IOB}}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only (see Figure 7). With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{\text{IOB}}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus. Figure 8 shows a possible I/O Processor system configuration.

The MBL 8086/8088/80186/80188 processors can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration as shown in Figure 9. In such a system configuration the processor would have access to memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{\text{RESB}}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{\text{RESB}}$ also enables or disables commands from one of the bus controllers.

A summary of the modes that the MBL 8289 has, along with its response to its status lines inputs, is summarized in Table 2.

*In some system configurations it is possible for a non-I/O Processor to have access to more than one Multi-Master System Bus, see Intel's 8289 Application Note.

TABLE 2 – SUMMARY OF MBL 8289 MODES, REQUESTING AND RELINQUISHING THE MULTI-MASTER SYSTEM BUS

Command	Status Lines From MBL 8086 / 8088 / 8089 / 80186 / 80188			IOB Mode Only	RESB (Mode) Only $\overline{\text{IOB}}$ = High RESB = High		IOB Mode RESB Mode $\overline{\text{IOB}}$ = Low RESB = High		Single Bus Mode $\overline{\text{IOB}}$ = High RESB = Low
	$\overline{\text{S2}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$	$\overline{\text{IOB}}$ = Low	SYSB/$\overline{\text{RESB}}$ = High	SYSB/$\overline{\text{RESB}}$ = Low	SYSB/$\overline{\text{RESB}}$ = High	SYSB/$\overline{\text{RESB}}$ = Low	
I/O COMMANDS	0	0	0	x		x	x	x	
	0	0	1	x		x	x	x	
	0	1	0	x		x	x	x	
HALT	0	1	1	x	x	x	x	x	x
MEM COMMANDS	1	0	0			x		x	
	1	0	1			x		x	
	1	1	0			x		x	
IDLE	1	1	1	x	x	x	x	x	x

NOTES:
1. x = Multi-Master System Bus is allowed to be Surrendered.
2. = Multi-Master System Bus is Requested.

Mode	Pin Strapping	Multi-Master System Bus	
		Requested**	Surrendered*
Single Bus Multi-Master Mode	$\overline{\text{IOB}}$ = High RESB = Low	Whenever the processor's status lines go active	HLT + TI · CBRQ + HPBRQ†
RESB Mode Only	$\overline{\text{IOB}}$ = High RESB = High	SYSB/$\overline{\text{RESB}}$ = High · ACTIVE STATUS	(SYSB/$\overline{\text{RESB}}$ = Low + TI) · CBRQ + HLT + HPBRQ
IOB Mode Only	$\overline{\text{IOB}}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) · CBRQ + HLT + HPBRQ
IOB Mode · RESB Mode	$\overline{\text{IOB}}$ = Low RESB = High	(Memory Command) · (SYSB/$\overline{\text{RESB}}$ = High)	((I/O Status Commands) + (SYSB/$\overline{\text{RESB}}$ = Low))· CBRQ + HPBRQ† + HLT

NOTES:

* $\overline{\text{LOCK}}$ prevents surrender of Bus to any other arbiter, $\overline{\text{CRQLCK}}$ prevents surrender of Bus to any lower priority arbiter.

** Except for HALT and Passive or IDLE Status.

† HPBRQ, Higher priority Bus request or $\overline{\text{BPRN}}$ = 1.

1. $\overline{\text{IOB}}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and · as "AND."
4. TI = Processor Idle Status $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ = 111
5. HLT = Processor Halt Status $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ = 011

Fig.7 — TYPICAL MEDIUM COMPLEXITY CPU SYSTEM

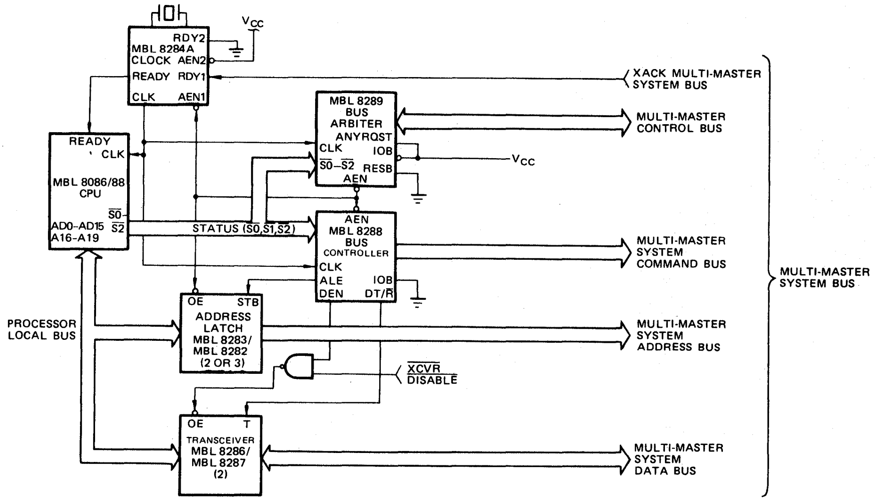


Fig.8 — TYPICAL MEDIUM COMPLEXITY IOB SYSTEM

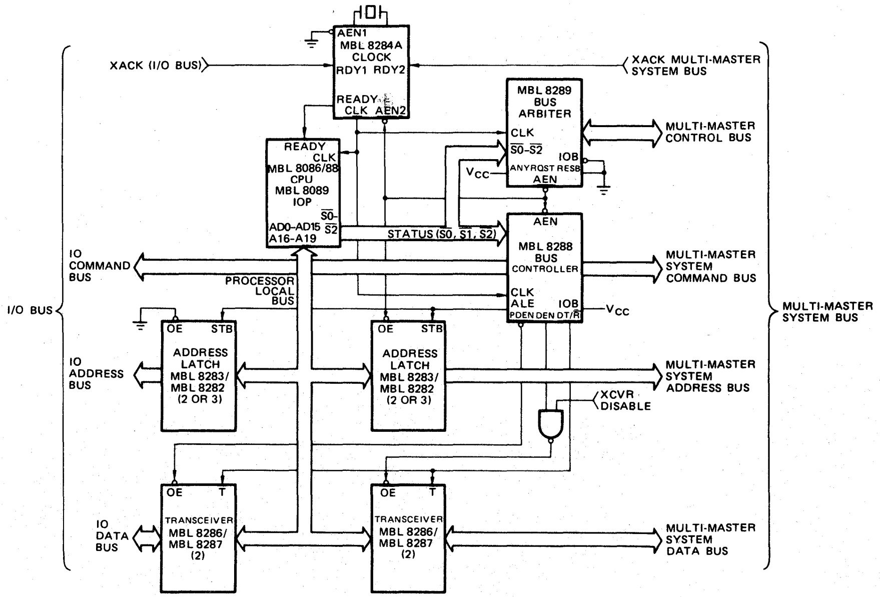
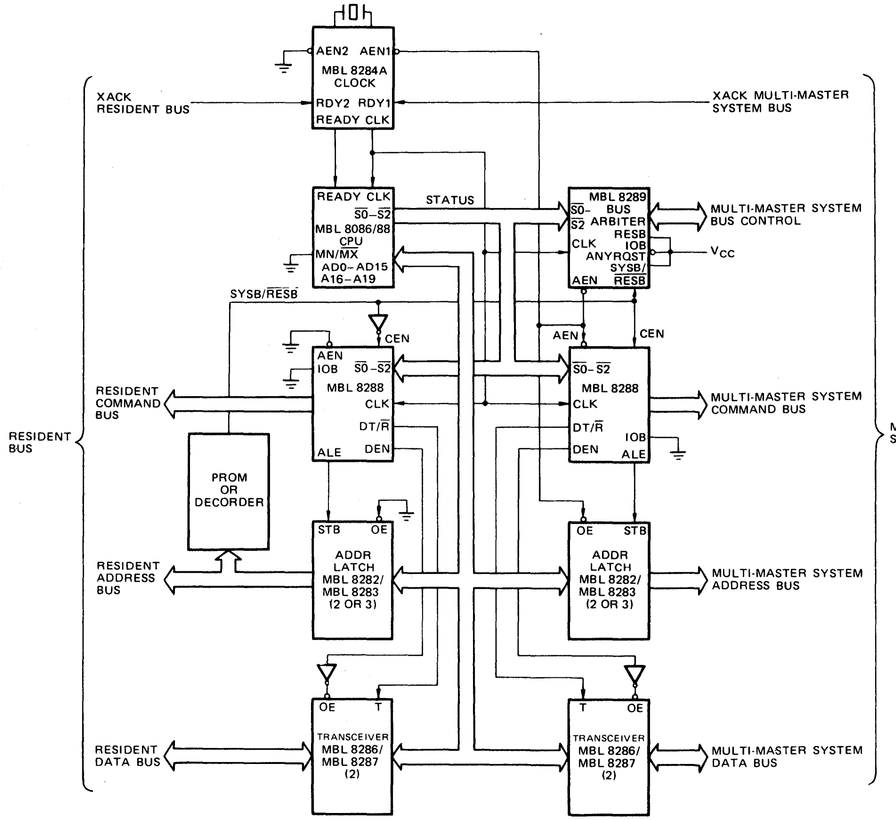


Fig. 9 — MBL 8289 BUS ARBITER SHOWN IN SYSTEM-RESIDENT BUS CONFIGURATION



* BY ADDING ANOTHER MBL 8289 ARBITER AND CONNECTING ITS $\overline{\text{AEN}}$ TO THE MBL 8288 WHOSE $\overline{\text{AEN}}$ IS PRESENTLY GROUNDED, THE PROCESSOR COULD HAVE ACCESS TO TWO MULTI-MASTER BUSES.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
All Output and Supply Voltages	-0.5V to +7.0V
All Input Voltages	-0.5V to +5.5V
Power Dissipation	1.0W

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Test Condition
V_C	Input Clamp Voltage			-1.0	V	V_{CC} = 4.50V, I_C = –5mA
I_F	Input Forward Current			–0.5	mA	V_{CC} = 5.50V, V_F = 0.45V
I_R	Reverse Input Leakage Current			60	μA	V_{CC} = 5.50V, V_R = 5.50V
V_{OL}	Output Low Voltage	$\overline{\text{BUSY}}$, $\overline{\text{CBRQ}}$		0.45	V	I_{OL} = 20mA
		$\overline{\text{AEN}}$		0.45	V	I_{OL} = 16mA
		$\overline{\text{BPRO}}$, $\overline{\text{BREQ}}$		0.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage	$\overline{\text{BUSY}}$, $\overline{\text{CBRQ}}$	Open Collector			
		$\overline{\text{AEN}}$, $\overline{\text{BPRO}}$, $\overline{\text{BREQ}}$	2.4		V	I_{OH} = 400μA
I_{CC}	Power Supply Current			95	mA	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage		2.0		V	
Cin Status	Input Capacitance			25	pF	
Cin (Others)	Input Capacitance			12	pF	

A.C. CHARACTERISTICS (V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

TIMING REQUIREMENTS

Symbol	Parameter	MBL 8289 Min	MBL 8289-1 Min.	Max.	Unit	Test Condition
TCLCL	CLK Cycle Period	125	100		ns	
TCLCH	CLK Low Time	65	53		ns	
TCHCL	CLK High Time	35	26		ns	
TSVCH	Status Active Setup	65	55	TCLCL-10	ns	
TSHCL	Status Inactive Setup	50	45	TCLCL-10	ns	
THVCH	Status Active Hold	10	10		ns	
THVCL	Status Inactive Hold	10	10		ns	
TBYSBL	$\overline{\text{BUSY}}$ ↑↓ Setup to $\overline{\text{BCLK}}$ ↓	20	20		ns	
TCBSBL	$\overline{\text{CBRQ}}$ ↑↓ Setup to $\overline{\text{BCLK}}$ ↓	20	20		ns	
TBLBL	$\overline{\text{BCLK}}$ Cycle Time	100	100		ns	
TBHCL	$\overline{\text{BCLK}}$ High Time	30	30	0.65[TBLBL]	ns	
TCLLL1	$\overline{\text{LOCK}}$ Inactive Hold	10	10		ns	
TCLLL2	$\overline{\text{LOCK}}$ Active Setup	40	40		ns	
TPNBL	$\overline{\text{BPRN}}$ ↓↑ to $\overline{\text{BCLK}}$ Setup Time	15	15		ns	
TCLSR1	SYSB/$\overline{\text{RESB}}$ Setup	0	0		ns	
TCLSR2	SYSB/$\overline{\text{RESB}}$ Hold	20	20		ns	
TIVIH	Initialization Pulse Width	3 TBLBL + 3 TCLCL	3 TBLBL + 3 TCLCL		ns	

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

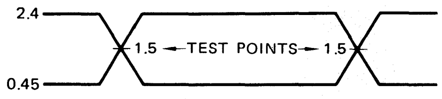
Symbol	Parameter	Min.	Max.	Unit	Test Condition
TBLBRL	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ Delay ↓↑		35	ns	
TBLPOH	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ ↓↑ (See Note 1)		40	ns	
TPNPO	$\overline{\text{BPRN}}$ ↓↑ to $\overline{\text{BPRO}}$ ↓↑ Delay (See Note 1)		25	ns	
TBLBYL	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Low		60	ns	
TBLBYH	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Float (See Note 2)		35	ns	
TCLAEH	CLK to $\overline{\text{AEN}}$ High		65	ns	
TBLAEL	$\overline{\text{BCLK}}$ to $\overline{\text{AEN}}$ Low		40	ns	
TBLCBL	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ Low		60	ns	
TBLCBH	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ Float (See Note 2)		35	ns	
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12	ns	From 2.0V to 0.8V

↓↑ Denotes that spec applies to both transition of the signal.

NOTES:

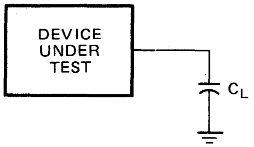
1. $\overline{\text{BCLK}}$ generates the first $\overline{\text{BPRO}}$ wherein subsequent $\overline{\text{BPRO}}$ changes lower in the chain are generated through $\overline{\text{BPRN}}$.
2. Measured at .5V above GND.

A.C. TESTING INPUT, OUTPUT WAVEFORM



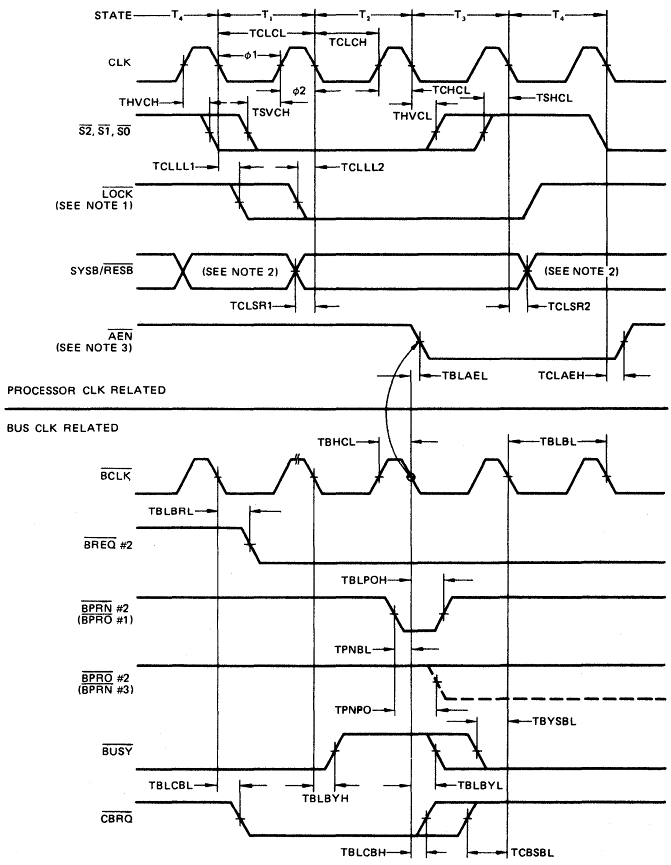
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". THE CLOCK IS DRIVEN AT 4.3V AND 0.25V. TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0". INPUT RISE AND FALL TIMES (MEASURED BETWEEN 0.8V AND 2.0V) ARE DRIVEN AT 5±2NS.

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L INCLUDES JIG CAPACITANCE

WAVEFORMS



NOTES:

1. $\overline{\text{LOCK}}$ ACTIVE CAN OCCUR DURING ANY STATE, AS LONG AS THE RELATIONSHIPS SHOWN ABOVE WITH RESPECT TO THE CLK ARE MAINTAINED. $\overline{\text{LOCK}}$ INACTIVE HAS NO CRITICAL TIME AND CAN BE ASYNCHRONOUS.
   – $\overline{\text{CRQLCK}}$ HAS NO CRITICAL TIMING AND IS CONSIDERED AN ASYNCHRONOUS INPUT SIGNAL.
2. GLITCHING OF SYSB/$\overline{\text{RESB}}$ PIN IS PERMITTED DURING THIS TIME. AFTER φ2 OF T1, AND BEFORE φ1 OF T4, SYSB/$\overline{\text{RESB}}$ SHOULD BE STABLE.
3. $\overline{\text{AEN}}$ LEADING EDGE IS RELATED TO $\overline{\text{BCLK}}$, TRAILING EDGE TO CLK. THE TRAILING EDGE OF AEN OCCURS AFTER BUS PRIORITY IS LOST.

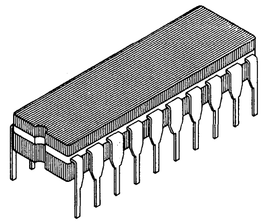
ADDITIONAL NOTES:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to $\overline{\text{BCLK}}$. The signals shown related to the $\overline{\text{BCLK}}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme as shown in Figure 6. Assume arbiter 1 has the bus and is holding busy low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{\text{BREQ\#2}}$. If $\overline{\text{BPRN\#2}}$ is high (as shown), arbiter #2 will pull low $\overline{\text{CBRQ}}$ line. $\overline{\text{CBRQ}}$ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{\text{CBRQ}}$]** Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its $\overline{\text{BPRO\#1}}$ (tied to $\overline{\text{BPRN\#2}}$) and releasing BUSY. Arbiter #2 now sees that it has priority from $\overline{\text{BPRN\#2}}$ being low and releases $\overline{\text{CBRQ}}$. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{\text{BPRO\#2}}$ [TPNPO].

**Note that even a higher priority arbiter which is acquiring the bus through $\overline{\text{BPRN}}$ will momentarily drop $\overline{\text{CBRQ}}$ until it has acquired the bus.

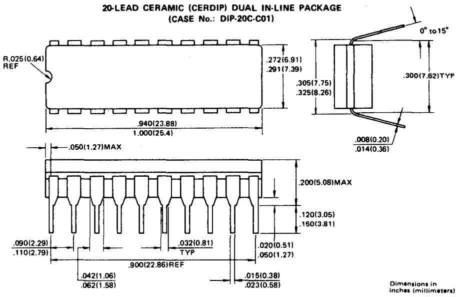
PACKAGE ILLUSTRATION AND DIMENSIONS

CERAMIC DIP (Suffix: CZ)



DIP-20C-C01

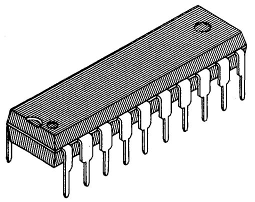
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



Dimensions in inches (millimeters)

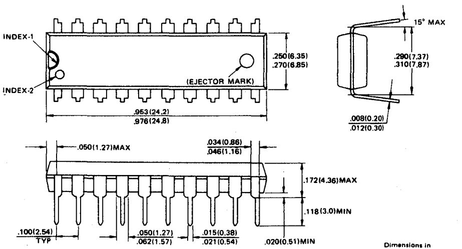
©1986 FUJITSU LIMITED D20001S-2C

PLASTIC DIP (Suffix: P)



DIP-20P-M01

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



Dimensions in inches (millimeters)

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Section 2

Microcomputers and Peripherals

8-Bit Microcomputers and Peripherals

4-Bit Microcomputers and Peripherals

October 1986
Edition 1.0

MBL8048N/E/H
MBL8035N/E/H
NMOS Single-Chip 8-Bit Microcomputer

Description

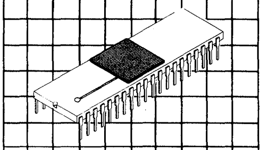
The Fujitsu MBL8048/MBL8035 is a totally self-contained 8-bit parallel one-chip microcomputer fabricated wtih an N-channel silicon gate MOS process.

The MBL8048 has a 1K x 8 ROM program memory, a 64 x 8 RAM data memory, 27 I/O ports, an 8-bit timer/counter and clock generator on-chip. A single power supply of +5V is used. The MBL8035 is identical to the MBL8048 except without program memory. It can be used with external memory for system prototyping and preproduction systems.

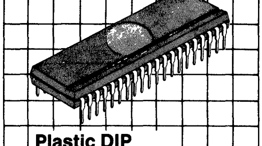
The design is optimized for low cost, high performance applications because the MBL8048/MBL8035 is fabricated on a single silicon chip and can be used for applications that require additional expansion of ROMs, RAMs, I/O port, etc.

This microcomputer permits external program operation and a single-step operation mode. Low power applications are possible by using the stand-by mode feature.

The MBL8048/MBL8035 is packaged in a standard 40-pin DIP package and operation is guaranteed from 0° C to 70° C.



Ceramic DIP
(DIP-40C-A01)

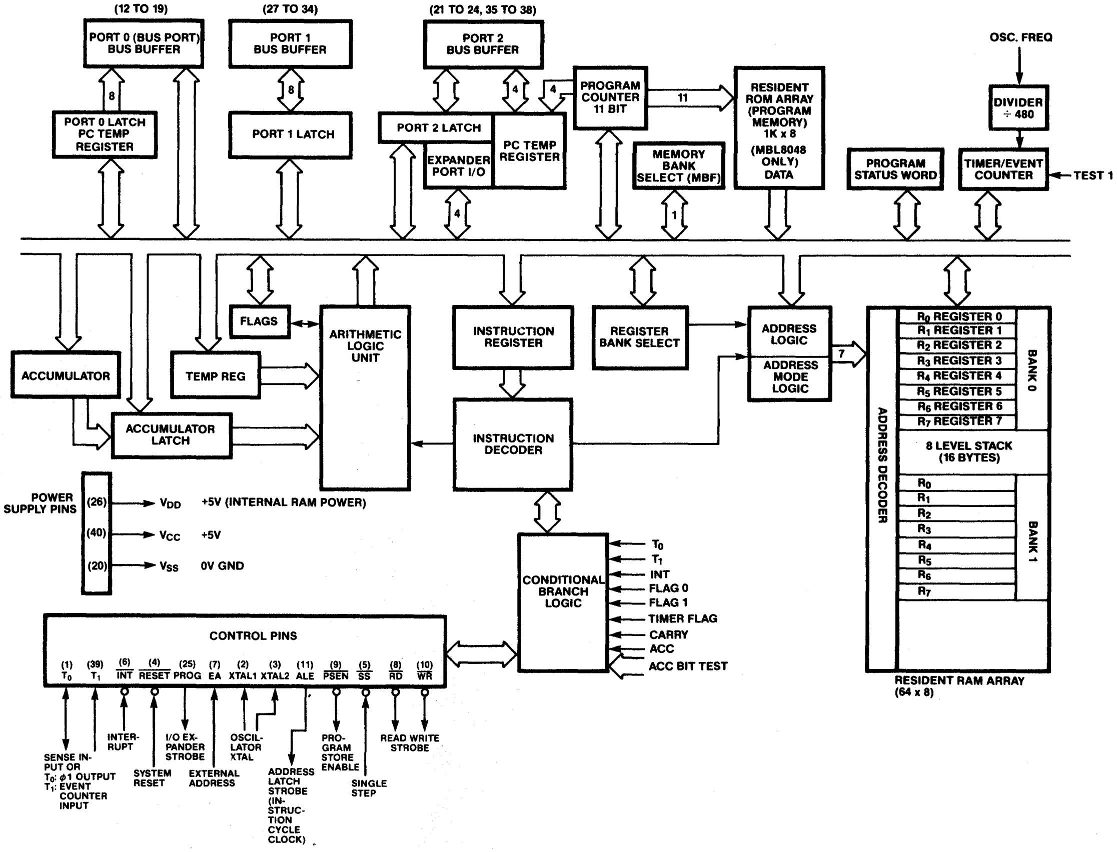


Plastic DIP
(DIP-40P-M01)

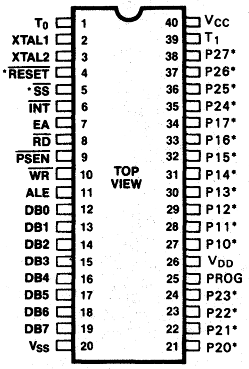
Features

- 8-bit Parallel Microcomputer
- 12-bit Addressing
- 96 Instructions: 70% Single Byte
- 1.875μs Cycle (E-Version)
  2.5μs Cycle (N-Version)
- All Instructions are 1 or 2 Cycles.
- 1K x 8 ROM (MBL8048 only)
  64 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Single Level Interrupt Capability
- Resident Clock Generator (External Frequency Source)
- External Input Capability
- Easily Expandable Memory and I/O
- 8 Level Stack
- External Program Mode Capability
- Low Power Stand-by Mode Capability
- Single +5V Power Supply
- N-channel Silicon Gate E/D MOS Process
- Standard 40-Pin DIP
- MBL8048: Compatible with Intel 8048
  MBL8035: Compatible with Intel 8035

Block Diagram



Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

*These pins are internally pulled up.

Pin Description

Pin No.	Pin Name	Symbol	Function
1	Sense	T_0	This pin has the following functions according to instructions. 1) Output of clock (ϕ1) 2MHz at 6MHz XTAL 2) Condition input for a Conditional Branch
2	Crystal 1	XTAL 1	This is an input terminal for the internal Clock Generator to be connected to a terminal of the external crystal. Also, this pin can be used as the input from an external clock source. Note: This input is not compatible with TTL levels.
3	Crystal 2	XTAL 2	This is an input terminal for the internal Clock Generator to be connected to the other terminal of the external crystal. Note: This input is not compatible with TTL level.
4	Reset	$\overline{\text{RESET}}$	This input forces the MPU to be reset or initialized. Note: This input is not compatible with TTL level.
5	Single Step	$\overline{\text{SS}}$	This input is used in conjunction with ALE for single step operation.
6	Interrupt	$\overline{\text{INT}}$	This input is used to request an external interrupt.
7	External Address	EA	When EA goes high while $\overline{\text{RESET}}$ is low, an external address (memory) can be used as the external program operation mode.
8	Read	$\overline{\text{RD}}$	This output is used as a strobe signal for an input of data from the data port (DB port). Also, it can be used as a read-enable signal when using an external data memory.
9	Program Store Enable	$\overline{\text{PSEN}}$	This output signal is generated at a fetch cycle in the external program operation mode. It is used as an enable signal for an external program memory.
10	Write	$\overline{\text{WR}}$	This output is a strobe signal for a data output from the DB port. Also, it can be used as a write-enable signal for an external data memory.
11	Address Latch Enable	ALE	This output signal is generated at the beginning of a fetch cycle both in the internal and external progaram memory operations. This output is used as a synchronizing signal with an external circuit and also, as a strobe signal for address outputs (A_0 thru A_7) of the DB port in the external program operation mode.
12 thru 19	Data Bus Port	DB0 thru DB7	These pins are used as a bidirectional 8-bit input/output port (DB port). When an external memory is used as a program memory or data memory, this port is used as an address bus (A_0 thru A_7) or data input/output port, respectively.
20	Power Supply	V_{SS}	This pin is used as the Ground (GND) terminal.
21 thru 24	Port 2	P20 thru P23	These are the lower four bits of a quasi-bidirectional input/output port (P2 port) which are used as address outputs (A_8 thru A_{11}) in a fetch cycle of the external program memory operation mode. When an expansion I/O instruction is executed, these are switched to an I/O expander bus for use with the MBL8243.

Pin Description
(Continued)

Pin No.	Pin Name	Symbol	Function
25	Program	PROG	This output is used as a strobe signal for an I/O expander (MBL8243) when performing an expansion I/O instruction.
26	Power Supply	V_{DD}	This is used as the power supply terminal (+5V) for the built-in RAM
27 thru 34	Port 1	$P1_0$ thru $P1_7$	This is a quasi-bidirectional input/output port (P1 port)
35 thru 38	Port 2	$P2_4$ thru $P2_7$	These are the upper four bits of the quasi-bidirectional input/output port 2 (P2).
39	Sense	T_1	This pin has the following functions according to the instruction given: 1) Event Input for Event Counter 2) Condition Input for Conditional Branch
40	Power Supply	V_{CC}	This is used as the power supply terminal (+5V). In stand-by operation mode this terminal is connected to GND.

Functional Descriptions for Basic Blocks

Block Name	Function
Clock Generation Circuitry	A master clock signal within a frequency range of 1MHz to 6MHz is supplied from the built-in Clock Generator using an external crystal and capacitor network, or from an external signal source. The frequency of the master clock is divided through the 1/3 Frequency Divider to generate a state clock signal. Then, the frequency of the state clock is divided through the 1/5 Frequency Divider to generate a final cycle clock signal. The state clock can be transferred to the T_0 terminal by an instruction. The cycle clock is used for internal operations and is also available on the ALE terminal.
I/O Port	Three bidirectional or quasi-bidirectional 8-bit I/O ports and three input terminals are provided for signal inputs and outputs. Port 0 (Bus Port) and the lower 4 bits of Port 2 shown in the Block Diagram are used for access to external memories or I/O expanders.
Built-in ROM and RAM	In the MBL8048, programs are stored in the built-in ROM (1 Byte). Also, the contents in the ROM can be used as data for some instructions. The built-in RAM (64 Bytes) is used for general register area, stack area and working area. ROM is expandable up to a total of 4K Bytes with externally attached ROM by switching the memory bank. RAM is expandable by an additional 256 Bytes with externally attached RAM. MBL8035 does not have any built-in ROM. It uses external ROM for program storing.
Program Counter	The program counter is an 11-bit register which indicates a fetch address of program memory and is incremented by every execution of an instruction.

Functional Descriptions for Basic Blocks

(Continued)

Block Name	Function
Instruction Register	The Instruction Register is an 8-bit register which stores a fetched instruction in a fetch cycle.
Instruction Decoder	The Instruction Decoder decodes the instruction stored in the Instruction register and generates various control signals for both internal circuitry and external peripherals.
Arithmetic Logic Unit (ALU)	Various operations such as addition, subtraction, comparison, etc., are executed in the ALU. Operation to be executed is determined from the decoding of an instruction.
Interval Timer/Event Counter	The Interval Timer/Event Counter is an 8-bit register which can be controlled by instruction execution. The interval timer mode or event counter mode can be designated by instruction execution, as well. This register is not initialized by the RESET signal. In the interval timer mode, the register can count up the frequency signal which is generated by dividing the cycle clock frequency by 32. When the source oscillation frequency is 6MHz, this enables the register to count a time interval of up to 20.48ms with resolution of 80μs. In this mode, the register generates an interrupt vector address (Address 07), if the register overflows from $(FF)_{16}$ to $(00)_{16}$. Even if an overflow occurs, the register can continue to count up. This enables the register to count a longer time interval by using proper software. In the event counter mode, the register counts on the falling edge of the T_1 input. In this mode, the features of the register other than the counting trigger are the same as those in the interval timer mode. Note: The T_1 input pulse has a 500ns Min. pulse width and a 7.5μs Min. cycle time at 6MHz of source oscillation.
Status Register Including Stack Pointer	The Status Register is an 8-bit register which consists of four bits for flags, three bits for the Stack Pointer and an unused bit. The flag bits indicate the status of the MPU. The Stack Pointer indicates with its three bits an address in the stack area to be used in the next subroutine call or interrupt.

Resident Data Memory Map (RAM)

Address (Hex)		
0	R_0 Register 0	Register Bank 0
1	R_1 Register 1	
2	R_2 Register 2	
3	R_3 Register 3	
4	R_4 Register 4	
5	R_5 Register 5	
6	R_6 Register 6	
7	R_7 Register 7	
8		Stack Register (16 Bytes) (8 Level Stack)
9		
≀	PC_L	
	CY HC FO BS PC_H	
≀		
16		
17		
18	R_0 Register 0	Register Bank 1
19	R_1 Register 1	
1A	R_2 Register 2	
1B	R_3 Register 3	
1C	R_4 Register 4	
1D	R_5 Register 5	
1E	R_6 Register 6	
1F	R_7 Register 7	
20	Working Area (32 Bytes)	
21		
22		
≀		
3D		
3E		
3F		

Status Register (PSW)

The Status Register is an 8-bit register configured as shown in the following figure. The upper four bits are used for flags to indicate the status of the MPU, and when a sub-routine call or an interrupt occurs, the contents of the program counter is transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining one bit is an unused bit.

7	6	5	4	3	2	1	0
CY	HC	F_0	BS	Blank (Unused Bit)	SP_2	SP_1	SP_0
←Flags→					←Stack Pointer→		

Flags

CY (Carry): When an overflow occurs in the Accumulator during an operation in the ALU, "1" is set in this bit.

HC (Half Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator as a result of an addition, "1" is set in this bit.

F_0(User Flag): This flag can be controlled as a user flag by the proper instruction.

BS (Bank select): This flag can be controlled to select a Register Bank by an instruction. When BS = 0, the Register Bank 0 is selected. When BS = 1, the Register Bank 1 is selected.

Stack Register (8 Level Capability)

The Stack Register occupies 16-bytes of memory within the on-board RAM. It is configured into eight levels of two bytes each as shown in Figure 1.

Stack Pointer (SP)
In Figure 1., "SP" indicates the stack level to be used for the next sub-routine call or interrupt. The Stack Pointer generates one of eight address codes and resides in the lower three bits of the status register.

SP = 0 0 0 0 1 $SP_2SP_1SP_0$

Program Counter (PC)
In Figure 1., "PC_n" indicates the individual bit contents of each of the Program Counter bits.

Interrupt Operation
There are two interrupt modes, external interrupts, and timer/counter interrupts.

When either interrupt occurs, an interrupt flag is set and upon completion of the executing instruction the interrupt is processed.

Interrupt processing is as follows:
1. The contents of the Status Register and Program Counter are saved on the Stack.

2) Program flow jumps to the address specified at address three (3) for external interrupts and address seven (7) for timer/counter interrupts.

3. Completion of the interrupt processing occurs upon execution of the RETR (Return and Restore Status) instruction.

4. The contents of the program counter and status register are restored from the stack, the interrupt flag is reset to be ready for the next interrupt, and program execution continues from where it left off.

Timer/counter interrupts occur when the overflow flag is set as a result of an overflow from the Timer/Counter.

External interrupts occur when a low level input is applied to the "INT" input.

External interrupts have priority over Timer/Counter interrupts, so if both interrupts occur at the same time the external interrupt will be processed first. After completion of the external interrupt and resetting of the interrupt flag the Timer/Counter interrupt will be processed.

Instructions
All instructions are either one or two bytes long and execute in one or two cycles. Addressing modes are classified into direct, expanded, indirect, immediate and implied.

Instruction Mode

1) 1 Byte Instruction

f

Implied Addressing Mode

f	r

Register Indirect Addressing Mode

f	r

Register Direct Addressing Mode

2) 2 Byte Instruction

f	OP

Immediate Addressing Mode

A_H	f	A_L

Expanded Addressing Mode

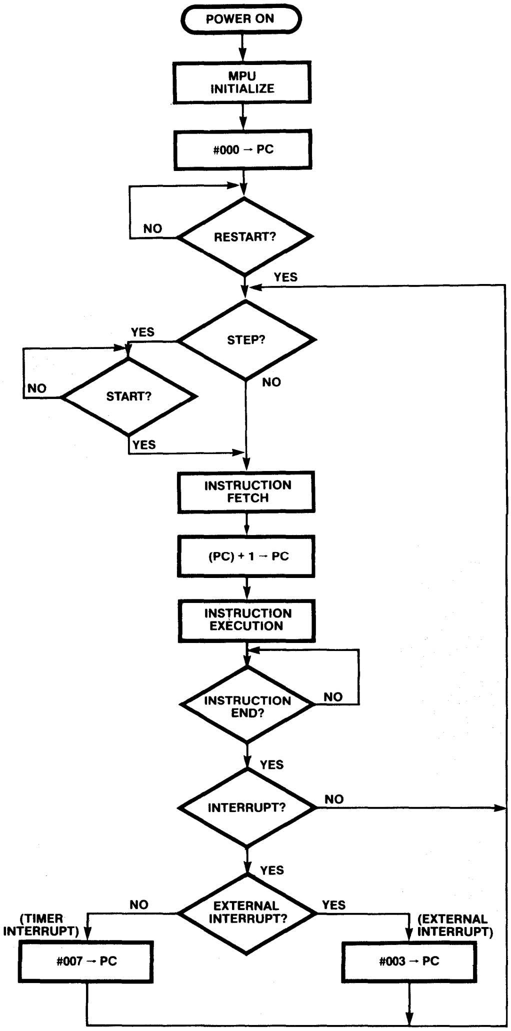
f: Instruction Operation Set
r: Register Set
OP: Operand Data
A_H, A_L: Operand Address

Figure 1.

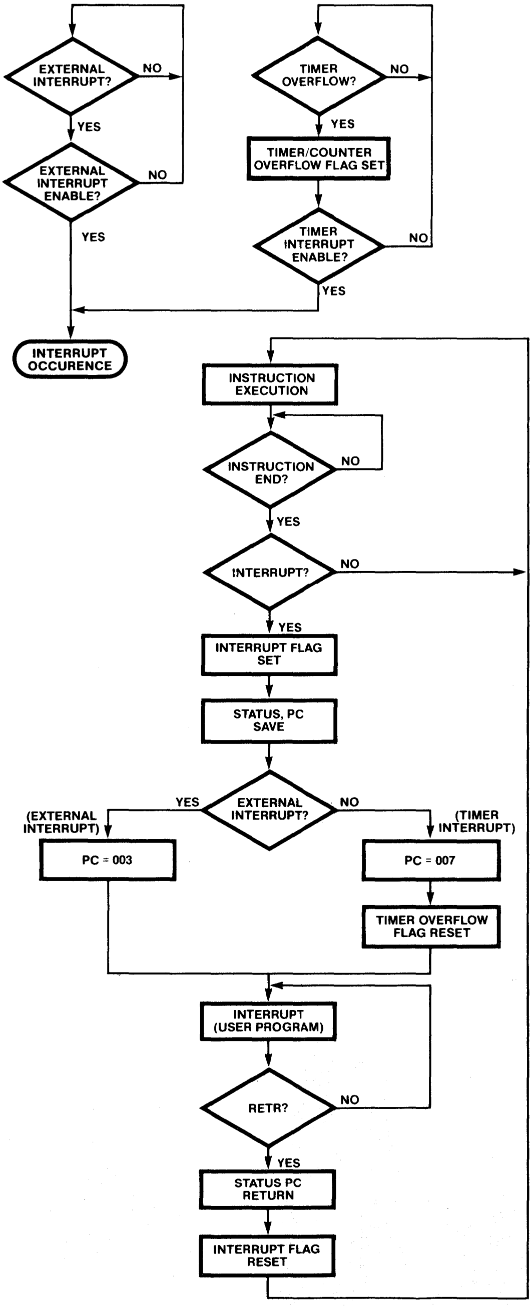
	7	6	5	4	3	2	1	0	
SP - 3									
SP - 2	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	A Set of 2 Bytes
SP - 1	CY	HC	F_0	BS	PC_{11}	PC_{10}	PC_9	PC_8	
SP									This level will be used at the next sub-routine call or interrupt. Stack Position SP = $00001SP_2SP_1SP_0$
SP + 1									

RAM Address

Operation Flow Chart

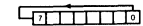
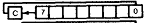
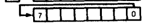
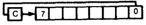


Flow Chart for Interrupt Operation



Instruction Set Summary

Accumulator

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Add register to A	ADD A,R_r	6X	1	1	*	*	—	—	$(R_r) + (A) \rightarrow (A)$
Add data memory to A	ADD A,@R_0	60	1	1	*	*	—	—	$((R_0)) + (A) \rightarrow (A)$
	ADD A,@R_1	61	1	1	*	*	—	—	$((R_1)) + (A) \rightarrow (A)$
Add immediate to A	ADD A,#data	03	2	2	*	*	—	—	data + (A) → (A)
Add register with carry	ADDC A,R_r	7X	1	1	*	*	—	—	$(R_r) + (A) + (C) \rightarrow (A)$
Add data memory with carry	ADDC A,@R_0	70	1	1	*	*	—	—	$((R_0)) + (A) + (C) \rightarrow (A)$
	ADDC A,@R_1	71	1	1	*	*	—	—	$((R_1)) + (A) + (C) \rightarrow (A)$
Add immediate to A with carry	ADDC A,#data	13	2	2	*	*	—	—	data + (A) + (C) → (A)
And register to A	ANL A,R_r	5X	1	1	—	—	—	—	$(R_r) \cap (A) \rightarrow (A)$
And data memory to A	ANL A,@R_0	50	1	1	—	—	—	—	$((R_0)) \cap (A) \rightarrow (A)$
	ANL A,@R_1	51	1	1	—	—	—	—	$((R_1)) \cap (A) \rightarrow (A)$
And immediate to A	ANL A,#data	53	2	2	—	—	—	—	data $\cap$ (A) → (A)
Clear A	CLR A	27	1	1	—	—	—	—	0 → (A)
Complement A	CPL A	37	1	1	—	—	—	—	$(\bar{A}) \rightarrow (A)$
Decimal Adjust A	DA A	57	1	1	*	—	—	—	Note (1)
Decrement A	DEC A	07	1	1	—	—	—	—	(A) -1 → (A)
Increment A	INC A	17	1	1	—	—	—	—	(A) + 1 → (A)
Or register to A	ORL A,R_r	4X	1	1	—	—	—	—	$(R_r) \cup (A) \rightarrow (A)$
Or data memory to A	ORL A,@R_0	40	1	1	—	—	—	—	$((R_0)) \cup (A) \rightarrow (A)$
	ORL A,@R_1	41	1	1	—	—	—	—	$((R_1) \cup (A) \rightarrow (A)$
Or immediate to A	ORL A,#data	43	2	2	—	—	—	—	data $\cup$ (A) → (A)
Rotate A left	RL A	E7	1	1	—	—	—	—	
Rotate A left with carry	RLC A	F7	1	1	*	—	—	—	
Rotate A right	RR A	77	1	1	—	—	—	—	
Rotate A right with carry	RRC A	67	1	1	*	—	—	—	
SWAP nibbles of A	SWAP A	47	1	1	—	—	—	—	$(A_{4\text{-}7}) \rightleftarrows (A_{0\text{-}3})$
Exclusive Or register to A	XRL A,R_r	DX	1	1	—	—	—	—	$(R_r) \oplus (A) \rightarrow (A)$
Exclusive Or data memory to A	XRL A,@R_0	D0	1	1	—	—	—	—	$((R_0)) \oplus (A) \rightarrow (A)$
	XRL A,@R_1	D1	1	1	—	—	—	—	$((R_1)) \oplus (A) \rightarrow (A)$
Exclusive Or immediate to A	XRL A,#data	D3	2	2	—	—	—	—	data $\oplus$ (A) → (A)

Instruction Set Summary
(Continued)

Input/Output

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
And immediate to BUS	ANL BUS,#data	98	2	2	—	—	—	—	data ∩ (BUS) → (BUS)
P_1	ANL P_1,#data	99	2	2	—	—	—	—	data ∩ (P_1) → (P_1)
P_2	ANL P_2,#data	9A	2	2	—	—	—	—	data ∩ (P_2) → (P_2)
And A to Expander Port	ANLD P_P,A	9X	1	2	—	—	—	—	(A) ∩ (P_P) → (P_P)
Input BUS to A	INS A,BUS	08	1	2	—	—	—	—	(BUS) → (A)
Port 1 to A	IN A,P_1	09	1	2	—	—	—	—	(P_1) → (A)
Port 2 to A	IN A,P_2	0A	1	2	—	—	—	—	(P_2) → (A)
Input Expander port to A	MOVD A,P_P	0X	1	2	—	—	—	—	(P_p) → ($A_{0\text{-}3}$) 0 → ($A_{4\text{-}7}$)
Or immediate to BUS	ORL BUS,#data	88	2	2	—	—	—	—	data ∪ (BUS) → (BUS)
P_1	ORL P_1,#data	89	2	2	—	—	—	—	data ∪ (P_1) → (P_1)
P_2	ORL P_2,#data	8A	2	2	—	—	—	—	data ∪ (P_2) → (P_2)
Or A to Expander Port	ORLD P_P,A	8X	1	2	—	—	—	—	data ∪ (P_P) → (P_P)
Output A to BUS	OUTL BUS, A	02	1	2	—	—	—	—	(A) → (BUS)
P_1	OUTL P_1,A	39	1	2	—	—	—	—	(A) → (P_1)
P_2	OUTL P_2,A	3A	1	2	—	—	—	—	(A) → (P_2)
Output A to Expander Port	MOVD P_P,A	3X	1	2	—	—	—	—	(A) → (P_P)

Data Moves

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Move register to A	MOV A,R_r	FX	1	1	—	—	—	—	(R_r) → (A)
Move data memory to A	MOV A,@R_0	F0	1	1	—	—	—	—	((R_0)) → (A)
	MOV A,@R_1	F1	1	1	—	—	—	—	((R_1)) → (A)
Move immediate to A	MOV A,#data	23	2	2	—	—	—	—	data → (A)
Move A to register	MOV R_r,A	AX	1	1	—	—	—	—	(A) → (R_r)
Move A to data memory	MOV @ R_0,A	A0	1	1	—	—	—	—	(A) → ((R_0))
	MOV @R_1,A	A1	1	1	—	—	—	—	(A) → ((R_1))
Move immediate to register	MOV R_r,#data	BX	2	2	—	—	—	—	data → (R_r)
Move immediate to data memory	MOV @R_0,#data	B0	2	2	—	—	—	—	data → ((R_0))
	MOV @R_1,#data	B1	2	2	—	—	—	—	data → ((R_1))
Move PSW to A	MOV A,PSW	C7	1	1	—	—	—	—	(PSW) → (A)
Move A to PSW	MOV PSW,A	D7	1	1	*	*	*	—	(A) → (PSW)
Move external data memory to A	MOVX A,@R_0	80	1	2	—	—	—	—	((R_0)) → (A)
	MOVX A,@R_1	81	1	2	—	—	—	—	((R_1)) → (A)
Move A to eternal data memory	MOVX @R_0,A	90	1	2	—	—	—	—	(A) → ((R_0))
	MOVX @R_1,A	91	1	2	—	—	—	—	(A) → ((R_1))
Move to A from current page	MOVP A,@A	A3	1	2	—	—	—	—	((A)) → (A)
Move to A from page 3	MOVP3 A,@A	E3	1	2	—	—	—	—	((A)) within page 3 → (A)
Exchange A and register	XCH A,R_r	2X	1	1	—	—	—	—	(R_r) ⇄ (A)
Exchange A and data memory	XCH A,@R_0	20	1	1	—	—	—	—	((R_0)) ⇄ (A)
	XCH A,@R_1	21	1	1	—	—	—	—	((R_1)) ⇄ (A)
Exchange nibble of A	XCHD A,@R_0	30	1	1	—	—	—	—	((R0)$_{0\text{-}3}$) ⇄ ($A_{0\text{-}3}$)
and data memory	XCHD A,@R_1	31	1	1	—	—	—	—	((R1)$_{0\text{-}3}$) ⇄ ($A_{0\text{-}3}$)

Instruction Set Summary
(Continued)

Registers

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Decrement Register	DEC R_r	CX	1	1	—	—	—	—	$(R_r) - 1 \rightarrow (R_r)$
Increment register	INC R_r	1X	1	1	—	—	—	—	$(R_r) + 1 \rightarrow (R_r)$
Increment data memory	INC @R_0	10	1	1	—	—	—	—	$((R_0)) + 1 \rightarrow ((R_0))$
	INC @ R_1	10	1	1	—	—	—	—	$((R_1)) + 1 \rightarrow ((R_1))$

Timer/Counter

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Disable Timer/Counter Interrupt	DIS TCNTI	35	1	1	—	—	—	—	
Enable Timer/Counter Interrupt	EN TCNTI	25	1	1	—	—	—	—	
Read Timer/Counter	MOV A,T	42	1	1	—	—	—	—	(T) → (A)
Load Timer/Counter	MOV T,A	62	1	1	—	—	—	—	(A) → (T)
Start Timer	STRT T	55	1	1	—	—	—	—	
Start Counter	STRT CNT	45	1	1	—	—	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	—	—	

Control

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Disable external Interrupt	DIS I	15	1	1	—	—	—	—	
Enable external Interrupt	EN I	05	1	1	—	—	—	—	
Enable Clock output on T_0	ENT$_0$ CLK	75	1	1	—	—	—	—	
No Operation	NOP	00	1	1	—	—	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	—	—	0 → (BS)
Select register bank 1	SEL RB1	D5	1	1	—	—	—	—	1 → (BS)
Select memory bank 0	SEL MB0	E5	1	1	—	—	—	—	0 → (MBF)
Select memory bank 1	SEL MB1	F5	1	1	—	—	—	—	1 → (MBF)

Instruction Set Summary
(Continued)

Branch

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Decrement register and test	DJNZ R addr	EX	2	2	—	—	—	—	$(R_r) \neq 0$ Note (2)
Jump unconditional	JMP addr	%4	2	2	—	—	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	—	—	Unconditional branch Note (3)
Jump on Carry = 1	JC addr	F6	2	2	—	—	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	—	—	(C) = 0
Jump on A zero	JZ addr	C6	2	2	—	—	—	—	(A) = 0
Jump on A not zero	JNZ addr	96	2	2	—	—	—	—	$(A) \neq 0$
Jump on T_0 = 1	JT0 addr	36	2	2	—	—	—	—	$(T_0) = 1$
Jump on T_0 = 0	JNT0 addr	26	2	2	—	—	—	—	$(T_0) = 0$
Jump on T_1 = 1	JT1 addr	56	2	2	—	—	—	—	$(T_1) = 1$
Jump on T_1 = 0	JNT1 addr	46	2	2	—	—	—	—	$(T_1) = 0$
Jump on F_0 = 1	JF0 addr	B6	2	2	—	—	—	—	$(F_0) = 1$
Jump on F_1 = 1	JF1 addr	76	2	2	—	—	—	—	$(F_1) = 1$
Jump on timer flag	JTF addr	16	2	2	—	—	—	—	(TF) = 1
Jump on $\overline{INT}$ = 0	JN1	86	2	2	—	—	—	—	$(\overline{INT}) = 0$
Jump on accumulator bit	JBr addr	%2	2	2	—	—	—	—	$(A_r) = 1$

Subroutine

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Jump to subroutine	CALL addr	%4	2	2	—	—	—	—	Note (4)
Return	RET	83	1	2	—	—	—	—	Note (5)
Return and restore status	RETR	90	1	2	*	*	*	—	Note (6)

Flags

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Clear carry	CLR C	97	1	1	Z	—	—	—	0 → (C)
Complement carry	CPL C	A7	1	1	CP	—	—	—	$(\overline{C}) \rightarrow (C)$
Clear Flag 0	CLR F_0	85	1	1	—	—	Z	—	0 → (F_0)
Complement Flag 0	CPL F_0	95	1	1	—	—	CP	—	$(\overline{F_0}) \rightarrow (F_0)$
Clear Flag 1	CLR F_1	A5	1	1	—	—	—	Z	0 → (F_1)
Complement Flag 1	CPL F_1	B5	1	1	—	—	—	CP	$(\overline{F_1}) \rightarrow (F_1)$

Notes:
Operation Code X: Tables-1, 2 %: Table 3
Flag*: This flag is set or reset in the state after executed instruction.
Z: This flag is reset.
CP: This flag is complemented.

1) The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.

2) DJNZ R_r, addr;
$(R_r) - 1 \rightarrow (R_r)$
if $(R_r) \neq 0$ addr → (PC_0 to PC_7)
if $(R_r) = 0$ execute next instruction

3) JMPP @A
((A)) → (PC_0 to PC_7)

4) CALL addr
(PC_0 to PC_7) → ((SP))
(SP) + 1 → (SP)
(PC_8 to PC_{11}), (MBF), (PSW_4 to PSW_7) → ((SP))
(SP) + 1 → (SP)
A_L → (PC_0 to PC_7)
A_H → (PC_8 to PC_{10})
MBF → (PC_{11})

5) RET
(SP) - 1 → (SP)
($(SP)_0$ to $(SP)_3$) → ($(PC)_8$ to $(PC)_{11}$)
(SP) - 1 → (SP)
((SP)) → (PC_0 to PC_7)

6) RETR
(SP) - 1 → (SP)
($(SP)_0$ to $(SP)_3$) → (PC_8 to PC_{11})
($(SP)_4$ to $(SP)_7$) → (PSW_4 to PSW_7)
(SP) - 1 → (SP)
((SP)) → (PC_0 to PC_7)
A_L: Lower 8 Bits of Address
A_H: A_8, A_9, A_{10} of Address
MBF: Memory Bank Flag

Instruction Set Summary
(Continued)

OP Code of Register Access (Table 1)

Mnemonic	Rr	R0	R1	R2	R3	R4	R5	R6	R7
INC Rr		18	19	1A	1B	1C	1D	1E	1F
XCH A,Rr		28	29	2A	2B	2C	2D	2E	2F
ORL A,Rr		48	49	4A	4B	4C	4D	4E	4F
ANL A,Rr		58	59	5A	5B	5C	5D	5E	5F
ADD A,Rr		68	69	6A	6B	6C	6D	6E	6F
ADDC A,Rr		78	79	7A	7B	7C	7D	7E	7F
MOV Rr,A		A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr,#data		B8	B9	BA	BB	BC	BD	BE	BF
DEC Rr		C8	C9	CA	CB	CC	CD	CE	CF
XRL A,Rr		D8	D9	DA	DB	DC	DD	DE	DF
DJNZ Rr,M		E8	E9	EA	EB	EC	ED	EE	EF
MOV A,Rr		F8	F9	FA	FB	FC	FD	FE	FF

7	6	5	4	3	2	1	0
					r_2	r_1	r_0

OP Code of Expander (Table 2)

Mnemonic	PP	P4	P5	P6	P7
MOVD A,P_P		0C	0D	0E	0F
MOVD P_P,A		3C	3D	3E	3F
ORLD P_P,A		8C	8D	8E	8F
ANLD P_P,A		9C	9D	9E	9F

7	6	5	4	3	2	1	0
						P_1	P_0

OP Code of JMP, CALL, JB_r (Table 3)

	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
JMP	A_H			0	0	1	0	0	A_L							
	First Byte								Second Byte							
CALL	A_H			1	0	1	0	0	A_L							
	First Byte								Second Byte							
JB_r	B_r			1	0	0	1	0	A_L							
	First Byte								Second Byte							

A_L; Address A_7 to A_0
A_H; Address A_{10}, A_9, A_8
B_r; r-th Bit on Accumulator

Instruction Codes

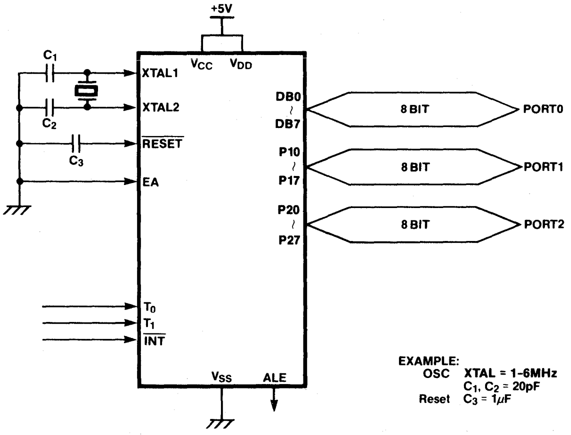
L H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUTL BSU,A	◥ ADD A, #	◥ JMP 0 x x	EN 1		DEC A	◤ INS A,BUS	◤ IN A,P1	◤ IN A,P2		◤ MOVD A,P4	◤ MOVD A,P5	◤ MOVD A,P6	◤ MOVD A,P7
1	INC @R0	INC @R1	◥ JB0 addr	◥ ADDC A #	◥ CALL 0 x x	DIS 1	◥ JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A,@R0	XCH A,@R1		◥ MOV A,#	◥ JMP 1 x x	EN TCNT1	◥ JNT0 addr	CLR A	XCH A,R0	XCH A,R1	XCH A,R2	XCH A,R3	XCH A,R4	XCH A,R5	XCH A,R6	XCH A,R7
3	XCHD A,@R0	XCHD A,@R1	◥ JB1 addr		◥ CALL 1 x x	DIS TCNT1	◥ JT0 addr	CPL A		◤ OUTL P1,A	◤ OUTL P2,A		◤ MOVD P4,A	◤ MOVD P5,A	◤ MOVD P6,A	◤ MOVD P7,A
4	ORL A,@R0	ORL A,@R1	MOV A,T	◥ ORL A,#	◥ JMP 2 x x	STRT CNT	◥ JNT1 addr	SWAP A	ORL A,R0	ORL A,R1	ORL A,R2	ORL A,R3	ORL A,R4	ORL A,R5	ORL A,R6	ORL A,R7
5	ANL A,@R0	ANL A,@R1	◥ JB2 addr	◥ ANL A,#	◥ CALL 2 x x	STRT T	◥ JT1 addr	DA A	ANL A,R0	ANL A,R1	ANL A,R2	ANL A,R3	ANL A,R4	ANL A,R5	ANL A,R6	ANL A,R7
6	ADD A,@R0	ADD A,@R1	MOV T,A		◥ JMP 3 x x	STOP TCNT		RRC A	ADD A,R0	ADD A,R1	ADD A,R2	ADD A,R3	ADD A,R4	ADD A,R5	ADD A,R6	ADD A,R7
7	ADDC A,@R0	ADDC A,@R1	◥ JB3 addr		◥ CALL 3 x x	ENT0 CLK	◥ JF1 addr	RR A	ADDC A,R0	ADDC A,R1	ADDC A,R2	ADDC A,R3	ADDC A,R4	ADDC A,R5	ADDC A,R6	ADDC A,R7
8	◤ MOVX A,@R0	◤ MOVX A,@R1		◤ RET	◥ JMP 4 x x	CLR F0	◥ JN1 addr		◥ ORL BUS,#	◥ ORL P1,#	◥ ORL P2,#		◤ ORLD P4,A	◤ ORLD P5,A	◤ ORLD P6,A	◤ ORLD P7,A
9	◤ MOVX @R0,A	◤ MOVX @R1,A	◥ JB4 addr	◤ RETR	◥ CALL 4 x x	CPL F0	◥ JNZ addr	CLR C	◥ ANL BUS,#	◥ ANL P1,#	◥ ANL P2,#		◤ ANLD P4,A	◤ ANLD P5,A	◤ ANLD P6,A	◤ ANLD P7,A
A	MOV @R0,A	MOV @R1,A		◤ MOVP A,@A	◥ JMP 5 x x	CLR F1		CPL C	MOV R0,A	MOV R1,A	MOV R2,A	MOV R3,A	MOV R4,A	MOV R5,A	MOV R6,A	MOV R7,A
B	◥ MOV @R0,#	◥ MOV @R1,#	◥ JB5 addr	◤ JMPP @A	◥ CALL 5 x x	CPL F1	◥ JF0 addr		◥ MOV R0, #	◥ MOV R1, #	◥ MOV R2, #	◥ MOV R3, #	◥ MOV R4, #	◥ MOV R5, #	◥ MOV R6, #	◥ MOV R7, #
C					◥ JMP 6 x x	SEL RB0	◥ JZ addr	MOV A,PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A,@R0	XRL A,@R1	◥ JB6 addr	◥ XRL A#	◥ CALL 6 x x	SEL RB1		MOV PSW,A	XRL A,R0	XRL A,R1	XRL A,R2	XRL A,R3	XRL A,R4	XRL A,R5	XRL A,R6	XRL A,R7
E				◤ MOVP3 A,@A	◥ JMP 7 x x	SEL MB0	◥ JNC addr	RL A	◥ DJNZ R0,M	◥ DJNZ R1,M	◥ DJNZ R2,M	◥ DJNZ R3,M	◥ DJNZ R4,M	◥ DJNZ R5,M	◥ DJNZ R6,M	◥ DJNZ R7,M
F	MOV A,@R0	MOV A,@R1	◥ JB7 addr		◥ CALL 7 x x	SEL MB1	◥ JC addr	RLC A	MOV A,R0	MOV A,R1	MOV A,R2	MOV A,R3	MOV A,R4	MOV A,R5	MOV A,R6	MOV A,R7

#: Immediate data
H; Higher 4 bits
L; Lower 4 bits

□	Single-byte, Single-cycle Instruction
◤	Single-byte, Two-cycle Instruction
◥	Two-byte, Two-cycle Instruction

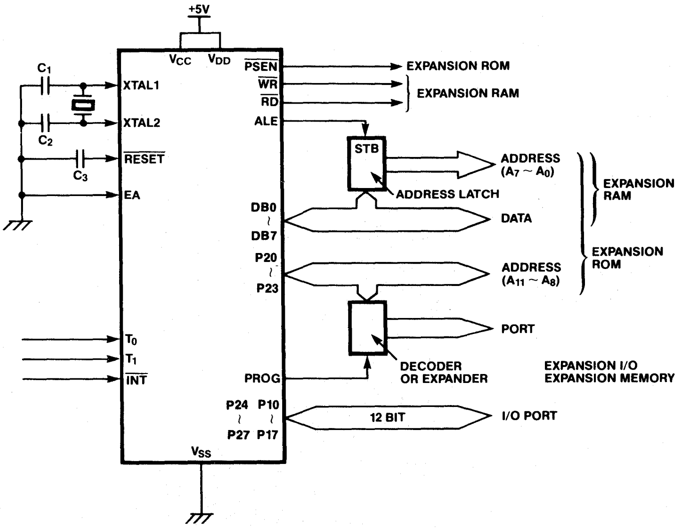
Typical Applications

(1) Stand Alone System



EXAMPLE:
OSC XTAL = 1-6MHz
C_1, C_2 = 20pF
Reset C_3 = 1μF

(2) Expanded System



Absolute Maximum Ratings†

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

†Permanent device damage may occur if the ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliabilty.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	+5.0 ±10%	V
	V_{SS}	0	V
Operating Temperature	T_A	0 to +70	°C

DC Characteristics

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Value Min.	Value Max.	Unit
Input Low Voltage	All Except XTAL1, 2, $\overline{\text{RESET}}$	V_{IL}		-0.3	0.8	V
	XTAL1,2, $\overline{\text{RESET}}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All Except XTAL1, 2, $\overline{\text{RESET}}$	V_{IH}		2.0	V_{CC}	V
	XTAL1,2, $\overline{\text{RESET}}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	BUS	V_{OL}	I_{OL} = 2.0mA		0.45	V
	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE	V_{OL1}	I_{OL} = 2.0mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
	Other outputs	V_{OL3}	I_{OL} = 1.6mA		0.45	V
Output High Voltage	BUS	V_{OH}	I_{OH} = -400μA	2.4		V
	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE	V_{OH1}	I_{OH} = -100μA	2.4		V
	Other Outputs	V_{OH2}	I_{OH} = -50μA	2.4		V
Input Leakage Current	T_1, $\overline{\text{INT}}$	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$		±10	μA
	P10-P17, P20-P27 EA, $\overline{\text{SS}}$	I_{IL1}	V_{SS} + 0.45V≤ $V_{IN} \leq V_{CC}$		-500	μA
Output Leakage Current	BUS, T_0 (High-Impedance)	I_{OL}	V_{SS} + 0.45V≤ $V_{IN} \leq V_{CC}$		±10	μA
V_{DD} Supply Current	MBL8048/35 N/E	I_{DD}			15	mA
	MBL8048/35 H				25	mA
Total Supply Current	MBL8048/35 N/E	I_{DD} + I_{CC}			135	mA
	MBL8048/35 H				155	mA

AC Characteristics*

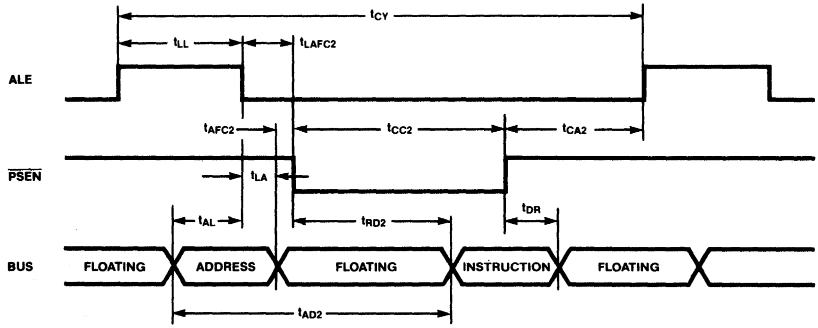
(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V

		H-Version		E-Version		N-Version		
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
ALE Pulse Width	t_{LL}	150		260		410		ns
Address Setup Time (to ALE↓)	t_{AL}	70		140		230		ns
Address Hold Time (from ALE↓)	t_{LA}	50		80		120		ns
Control Pulse Width (RD, WR)	t_{CC1}	480		730		1050		ns
Control Pulse Width (PSEN)	t_{CC2}	350		550		800		ns
Data Setup Time (before WR↑)	t_{DW}	390		610		880		ns
Data Hold Time (after WR↑)**	t_{WD}	40		80		120		ns
Data Hold Time (after RD↑, PSEN↑)	t_{DR}	0	110	0	160	0	220	ns
Data Delayed Time (RD↓ to data in)	t_{RD1}		350		550		800	ns
Data Delayed Time (PSEN↓ to data in)	t_{RD2}		210		360		550	ns
Address Setup Time (to WR↓)	t_{AW}	310		480		680		ns
Address Setup Time (RD, to data in)	t_{AD1}		760		1130		1590	ns
Address Setup Time (PSEN, to data in)	t_{AD2}		480		750		1090	ns
Address Floating Time (to RD↓, WR↓)	t_{AFC1}	140		210		290		ns
Address Floating Time (to PSEN↓)	t_{AFC2}	10		20		40		ns
RD, WR Output Time (from ALE↓)	t_{LAFC1}	200		300		420		ns
PSEN Output Time (from ALE↓)	t_{LAFC2}	60		110		170		ns
ALE Output Time (from RD↑, WR↑, PROG↑)	t_{CA1}	50		80		120		ns
ALE Output Time (from PSEN↑)	t_{CA2}	320		460		620		ns
Port Control Setup Before Falling Edge of PROG Time	t_{CP}	100		170		250		ns
Port Control Hold After Falling Edge of PROG Time	t_{PC}	160		300		460		ns
PROG Time P2 Input Must Be Valid	t_{PR}		700		1000		1380	ns
P2 Input Data Hold Time (after PROG↑)	t_{PF}	0	140	0	190	0	250	ns
Output Data Setup Time (to PROG↑)	t_{DP}	400		600		850		ns
Output Data Hold Time (after PROG↑)	t_{PD}	90		130		200		ns
PROG Pulse Width	t_{PP}	700		1060		1500		ns
Port2 I/O Data Setup Time (to ALE↑)	t_{PL}	160		300		460		ns
Port2 I/O Data Hold Time (from ALE↑)	t_{LP}	40		60		80		ns
Port Data Output Time (from ALE↓)	t_{PV}		510		660		850	ns
Cycle Time***	t_{CY}	1.36		1.875		2.5		µs
T_0 Output Cycle Time	t_{OPRR}	270		370		500		ns

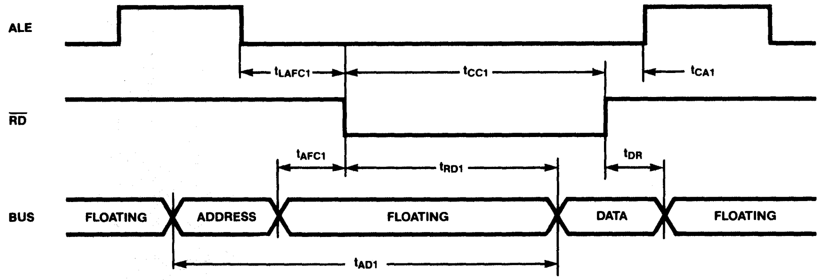
*: 6MHz XTAL (N-Version), 8MHz XTAL (E-Version), 11MHz XTAL (H-Version) Load Conditions: BUS: C_L = 150pF; Other Outputs C_L = 80pF
**: Load Conditions C_L = 20pF, High Impedance
***; t_{CY} = 2.5µs (6MHz XTAL N-Version), t_{CY} = 1.875µs (8MHz XTAL E-Version), t_{CY} = 1.36µs (11MHz XTAL H-Version)

Timing Diagram

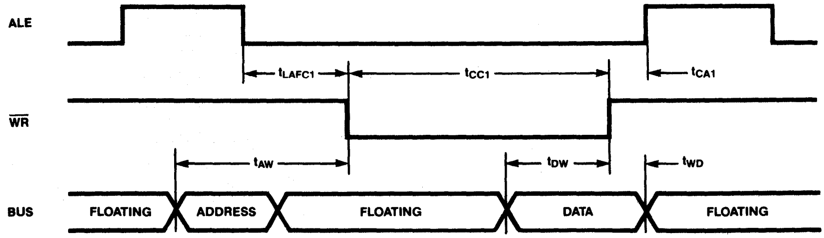
Instruction Fetch From External Program Memory



Read From External Data Memory

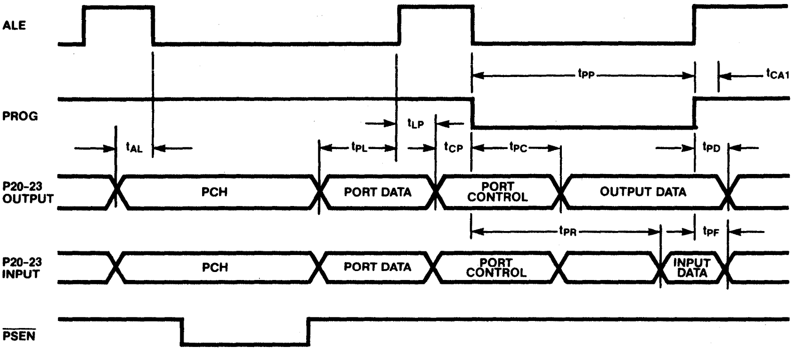


Write To External Data Memory

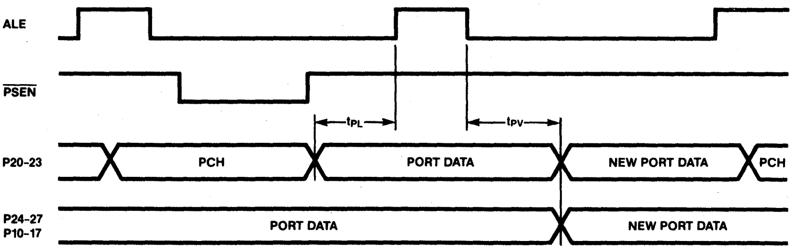


Timing Diagram
(Continued)

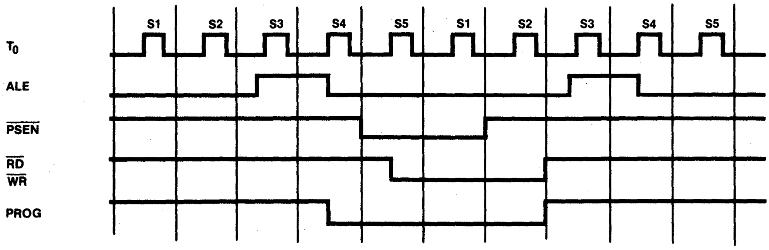
P20-23 Input/Output For Use Of External Program Memory And Expander I/O Port



Port 1/Port 2 Outputs



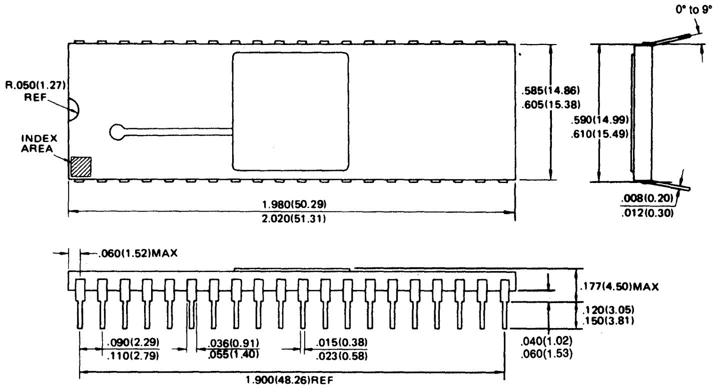
Clock Outputs



Package Dimensions

Dimensions in inches
(millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)



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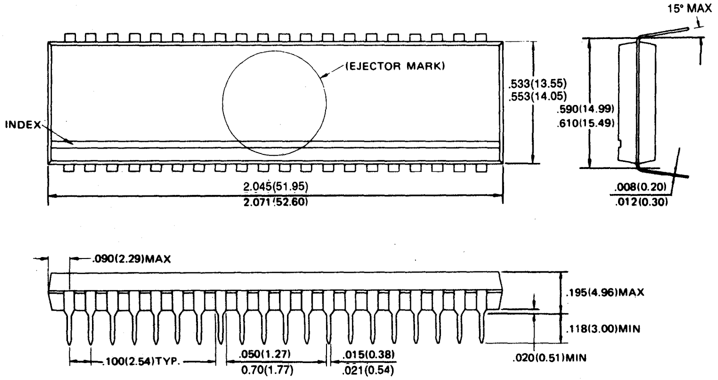
40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



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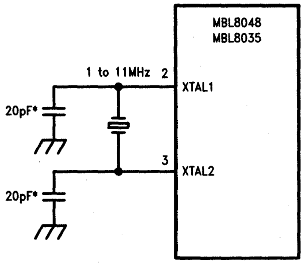
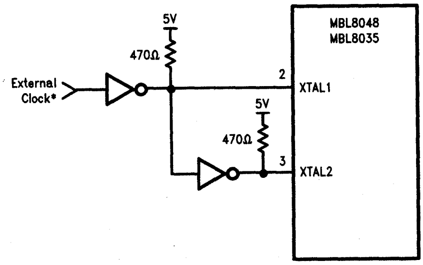
Oscillation Circuits

Crystal Oscillator



*Including stray capacitances

External Clock Drive



*Both high and low times should be more than 35% of the cycle time, and rise and fall times should be less than 20ns.

Advanced Products **FUJITSU**

October 1986
Edition 1.0

MBL8049N/E/H MBL8039N/E/H

NMOS Single-Chip 8-Bit Microcomputer

Description

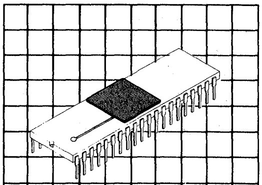
The Fujitsu MBL8049/MBL8039 is a totally self-contained 8-bit parallel one-chip microcomputer fabricated with an N-channel silicon gate MOS process.

The MBL8049 has a 2K × 8 ROM program memory, a 128 × 8 RAM data memory, 27 I/O ports, an 8-bit timer/counter and clock generator on chip. A single power supply of +5V is used. The MBL8039 is identical to the MBL8049 except without program memory. It can be used with external memory for system prototyping and preproduction systems.

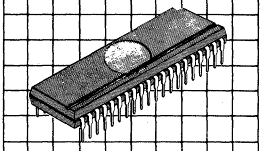
The design is optimized for low cost, high performance applications because the MBL8049/MBL8039 is fabricated on a single silicon chip and can be used for applications that require additional expansion of ROMs, RAMs, I/O port, etc.

This microcomputer permits external program operation and a single-step operation mode. Low power applications are possible by using the stand-by mode feature.

The MBL8049/MBL8039 is packaged in a standard 40-pin DIP package and operation is guaranteed from 0°C to 70°C.



Ceramic DIP (DIP-40C-A01)

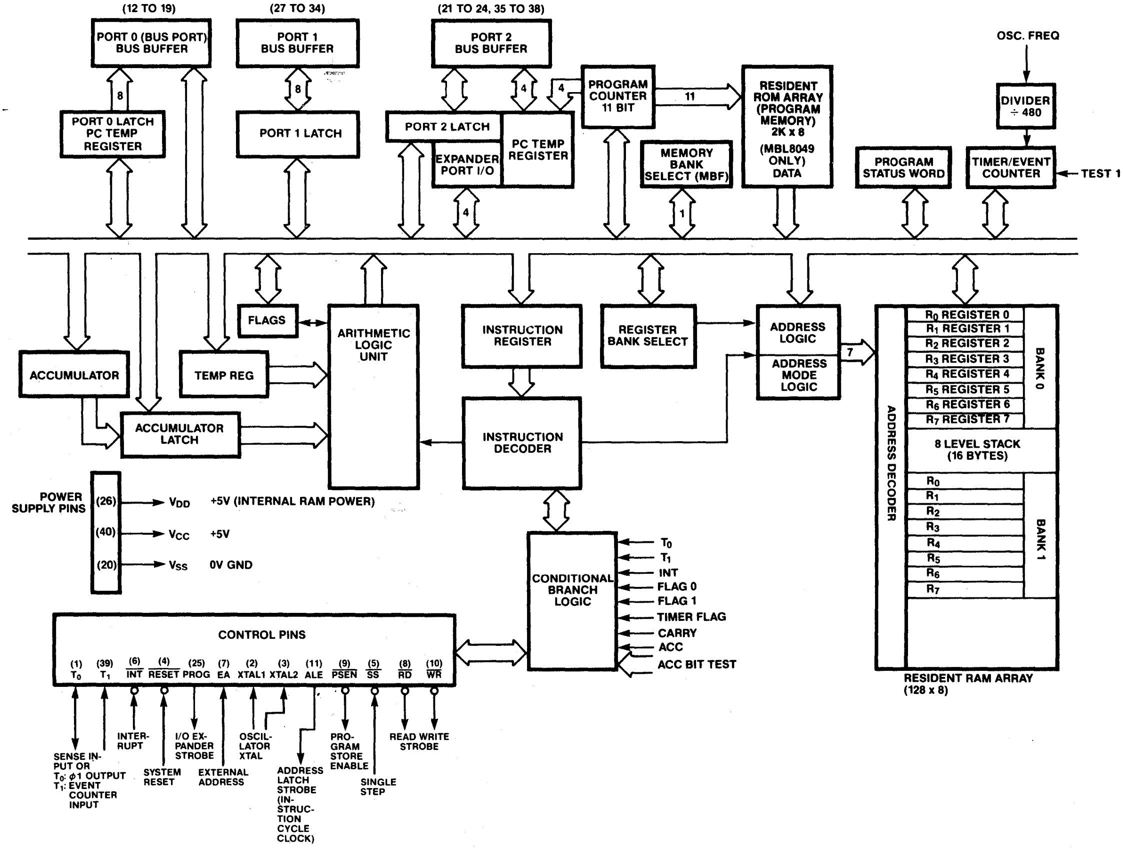


Plastic DIP (DIP-40P-M01)

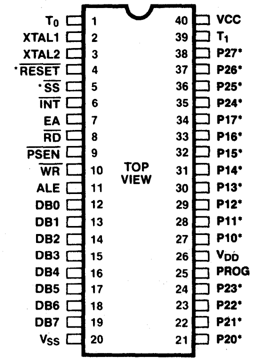
Features

- **8-bit Parallel Microcomputer**
- **12-bit Addressing**
- **96 Instructions: 70% Single Byte**
- **1.875μs Cycle (E-Version)**
  2.5μs Cycle (N-Version)
  All Instructions are 1 or 2 Cycles.
- **2K x 8 ROM (MBL8049 only)**
  128 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Single Level Interrupt Capability**
- **Resident Clock Generator (External Frequency Source)**
- **External Input Capability**
- **Easily Expandable Memory and I/O**
- **8 Level Stack**
- **External Program Mode Capability**
- **Low Power Stand-by Mode Capability**
- **Single +5V Power Supply**
- **N-channel Silicon Gate E/D MOS Process**
- **Standard 40-Pin DIP**
- **MBL8049: Compatible with Intel 8049**
  MBL8039: Compatible with Intel 8039

Block Diagram



Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

*These pins are internally pulled up.

Pin Description

Pin No.	Pin Name	Symbol	Function
1	Sense	T_0	This pin has the following functions according to instructions. 1) Output of clock (ϕ1) 2MHz at 6 MHz XTAL 2) Condition input for a Conditional Branch
2	Crystal 1	XTAL 1	This is an input terminal for the internal Clock Generator to be connected to a terminal of the external crystal. Also, this pin can be used as the input from an external clock source. Note: This input is not compatible with TTL levels.
3	Crystal 2	XTAL 2	This is an input terminal for the internal Clock Generator to be connected to the external crystal. Note: This input is not compatible with TTL level.
4	Reset	$\overline{\text{RESET}}$	This input forces the MPU to be reset or initialized. Note: This input is not compatible with TTL level.
5	Single Step	$\overline{\text{SS}}$	This input is used in conjunction with ALE for single step operation.
6	Interrupt	$\overline{\text{INT}}$	This input is used to request an external interrupt.
7	External Address	EA	When EA goes high while $\overline{\text{RESET}}$ is low, an external address (memory) can be used as the external program operation mode.
8	Read	$\overline{\text{RD}}$	This output is used as a strobe signal for an input of data from the data bus port (DB port). Also, it can be used as a read-enable signal when using an external data memory.
9	Program Store Enable	$\overline{\text{PSEN}}$	This output signal is generated at a fetch cycle in the external program operation mode. It is used as an enable signal for an external program memory.
10	Write	$\overline{\text{WR}}$	This output is a strobe signal for a data output from the DB port. Also, it can be used as a write-enable signal for an external data memory.
11	Address Latch Enable	ALE	This output signal is generated at the beginning of a fetch cycle both in the internal and external program memory operations. This output is used as a synchronizing signal with an external circuit and also, as a strobe signal for address outputs (A_0 thru A_7) of the DB port in the external program operation mode.
12 thru 19	Data Bus Port	DB0 thru DB7	These pins are used as a bidirectional 8-bit input/output port (DB port). When an external memory is used as a program memory or data memory, this port is used as an address bus (A_0 thru A_7) or data input/output port, respectively.
20	Power Supply	V_{SS}	This pin is used as the Ground (GND) terminal.
21 thru 24	Port 2	P20 thru P23	These are the lower four bits of a quasi-bidirectional input/output port (P2 port) which are used as address outputs (A_8 thru A_{11}) in a fetch cycle of the external program memory operation mode. When an expansion I/O instruction is executed, these are switched to an I/O expander bus for use with the MBL8243.

Pin Description
(Continued)

Pin No.	Pin Name	Symbol	Function
25	Program	PROG	This output is used as a strobe signal for an I/O expander (MBL8243) when performing an expansion I/O instruction.
26	Power Supply	V_{DD}	This is used as the power supply terminal (+5V) for the built-in RAM.
27 thru 34	Port 1	$P1_0$ thru $P1_7$	This is a quasi-bidirectional input/output port (P1 port)
35 thru 38	Port 2	$P2_4$ thru $P2_7$	These are the upper four bits of the quasi-bidirectional input/output port 2 (P2).
39	Sense	T_1	This pin has the following functions according to the instruction given: 1) Event Input for Event Counter 2) Condition Input for Conditional Branch
40	Power Supply	V_{CC}	This is used as the power supply terminal (+5V). In stand-by operation mode this terminal is connected to GND.

Functional Descriptions for Basic Blocks

Block Name	Function
Clock Generation Circuitry	A master clock signal within a frequency range of 1MHz to 6MHz is supplied from the built-in Clock Generator using an external crystal and capacitor network, or from an external signal source. The frequency of the master clock is divided through the 1/3 Frequency Divider to generate a state clock signal. Then, the frequency of the state clock is divided through the 1/5 Frequency Divider to generate a final cycle clock signal. The state clock can be transferred to the T_0 terminal by an instruction. The cycle clock is used for internal operations and is also available on the ALE terminal.
I/O Port	Three bidirectional or quasi-bidirectional 8-bit I/O ports and three input terminals are provided for signal inputs and outputs. Port 0 (Bus Port) and the lower 4 bits of Port 2 shown in the Block Diagram are used for access to external memories or I/O expanders.
Built-in ROM and RAM	In the MBL8049, programs are stored in the built-in ROM (2K Bytes). Also, the contents in the ROM can be used as data for some instructions. The built-in RAM (128 bytes) is used for general register area, stack area and working area. ROM is expandable up to a total of 4K Bytes with externally attached ROM by switching the memory bank. RAM is expandable by an additional 256 Bytes with externally attached RAM. MBL8039 does not have any built-in ROM. It uses external ROM for program storing.
Program Counter	The program counter is an 11-bit register which indicates a fetch address of program memory and is incremented by every execution of an instruction.

Functional Descriptions for Basic Blocks
(Continued)

Block Name	Function
Instruction Register	The Instruction Register is an 8-bit register which stores a fetched instruction in a fetch cycle.
Instruction Decoder	The Instruction Decoder decodes the instruction stored in the Instruction register and generates various control signals for both internal circuitry and external peripherals.
Arithmetic Logic Unit (ALU)	Various operations such as addition, subtraction, comparison, etc., are executed in the ALU. Operation to be executed is determined from the decoding of an instruction.
Interval Timer/Event Counter	The Interval Timer/Event Counter is an 8-bit register which can be controlled by instruction execution. The interval timer mode or event counter mode can be designated by instruction execution, as well. This register is not initialized by the RESET signal. In the interval timer mode, the register can count up the frequency signal which is generated by dividing the cycle clock frequency by 32. When the source oscillation frequency is 6MHz, this enables the register to count a time interval of up to 20.48ms with resolution of 80μs. In this mode, the register generates an interrupt vector address (Address 07), if the register overflows from $(FF)_{16}$ to $(00)_{16}$. Even if an overflow occurs, the register can continue to count up. This enables the register to count a longer time interval by using proper software. In the event counter mode, the register counts on the falling edge of the T_1 input. In this mode, the features of the register other than the counting trigger are the same as those in the interval timer mode. Note: The T_1 input pulse has a 500ns Min. pulse width and a 7.5μs Min. cycle time at 6MHz of source oscillation.
Status Register Including Stack Pointer	The Status Register is an 8-bit register which consists of four bits for flags, three bits for the Stack Pointer and an unused bit. The flag bits indicate the status of the MPU. The Stack Pointer indicates with its three bits, an address in the stack area to be used in the next subroutine call or interrupt.

Resident Data Memory Map (RAM)

Address (Hex)		
0	R_0 Register 0	Register Bank 0
1	R_1 Register 1	
2	R_2 Register 2	
3	R_3 Register 3	
4	R_4 Register 4	
5	R_5 Register 5	
6	R_6 Register 6	
7	R_7 Register 7	
8		Stack Register (16 Bytes) (8 Level Stack)
9		
≀		
SP-2	PC_L	
SP-1	CY HC FO BS PC_H	
SP		
≀		
16		
17		
18	R_0 Register 0	Register Bank 1
19	R_1 Register 1	
1A	R_2 Register 2	
1B	R_3 Register 3	
1C	R_4 Register 4	
1D	R_5 Register 5	
1E	R_6 Register 6	
1F	R_7 Register 7	
20	Working Area (96 Bytes)	
21		
22		
≀		
7D		
7E		
7F		

Status Register (PSW)

The Status Register is an 8-bit register configured as shown in the following figure. The upper four bits are used for flags to indicate the status of the MPU, and when a sub-routine call or an interrupt occurs, the contents of the program counter is transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining one bit is an unused bit.

7	6	5	4	3	2	1	0
CY	HC	F_0	BS	Blank (Unused Bit)	SP_2	SP_1	SP_0
←Flags→					←Stack Pointer→		

Flags

CY (Carry): When an overflow occurs in the Accumulator during an operation in the ALU, "1" is set in this bit.

HC (Half Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator as a result of an addition, "1" is set in this bit.

F_0(User Flag): This flag can be controlled as a user flag by the proper instruction.

BS (Bank select): This flag can be controlled to select a Register Bank by an instruction. When BS = 0, the Register Bank 0 is selected. When BS = 1, the Register Bank 1 is selected.

Stack Register (8 Level Capability)
The Stack Register occupies 16-bytes of memory within the on-board RAM. It is configured into eight levels of two bytes each as shown in Figure 1.

Stack Pointer (SP)
In Figure 1., "SP" indicates the stack level to be used for the next sub-routine call or interrupt. The Stack Pointer generates one of eight address codes and resides in the lower three bits of the status register.

SP = 0 0 0 0 1 $SP_2SP_1SP_0$

Program Counter (PC)
In Figure 1., "PC_n" indicates the individual bit contents of each of the Program Counter bits.

Interrupt Operation
There are two interrupt modes, external interrupts, and timer/counter interrupts.

When either interrupt occurs, an interrupt flag is set and upon completion of the executing instruction the interrupt is processed.

Interrupt processing is as follows:
1. The contents of the Status Register and Program Counter are saved on the Stack.

2. Program flow jumps to the address specified at address three (3) for external interrupts and address seven (7) for timer/counter interrupts.

3. Completion of the interrupt processing occurs upon execution of the RETR (Return and Restore Status) instruction.

4. The contents of the program counter and status register are restored from the stack, the interrupt flag is reset to be ready for the next interrupt, and program execution continues from where it left off.

Timer/counter interrupts occur when the overflow flag is set as a result of an overflow from the Timer/Counter.

External interrupts occur when a low level input is applied to the "INT" input.

External interrupts have priority over Timer/Counter interrupts, so if both interrupts occur at the same time the external interrupt will be processed first. After completion of the external interrupt and resetting of the interrupt flag the Timer/ Counter interrupt will be processed.

Instructions
All instructions are either one or two bytes long and execute in one or two cycles. Addressing modes are classified into direct, expanded, indirect, immediate and implied.

Instruction Mode

1) 1 Byte Instruction

f

Implied Addressing Mode

f	r

Register Indirect Addressing Mode

f	r

Register Direct Addressing Mode

2) 2 Byte Instruction

f	OP

Immediate Addressing Mode

A_H	f	A_L

Expanded Addressing Mode

f: Instruction Operation Set
r: Register Set
OP: Operand Data
A_H, A_L: Operand Address

Figure 1.

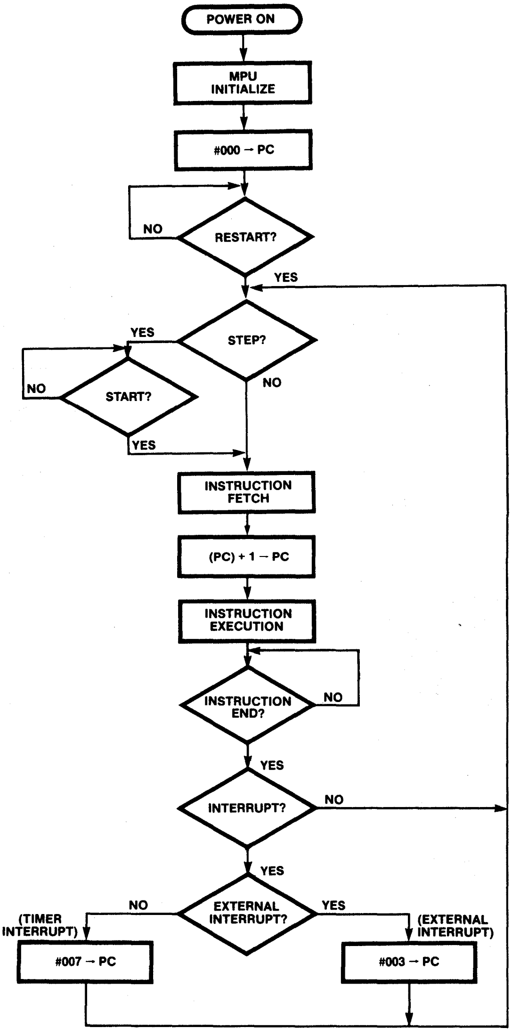
	7	6	5	4	3	2	1	0
SP - 3								
SP - 2	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
SP - 1	CY	HC	F_0	BS	PC_{11}	PC_{10}	PC_9	PC_8
SP								
SP + 1								

A Set of 2 Bytes

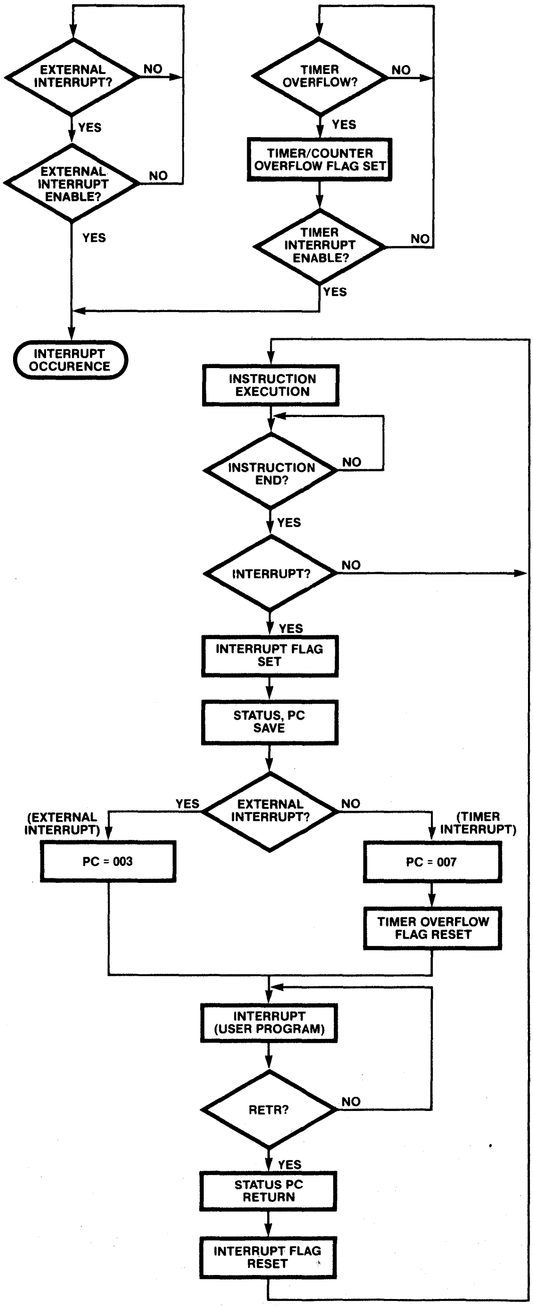
This level will be used at the next sub-routine call or interrupt.
Stack Position
SP = $00001SP_2SP_1SP_0$

RAM Address

Operation Flow Chart

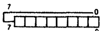
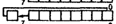
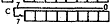
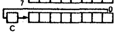


Flow Chart for Interrupt Operation



Instruction Set Summary

Accumulator

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Add register to A	ADD A,R_r	6X	1	1	*	*	—	—	$(R_r) + (A) \rightarrow (A)$
Add data memory to A	ADD A,@R_0	60	1	1	*	*	—	—	$((R_0)) + (A) \rightarrow (A)$
	ADD A,@R_1	61	1	1	*	*	—	—	$((R_1)) + (A) \rightarrow (A)$
Add immediate to A	ADD A,#data	03	2	2	*	*	—	—	data + $(A) \rightarrow (A)$
Add register with carry	ADDC A,R_r	7X	1	1	*	*	—	—	$(R_r) + (A) + (C) \rightarrow (A)$
Add data memory with carry	ADDC A,@R_0	70	1	1	*	*	—	—	$((R_0)) + (A) + (C) \rightarrow (A)$
	ADDC A,@R_1	71	1	1	*	*	—	—	$((R_1)) + (A) + (C) \rightarrow (A)$
Add immediate to A with carry	ADDC A,#data	13	2	2	*	*	—	—	data + $(A) + (C) \rightarrow (A)$
And register to A	ANL A,R_r	5X	1	1	—	—	—	—	$(R_r) \cap (A) \rightarrow (A)$
And data memory to A	ANL A,@R_0	50	1	1	—	—	—	—	$((R_0)) \cap (A) \rightarrow (A)$
	ANL A,@R_1	51	1	1	—	—	—	—	$((R_1)) \cap (A) \rightarrow (A)$
And immediate to A	ANL A,#data	53	2	2	—	—	—	—	data $\cap (A) \rightarrow (A)$
Clear A	CLR A	27	1	1	—	—	—	—	$0 \rightarrow (A)$
Complement A	CPL A	37	1	1	—	—	—	—	$(\bar{A}) \rightarrow (A)$
Decimal Adjust A	DA A	57	1	1	*	—	—	—	Note (1)
Decrement A	DEC A	07	1	1	—	—	—	—	$(A) -1 \rightarrow (A)$
Increment A	INC A	17	1	1	—	—	—	—	$(A) + 1 \rightarrow (A)$
Or register to A	ORL A,R_r	4X	1	1	—	—	—	—	$(R_r) \cup (A) \rightarrow (A)$
Or data memory to A	ORL A,@R_0	40	1	1	—	—	—	—	$((R_0)) \cup (A) \rightarrow (A)$
	ORL A,@R_1	41	1	1	—	—	—	—	$((R_1) \cup (A) \rightarrow (A)$
Or immediate to A	ORL A,#data	43	2	2	—	—	—	—	data $\cup (A) \rightarrow (A)$
Rotate A left	RL A	E7	1	1	—	—	—	—	
Rotate A left with carry	RLC A	F7	1	1	*	—	—	—	
Rotate A right	RR A	77	1	1	—	—	—	—	
Rotate A right with carry	RRC A	67	1	1	*	—	—	—	
SWAP nibbles of A	SWAP A	47	1	1	—	—	—	—	$(A_{4-7}) \rightleftarrows (A_{0-3})$
Exclusive Or register to A	XRL A,R_r	DX	1	1	—	—	—	—	$(R_r) \oplus (A) \rightarrow (A)$
Exclusive Or data memory to A	XRL A,@R_0	D0	1	1	—	—	—	—	$((R_0)) \oplus (A) \rightarrow (A)$
	XRL A,@R_1	D1	1	1	—	—	—	—	$((R_1)) \oplus (A) \rightarrow (A)$
Exclusive Or immediate to A	XRL A,#data	D3	2	2	—	—	—	—	data$\oplus (A) \rightarrow (A)$

Instruction Set Summary
(Continued)

Input/Output

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
And immediate to BUS	ANL BUS,#data	98	2	2	—	—	—	—	data ∩ (BUS) → (BUS)
P_1	ANL P_1,#data	99	2	2	—	—	—	—	data ∩ (P_1) → (P_1)
P_2	ANL P_2,#data	9A	2	2	—	—	—	—	data ∩ (P_2) → (P_2)
And A to Expander Port	ANLD P_P,A	9X	1	2	—	—	—	—	(A) ∩ (P_P) → (P_P)
Input BUS to A	INS A,BUS	08	1	2	—	—	—	—	(BUS) → (A)
Port 1 to A	IN A,P_1	09	1	2	—	—	—	—	(P_1) → (A)
Port 2 to A	IN A,P_2	0A	1	2	—	—	—	—	(P_2) → (A)
Input Expander port to A	MOVD A,P_P	0X	1	2	—	—	—	—	(P_P) → $(A)_{0-3}$ 0 → $(A)_{4-7}$
Or immediate to BUS	ORL BUS,#data	88	2	2	—	—	—	—	data ∪ (BUS) → (BUS)
P_1	ORL P_1,#data	89	2	2	—	—	—	—	data ∪ (P_1) → (P_1)
P_2	ORL P_2,#data	8A	2	2	—	—	—	—	data ∪ (P_2) → (P_2)
Or A to Expander Port	ORLD P_P,A	8X	1	2	—	—	—	—	data ∪ (P_P) → (P_P)
Output A to BUS	OUTL BUS,A	02	1	2	—	—	—	—	(A) → (BUS)
P_1	OUTL P_1,A	39	1	2	—	—	—	—	(A) → (P_1)
P_2	OUTL P_2,A	3A	1	2	—	—	—	—	(A) → (P_2)
Output A to Expander Port	MOVD P_P,A	3X	1	2	—	—	—	—	(A) → (P_P)

Data Moves

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Move register to A	MOV A,R_r	FX	1	1	—	—	—	—	(R_r) → (A)
Move data memory to A	MOV A,@R_0	F0	1	1	—	—	—	—	((R_0)) → (A)
	MOV A,@R_1	F1	1	1	—	—	—	—	((R_1)) → (A)
Move immediate to A	MOV A,#data	23	2	2	—	—	—	—	data → (A)
Move A to register	MOV R_r,A	AX	1	1	—	—	—	—	(A) → (R_r)
Move A to data memory	MOV @ R_0,A	A0	1	1	—	—	—	—	(A) → ((R_0))
	MOV @R_1,A	A1	1	1	—	—	—	—	(A) → ((R_1))
Move immediate to register	MOV R_r,#data	BX	2	2	—	—	—	—	data → (R_r)
Move immediate to data memory	MOV @R_0,#data	B0	2	2	—	—	—	—	data → ((R_0))
	MOV @R_1,#data	B1	2	2	—	—	—	—	data → ((R_1))
Move PSW to A	MOV A,PSW	C7	1	1	—	—	—	—	(PSW) → (A)
Move A to PSW	MOV PSW,A	D7	1	1	*	*	*	—	(A) → (PSW)
Move external data memory to A	MOVX A,@R_0	80	1	2	—	—	—	—	((R_0)) → (A)
	MOVX A,@R_1	81	1	2	—	—	—	—	((R_1)) → (A)
Move A to eternal data memory	MOVX @R_0,A	90	1	2	—	—	—	—	(A) → ((R_0))
	MOVX @R_1,A	91	1	2	—	—	—	—	(A) → ((R_1))
Move to A from current page	MOVP A,@A	A3	1	2	—	—	—	—	((A)) → (A)
Move to A from page 3	MOVP3 A,@A	E3	1	2	—	—	—	—	((A)) within page 3 → (A)
Exchange A and register	XCH A,R_r	2X	1	1	—	—	—	—	(R_r) ⇄ (A)
Exchange A and data memory	XCH A,@R_0	20	1	1	—	—	—	—	((R_0)) ⇄ (A)
	XCH A,@R_1	21	1	1	—	—	—	—	((R_1)) ⇄ (A)
Exchange nibble of A	XCHD A,@R_0	30	1	1	—	—	—	—	$((R0)_{0-3})$ ⇄ (A_{0-3})
and data memory	XCHD A,@R_1	31	1	1	—	—	—	—	$((R1)_{0-3})$ ⇄ (A_{0-3})

Instruction Set Summary
(Continued)

Registers

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Decrement Register	DEC R_r	CX	1	1	—	—	—	—	$(R_r) - 1 \rightarrow (R_r)$
Increment register	INC R_r	1X	1	1	—	—	—	—	$(R_r) + 1 \rightarrow (R_r)$
Increment data memory	INC @R_0	10	1	1	—	—	—	—	$((R_0)) + 1 \rightarrow ((R_0))$
	INC @R_1	11	1	1	—	—	—	—	$((R_1)) + 1 \rightarrow ((R_1))$

Timer/Counter

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Disable Timer/Counter Interrupt	DIS TCNTI	35	1	1	—	—	—	—	
Enable Timer/Counter Interrupt	EN TCNTI	25	1	1	—	—	—	—	
Read Timer/Counter	MOV A,T	42	1	1	—	—	—	—	(T) → (A)
Load Timer/Counter	MOV T,A	62	1	1	—	—	—	—	(A) → (T)
Start Timer	STRT T	55	1	1	—	—	—	—	
Start Counter	STRT CNT	45	1	1	—	—	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	—	—	

Control

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Disable external Interrupt	DIS I	15	1	1	—	—	—	—	
Enable external Interrupt	EN I	05	1	1	—	—	—	—	
Enable Clock output on T_0	ENT$_0$ CLK	75	1	1	—	—	—	—	
No Operation	NOP	00	1	1	—	—	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	—	—	0 → (BS)
Select register bank 1	SEL RB1	D5	1	1	—	—	—	—	1 → (BS)
Select memory bank 0	SEL MB0	E5	1	1	—	—	—	—	0 → (MBF)
Select memory bank 1	SEL MB1	F5	1	1	—	—	—	—	1 → (MBF)

Instruction Set Summary
(Continued)

Branch

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Decrement register and test	DJNZ R addr	EX	2	2	—	—	—	—	$(R_r) \neq 0$ Note (2)
Jump unconditional	JMP addr	%4	2	2	—	—	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	—	—	Unconditional Branch Note (3)
Jump on Carry = 1	JC addr	F6	2	2	—	—	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	—	—	(C) = 0
Jump on A zero	JZ addr	C6	2	2	—	—	—	—	(A) = 0
Jump on A not zero	JNZ addr	96	2	2	—	—	—	—	$(A) \neq 0$
Jump on T_0 = 1	JT0 addr	36	2	2	—	—	—	—	(T_0) = 1
Jump on T_0 = 0	JNT0 addr	26	2	2	—	—	—	—	(T_0) = 0
Jump on T_1 = 1	JT1 addr	56	2	2	—	—	—	—	(T_1) = 1
Jump on T_1 = 0	JNT1 addr	46	2	2	—	—	—	—	(T_1) = 0
Jump on F_0 = 1	JF0 addr	B6	2	2	—	—	—	—	$(F_0$ = 1
Jump on F_1 = 1	JF1 addr	76	2	2	—	—	—	—	(F_1) = 1
Jump on timer flag	JTF addr	16	2	2	—	—	—	—	(TF) = 1
Jump on $\overline{INT}$ = 0	JN1	86	2	2	—	—	—	—	$(\overline{INT})$ = 0
Jump on accumulator bit	JBr addr	%2	2	2	—	—	—	—	(A_r) = 1

Subroutine

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Jump to subroutine	CALL addr	%4	2	2	—	—	—	—	Note (4)
Return	RET	83	1	2	—	—	—	—	Note (5)
Return and restore status	RETR	90	1	2	*	*	*	—	Note (6)

Flags

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Clear carry	CLR C	97	1	1	Z	—	—	—	0 → (C)
Complement carry	CPL C	A7	1	1	CP	—	—	—	$(\overline{C})$ → (C)
Clear Flag 0	CLR F_0	85	1	1	—	—	Z	—	0 → (F_0)
Complement Flag 0	CPL F_0	95	1	1	—	—	CP	—	$(\overline{F_0})$ → (F_0)
Clear Flag 1	CLR F_1	A5	1	1	—	—	—	Z	0 → (F_1)
Complement Flag 1	CPL F_1	B5	1	1	—	—	—	CP	$(\overline{F_1})$ → (F_1)

Notes:
Operation Code X: Tables-1, 2   %: Table 3
Flag*: This flag is set or reset in the state after executed instruction.
Z: This flag is reset.
CP: This flag is complemented.

1) The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.

2) DJNZ R_r, addr;
$(R_r) - 1 \rightarrow (R_r)$
if $(R_r) \neq 0$ addr → $(PC_0$ to $PC_7)$
if $(R_r) = 0$ execute next instruction

3) JMPP @A
((A)) → $(PC_0$ to $PC_7)$

4) CALL addr
$(PC_0$ to $PC_7)$ → ((SP))
(SP) + 1 → (SP)
$(PC_8$ to $PC_{11})$, (MBF), $(PSW_4$ to $PSW_7)$ → ((SP))
(SP) + 1 → (SP)
A_L → $(PC_0$ to $PC_7)$
A_H → $(PC_8$ to $PC_{10})$
MBF → (PC_{11})

5) RET
(SP) - 1 → (SP)
$((SP)_0$ to $(SP)_3)$ → $((PC)_8$ to $(PC)_{11})$
(SP) - 1 → (SP)
((SP)) → $(PC_0$ to $PC_7)$

6) RETR
(SP) – 1 → (SP)
$((SP)_0$ to $(SP)_3)$ → $(PC_8$ to $PC_{11})$
$((SP)_4$ to $(SP)_7)$ → $(PSW_4$ to $PSW_7)$
(SP) – 1 → (SP)
((SP)) → $(PC_0$ to $PC_7)$

A_L: Lower 8 Bits of Address
A_H: A_8, A_9, A_{10} of Address
MBF: Memory Bank Flag

Instruction Set Summary
(Continued)

OP Code of Register Access (Table 1)

Mnemonic	Rr	R0	R1	R2	R3	R4	R5	R6	R7
INC Rr		18	19	1A	1B	1C	1D	1E	1F
XCH A,Rr		28	29	2A	2B	2C	2D	2E	2F
ORL A,Rr		48	49	4A	4B	4C	4D	4E	4F
ANL A,Rr		58	59	5A	5B	5C	5D	5E	5F
ADD A,Rr		68	69	6A	6B	6C	6D	6E	6F
ADDC A,Rr		78	79	7A	7B	7C	7D	7E	7F
MOV Rr,A		A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr,#data		B8	B9	BA	BB	BC	BD	BE	BF
DEC Rr		C8	C9	CA	CB	CC	CD	CE	CF
XRL A,Rr		D8	D9	DA	DB	DC	DD	DE	DF
DJNZ Rr,M		E8	E9	EA	EB	EC	ED	EE	EF
MOV A,Rr		F8	F9	FA	FB	FC	FD	FE	FF

7	6	5	4	3	2	1	0
					r_2	r_1	r_0

OP Code of Expander (Table 2)

Mnemonic	PP	P4	P5	P6	P7
MOVD A,P_P		0C	0D	0E	0F
MOVD P_P,A		3C	3D	3E	3F
ORLD P_P,A		8C	8D	8E	8F
ANLD P_P,A		9C	9D	9E	9F

7	6	5	4	3	2	1	0
						P_1	P_0

OP Code of JMP, CALL, JB_r (Table 3)

	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
JMP	A_H			0	0	1	0	0	A_L							
	First Byte								Second Byte							
CALL	A_H			1	0	1	0	0	A_L							
	First Byte								Second Byte							
JB_r	B_r			1	0	0	1	0	A_L							
	First Byte								Second Byte							

A_L; Address A_7 to A_0
A_H; Address A_{10}, A_9, A_8
B_r; r-th Bit on Accumulator

Instruction Codes

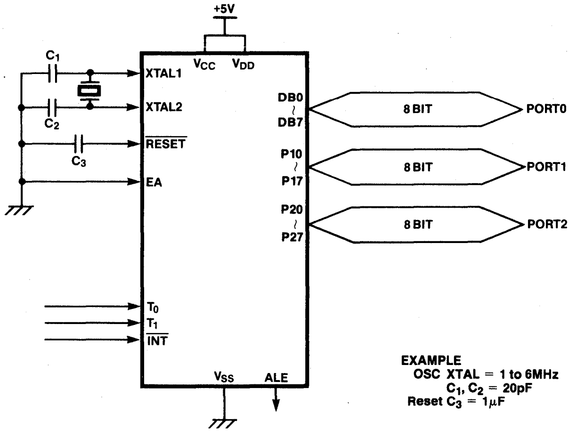
H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	HALT	OUTL BSU,A	◥ ADD A, #	◥ JMP 0 x x	EN 1		DEC A	◤ INS A,BUS	◤ IN A,P1	◤ IN A,P2		◤ MOVD A,P4	◤ MOVD A,P5	◤ MOVD A,P6	◤ MOVD A,P7
1	INC @R0	INC @R1	◥ JB0 addr	◥ ADDC A #	◥ CALL 0 x x	DIS 1	◥ JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A,@R0	XCH A,@R1		◥ MOV A,#	◥ JMP 1 x x	EN TCNT1	◥ JNT0 addr	CLR A	XCH A,R0	XCH A,R1	XCH A,R2	XCH A,R3	XCH A,R4	XCH A,R5	XCH A,R6	XCH A,R7
3	XCHD A,@R0	XCHD A,@R1	◥ JB1 addr		◥ CALL 1 x x	DIS TCNT1	◥ JT0 addr	CPL A		◤ OUTL P1,A	◤ OUTL P2,A		◤ MOVD P4,A	◤ MOVD P5,A	◤ MOVD P6,A	◤ MOVD P7,A
4	ORL A,@R0	ORL A,@R1	MOV A,T	◥ ORL A,#	◥ JMP 2 x x	STRT CNT	◥ JNT1 addr	SWAP A	ORL A,R0	ORL A,R1	ORL A,R2	ORL A,R3	ORL A,R4	ORL A,R5	ORL A,R6	ORL A,R7
5	ANL A,@R0	ANL A,@R1	◥ JB2 addr	◥ ANL A,#	◥ CALL 2 x x	STRT T	◥ JT1 addr	DA A	ANL A,R0	ANL A,R1	ANL A,R2	ANL A,R3	ANL A,R4	ANL A,R5	ANL A,R6	ANL A,R7
6	ADD A,@R0	ADD A,@R1	MOV T,A		◥ JMP 3 x x	STOP TCNT		RRC A	ADD A,R0	ADD A,R1	ADD A,R2	ADD A,R3	ADD A,R4	ADD A,R5	ADD A,R6	ADD A,R7
7	ADDC A,@R0	ADDC A,@R1	◥ JB3 addr		◥ CALL 3 x x	ENT0 CLK	◥ JF1 addr	RR A	ADDC A,R0	ADDC A,R1	ADDC A,R2	ADDC A,R3	ADDC A,R4	ADDC A,R5	ADDC A,R6	ADDC A,R7
8	◤ MOVX A,@R0	◤ MOVX A,@R1		◤ RET	◥ JMP 4 x x	CLR F0	◥ JN1 addr		◥ ORL BUS,#	◥ ORL P1,#	◥ ORL P2,#		◤ ORLD P4,A	◤ ORLD P5,A	◤ ORLD P6,A	◤ ORLD P7,A
9	◤ MOVX @R0,A	◤ MOVX @R1,A	◥ JB4 addr	◤ RETR	◥ CALL 4 x x	CPL F0	◥ JNZ addr	CLR C	◥ ANL BUS,#	◥ ANL P1. #	◥ ANL P2. #		◤ ANLD P4,A	◤ ANLD P5,A	◤ ANLD P6,A	◤ ANLD P7,A
A	MOV @R0,A	MOV @R1,A		◤ MOVP A,@A	◥ JMP 5 x x	CLR F1		CPL C	MOV R0,A	MOV R1,A	MOV R2,A	MOV R3,A	MOV R4,A	MOV R5,A	MOV R6,A	MOV R7,A
B	◥ MOV @R0,#	◥ MOV @R1,#	◥ JB5 addr	◤ JMPP @A	◥ CALL 5 x x	CPL F1	◥ JF0 addr		◥ MOV R0#	◥ MOV R1#	◥ MOV R2#	◥ MOV R3#	◥ MOV R4#	◥ MOV R5#	◥ MOV R6#	◥ MOV R7#
C					◥ JMP 6 x x	SEL RB0	◥ JZ addr	MOV A,PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A,@R0	XRL A,@R1	◥ JB6 addr	◥ XRL A#	◥ CALL 6 x x	SEL RB1		MOV PSW,A	XRL A,R0	XRL A,R1	XRL A,R2	XRL A,R3	XRL A,R4	XRL A,R5	XRL A,R6	XRL A,R7
E				◤ MOVP3 A,@A	◥ JMP 7 x x	SEL MB0	◥ JNC addr	RL A	◥ DJNZ R0,M	◥ DJNZ R1,M	◥ DJNZ R2,M	◥ DJNZ R3,M	◥ DJNZ R4,M	◥ DJNZ R5,M	◥ DJNZ R6,M	◥ DJNZ R7,M
F	MOV A,@R0	MOV A,@R1	◥ JB7 addr		◥ CALL 7 x x	SEL MB1	◥ JC addr	RLC A	MOV A,R0	MOV A,R1	MOV A,R2	MOV A,R3	MOV A,R4	MOV A,R5	MOV A,R6	MOV A,R7

#: Immediate data
H; Higher 4 bits
L; Lower 4 bits

□	Single-byte, Single-cycle Instruction
◤	Single-byte, Two-cycle Instruction
◥	Two-byte, Two-cycle Instruction

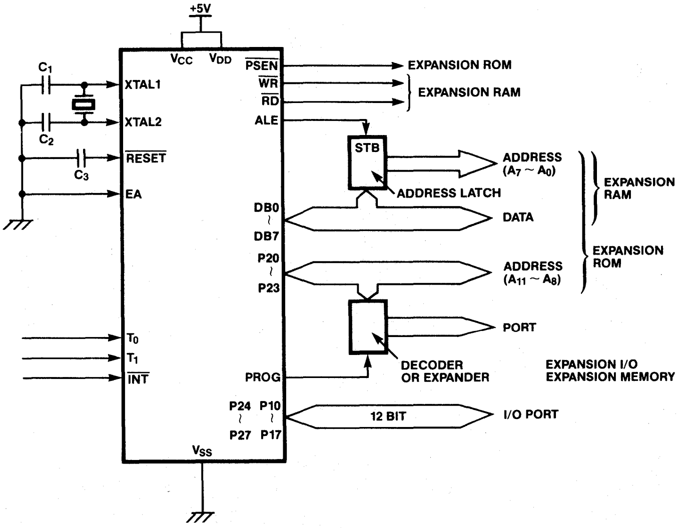
Typical Applications

(1) Stand Alone System



EXAMPLE
OSC XTAL = 1 to 6MHz
C_1, C_2 = 20pF
Reset C_3 = 1μF

(2) Expanded System



Absolute Maximum Ratings†

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

†Permanent device damage may occur if the ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliabilty.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	+5.0 ±10%	V
	V_{SS}	0	V
Operating Temperature	T_A	0 to +70	°C

DC Characteristics

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

			Test	Value		
Parameter		**Symbol**	**Conditions**	**Min.**	**Max.**	**Unit**
Input Low Voltage	All Except XTAL1, 2, $\overline{\text{RESET}}$	V_{IL}		-0.3	0.8	V
	XTAL1,2, $\overline{\text{RESET}}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All Except XTAL1, 2, $\overline{\text{RESET}}$	V_{IH}		2.0	V_{CC}	V
	XTAL1,2, $\overline{\text{RESET}}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	BUS	V_{OL}	I_{OL} = 2.0mA		0.45	V
	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE	V_{OL1}	I_{OL} = 2.0mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
	Other outputs	V_{OL3}	I_{OL} = 1.6mA		0.45	V
Output High Voltage	BUS	V_{OH}	I_{OH} = −400μA	2.4		V
	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE	V_{OH1}	I_{OH} = −100μA	2.4		V
	Other Outputs	V_{OH2}	I_{OH} = −50μA	2.4		V
Input Leakage Current	T_1, $\overline{\text{INT}}$	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$		±10	μA
	P10-P17, P20-P27 EA, $\overline{\text{SS}}$	I_{IL1}	$V_{SS} + 0.45V \leq V_{IN} \leq V_{CC}$		-500	μA
Output Leakage Current	BUS, T_0 (High-Impedance)	I_{OL}	$V_{SS} + 0.45V \leq V_{IN} \leq V_{CC}$		±10	μA
V_{DD} Supply Current	MBL8049/39N/E	I_{DD}			30	mA
	MBL8049/39H				50	mA
Total Supply Current	MBL8049/39N/E	I_{DD} + I_{CC}			150	mA
	MBL8049/39H				170	mA

AC Characteristics*

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V

		H-Version		E-Version		N-Version		
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
ALE Pulse Width	t_{LL}	150		260		410		ns
Address Setup Time (to ALE↓)	t_{AL}	70		140		230		ns
Address Hold Time (from ALE↓)	t_{LA}	50		80		120		ns
Control Pulse Width (RD, WR)	t_{CC1}	480		730		1050		ns
Control Pulse Width (PSEN)	t_{CC2}	350		550		800		ns
Data Setup Time (before WR↑)	t_{DW}	390		610		880		ns
Data Hold Time (after WR↑)**	t_{WD}	40		80		120		ns
Data Hold Time (after RD↑, PSEN↑)	t_{DR}	0	110	0	160	0	220	ns
Data Delayed Time (RD↓ to data in)	t_{RD1}		350		550		800	ns
Data Delayed Time (PSEN↓ to data in)	t_{RD2}		210		360		550	ns
Address Setup Time (to WR↓)	t_{AW}	310		480		680		ns
Address Setup Time (RD, to data in)	t_{AD1}		760		1130		1590	ns
Address Setup Time (PSEN, to data in)	t_{AD2}		480		750		1090	ns
Address Floating Time (to RD↓, WR↓)	t_{AFC1}	140		210		290		ns
Address Floating Time (to PSEN↓)	t_{AFC2}	10		20		40		ns
RD, WR Output Time (from ALE↓)	t_{LAFC1}	200		300		420		ns
PSEN Output Time (from ALE↓)	t_{LAFC2}	60		110		170		ns
ALE Output Time (from RD↑, WR↑, PROG↑)	t_{CA1}	50		80		120		ns
ALE Output Time (from PSEN↑)	t_{CA2}	320		460		620		ns
Port Control Setup Before Falling Edge of PROG Time	t_{CP}	100		170		250		ns
Port Control Hold After Falling Edge of PROG Time	t_{PC}	160		300		460		ns
PROG Time P2 Input Must Be Valid	t_{PR}		700		1000		1380	ns
P2 Input Data Hold Time (after PROG↑)	t_{PF}	0	140	0	190	0	250	ns
Output Data Setup Time (to PROG↑)	t_{DP}	400		600		850		ns
Output Data Hold Time (after PROG↑)	t_{PD}	90		130		200		ns
PROG Pulse Width	t_{PP}	700		1060		1500		ns
Port2 I/O Data Setup Time (to ALE↑)	t_{PL}	160		300		460		ns
Port2 I/O Data Hold Time (from ALE↑)	t_{LP}	40		60		80		ns
Port Data Output Time (from ALE↓)	t_{PV}		510		660		850	ns
Cycle Time***	t_{CY}	1.36		1.875		2.5		µs
T_0 Output Cycle Time	t_{OPRR}	270		370		500		ns

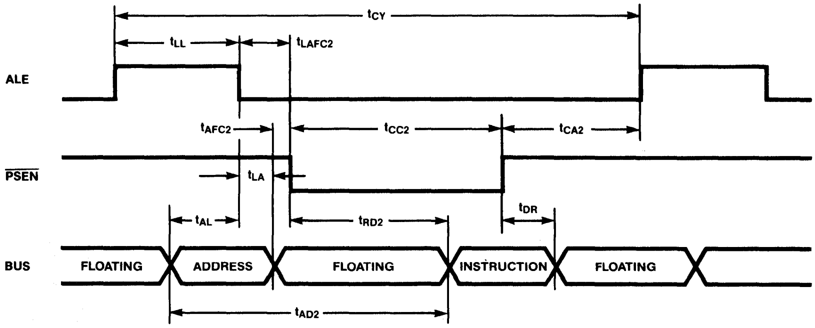
*: 6MHz XTAL (N-Version), 8MHz XTAL (E-Version), 11MHz XTAL (H-Version) Load Conditions: BUS: C_L = 150pF; Other Outputs C_L = 80pF.

**: Load Conditions C_L = 20pF, High Impedance

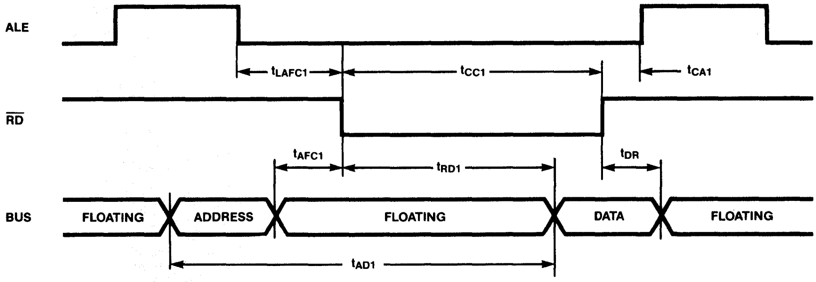
***: t_{CY} = 2.5µs (6MHz XTAL N-Version), t_{CY} = 1.875µs (8MHz XTAL E-Version), t_{CY} = 1.36µs (11MHz XTAL H-Version)

Timing Diagram

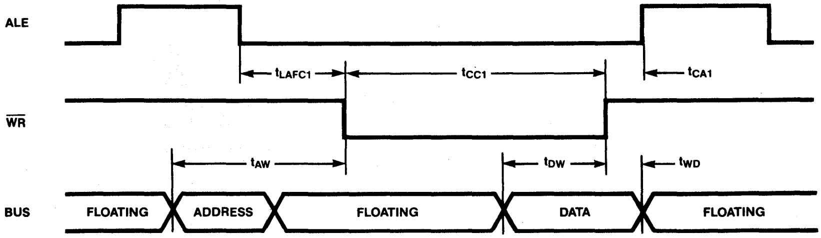
Instruction Fetch From External Program Memory



Read From External Data Memory

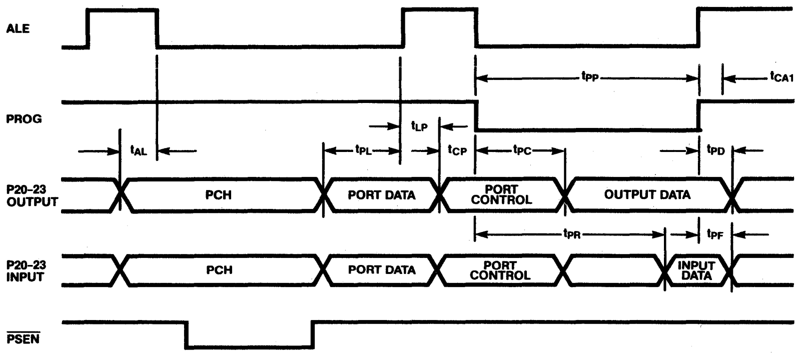


Write To External Data Memory

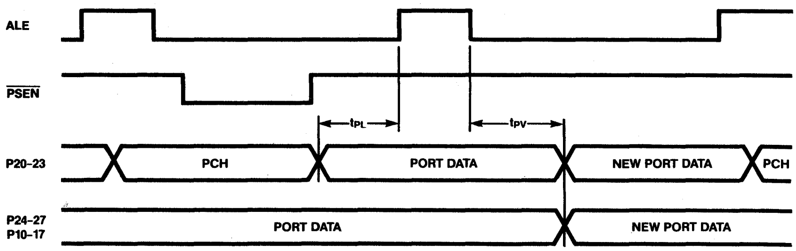


Timing Diagram
(Continued)

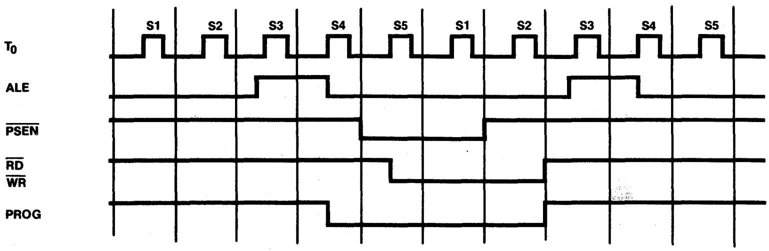
P20–23 Input/Output For Use Of External Program Memory And Expander I/O Port



Port 1/Port 2 Outputs



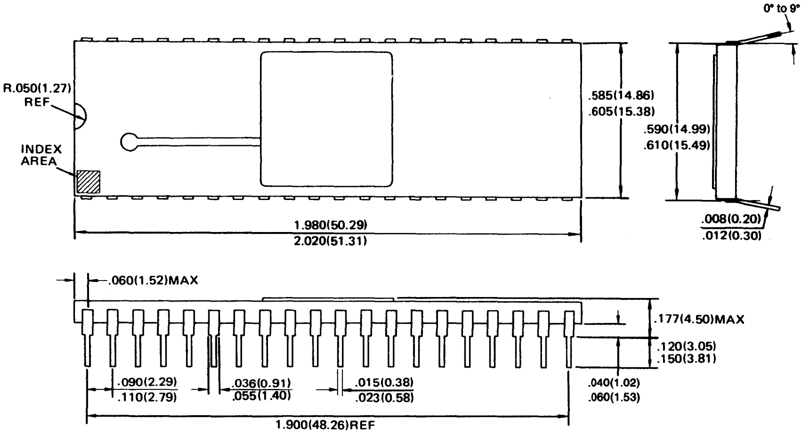
Clock Outputs



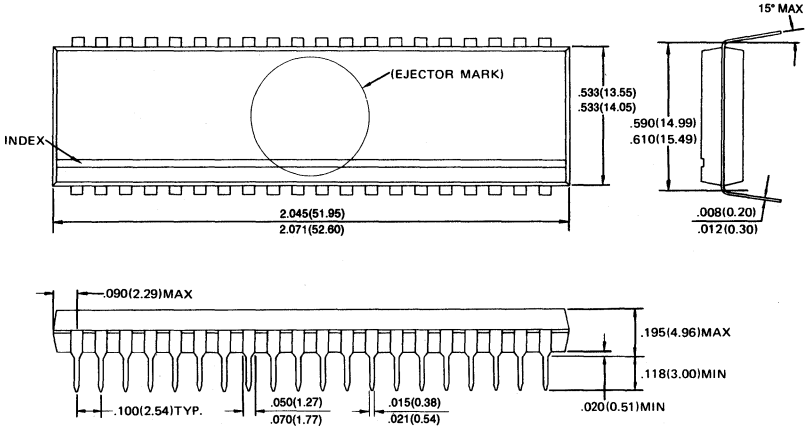
Package Dimensions

Dimensions in inches
(millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)

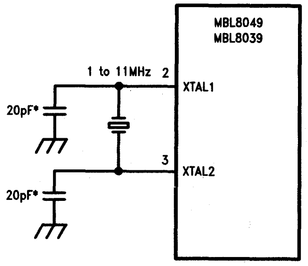


40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



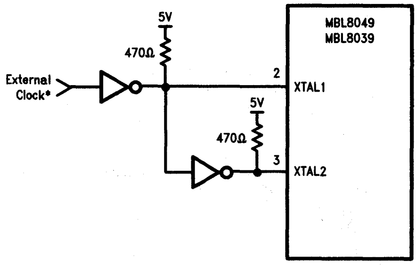
Oscillation Circuits

Crystal Oscillator



* Including stray capacitances

External Clock Drive



*Both high and low times should be more than 35% of the cycle time, and rise and fall times should be less than 20 ns.

FUJITSU

NMOS SINGLE-CHIP 8-BIT MICROCOMPUTER

MBL8749H/N

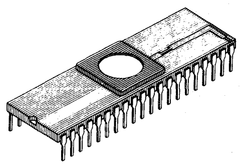
October 1986
Edition 1.0

DESCRIPTION

The Fujitsu MBL8749 is an 8-bit single-chip microcomputer that uses a 2K × 8-bit Electrically Programmable Read Only Memory (EPROM) for program memory. The EPROM can be erased by using an ultraviolet (UV) light source; thus, program memory for the MBL8749 can be changed as often as required. Also included in the MBL8749 are: 256 × 8-bit static RAM, 27 I/O lines, an 8-bit timer/counter, and a clock generator. The device can be ordered in either of two speed versions: N-version for operation at 6MHz and the H-version for operation at 11MHz. For either frequency, the operating temperature range is 0°C to 70°C.

The MBL8749 is fabricated using an N-channel, 2-layer polysilicon-gate MOS process. The MBL8749 is housed in a 40-pin ceramic windowed DIP and requires a single +5-volt supply for basic operation and a 21-volt supply for programming the EPROM.

The MBL8749 is well suited for applications such as system evaluation, system prototyping, and low-volume production work.

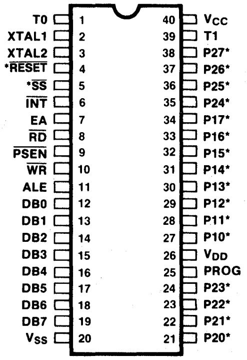


Ceramic DIP
(DIP-40C-A04)

FEATURES

- 2K × 8-bit program memory (EPROM)
- 256 × 8-bit data memory (static RAM)
- 8-level stack
- 8 pairs of working registers
- 27 I/O lines: Two 8-bit I/O ports, one 8-bit data bus, two test inputs, and one interrupt input
- 8-bit timer/counter
- On-chip clock generator (or external clock source)
- Single-level interrupt
- External program mode
- Single-step operation
- RAM retention in low-power standby mode
- ALU functions: Addition, decimal adjust addition, and logic operations
- Instruction cycle time: 1.36μs for H-version (11MHz) and 2.5μs for N-Version (6MHz)
- Powerful instruction set: 96 instructions (230 op-codes). All instructions complete in one or two instruction cycles with 70% being of the single-byte type
- Some instructions can process ROM contents as data

PIN ASSIGNMENT



*These pins have on-chip pullups.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Features (Cont)

- I/O port data can be handled directly in logic operations
- Binary coded decimal (BCD) data can be handled
- Single +5V power supply
- 0°C to 70°C operating temperature range
- N-channel, 2-layer polysilicon-gate MOS process
- 40-pin ceramic DIP package
- Compatible with Intel 8749
- Replaceable with Fujitsu MBL8049/48 and Intel 8049/8048

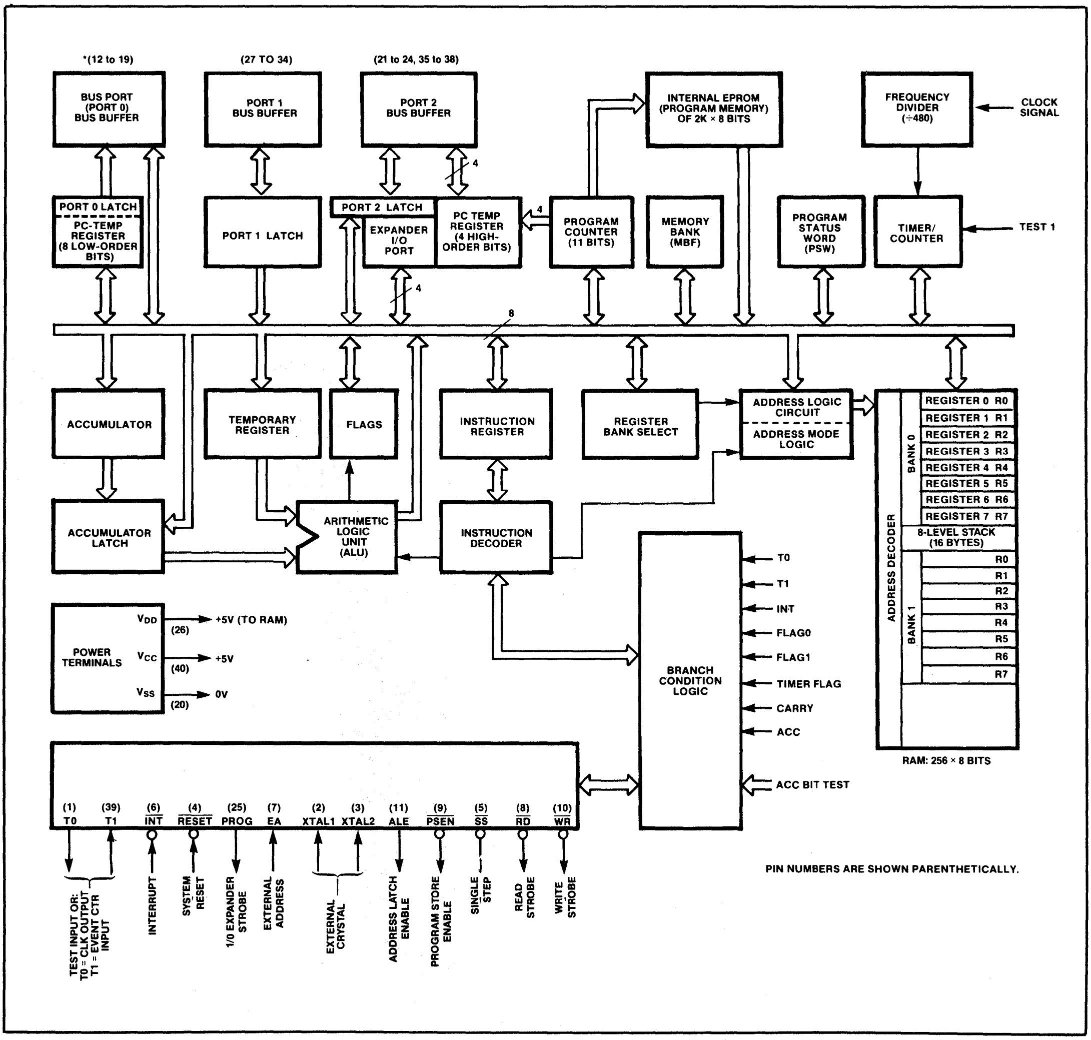
PIN DESCRIPTIONS

Pin No.	Symbol	Function
1	T0	Test Input 0: Input for conditional branch instructions JT0 and JNT0. Clock output when an ENT0 CLK instruction is executed.
2	XTAL1	Connections for external crystal. If an external TTL clock source is used, proper interface circuits are required between the clock source and XTAL1/XTAL2, since these inputs are not TTL compatible. Generally an open-collector drive and a squarewave pulse shaper will suffice.
3	XTAL2	
4	$\overline{\text{RESET}}$	When active low, resets MPU and initializes processor as follows: • Clears program counter and stack pointer. • Selects memory bank 0 and register bank 0. • Disables T0 output. • Places bus in the high-impedance state and ports 1 and 2 in the input mode. • Disables interrupts and stops the timer/counter. • Clears timer and user flags F0 and F1.
5	$\overline{\text{SS}}$	Input for single step operation. When $\overline{\text{SS}}$ is pulsed and goes low, the MPU executes the current instruction and stops. The next instruction address is fetched and placed in the four low-order bits of port 2 and the bus port. When $\overline{\text{SS}}$ is pulsed high, the single-step operation is repeated so long as $\overline{\text{SS}}$ is repetitively driven low, high, low, high, etc. When $\overline{\text{SS}}$ is permanently set to the high state, normal operation resumes.
6	$\overline{\text{INT}}$	When active low, initiates an external interrupt request. The $\overline{\text{INT}}$ input signal must remain low until the interrupt request is latched. This pin also serves as an input for a conditional branch instruction (JNI).
7	EA	All program memory accesses are directed to an external program memory when EA is high. At this time, the Program Store Enable ($\overline{\text{PSEN}}$) strobe is also output to external program memory.
8	$\overline{\text{RD}}$	The read strobe ($\overline{\text{RD}}$) is active (Low) when data is read from the bus port. This strobe output signal enables data onto the bus port from external devices including external data memory. The $\overline{\text{RD}}$ strobe is output when either an INS A,BUS or MOVX A @Rr instruction is executed.
9	$\overline{\text{PSEN}}$	The Program Store Enable ($\overline{\text{PSEN}}$) strobe is output to external program memory each time the memory is accessed. This external program memory enable signal is generated in the instruction fetch cycle and the instruction is fetched on the rising edge of this signal.

PIN DESCRIPTIONS (continued)

Pin No.	Designator	Function
10	$\overline{\text{WR}}$	When active low, the write ($\overline{\text{WR}}$) strobe enables data to pass from the data bus port to external I/O devices, including external memory. The $\overline{\text{WR}}$ strobe is active when executing an "OUTL BUS, A" or a "MOVX@Rr, A" instruction.
11	ALE	Clock signal (ALE) output generated in each instruction cycle. This signal is used for external synchronization with the MPU. The address signal to the external program memory or external data memory is latched at the falling edge of the ALE signal. This signal is output except during single-step operations.
12 to 19	DB0 to DB7	A bidirectional I/O port called the bus port (Port 0). Strobe signals $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are output on data input or output. This port can also be used for latch output or as the interface to the external program memory or external data memory. When the external program memory is accessed, the address signal (the low-order 8 bits) is output synchronously with the ALE signal and the instruction is fetched from the specified address synchronously with the $\overline{\text{PSEN}}$ signal. When external data memory is accessed, the address signal is output synchronously with the ALE signal and data is read or written synchronously with the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal. When data is not being input or output, the bus port is in a high-impedance state.
20	V_{SS}	Ground terminal (GND)
21 to 24	P20 to P23	A pseudo-bidirectional I/O port. All bits must be set to 1 before the port is used for input. The four low-order bits (P20 to P23) function as the interface to the I/O expander (MBL8243) or serve as an output for the address signal (four high-order bits) when the external program memory is used. The port data is lost on access to the I/O expander and retained when the external program memory is accessed; it is recovered when no address data is output.
35 to 38	P24 to P27	
25	PROG	Strobe signal (PROG) output to the I/O expander. This signal is also used as an input strobe to program the internal EPROM.
26	V_{DD}	Power supply to the internal RAM and EPROM.
27 to 34	P10 to P17	An 8-bit pseudo-bidirectional I/O port. All bits must be set high before the port is used for input.
39	T1	Input for conditional branch instructions JT1 and JNT1; also serves as event input when event counter mode is selected. The event counter is incremented on the falling edge of this input signal.
40	V_{CC}	+5-volt power supply.

BLOCK DIAGRAM

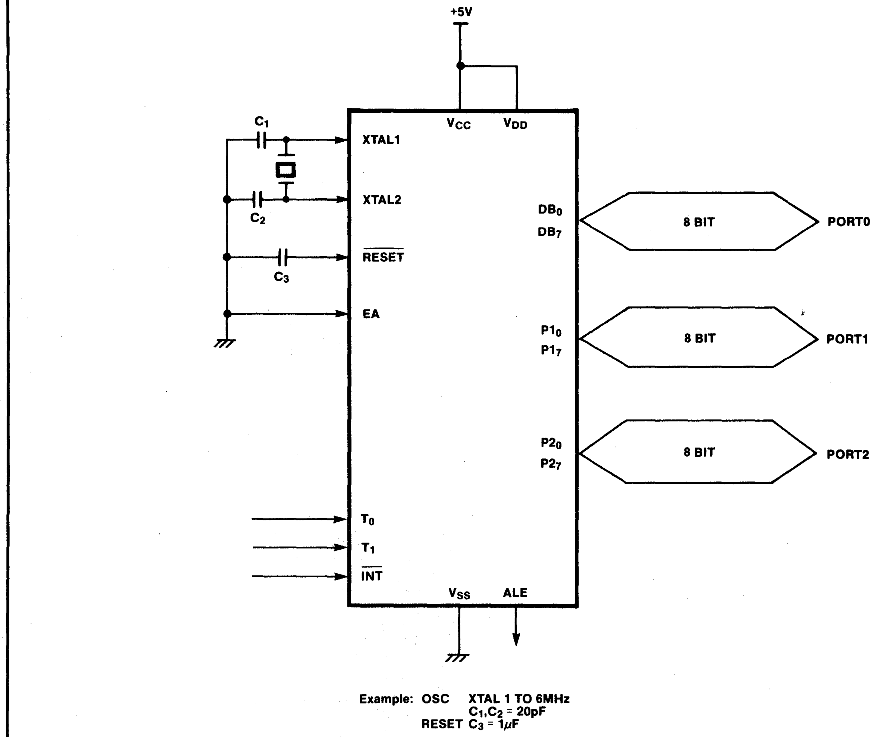


PIN NUMBERS ARE SHOWN PARENTHETICALLY.

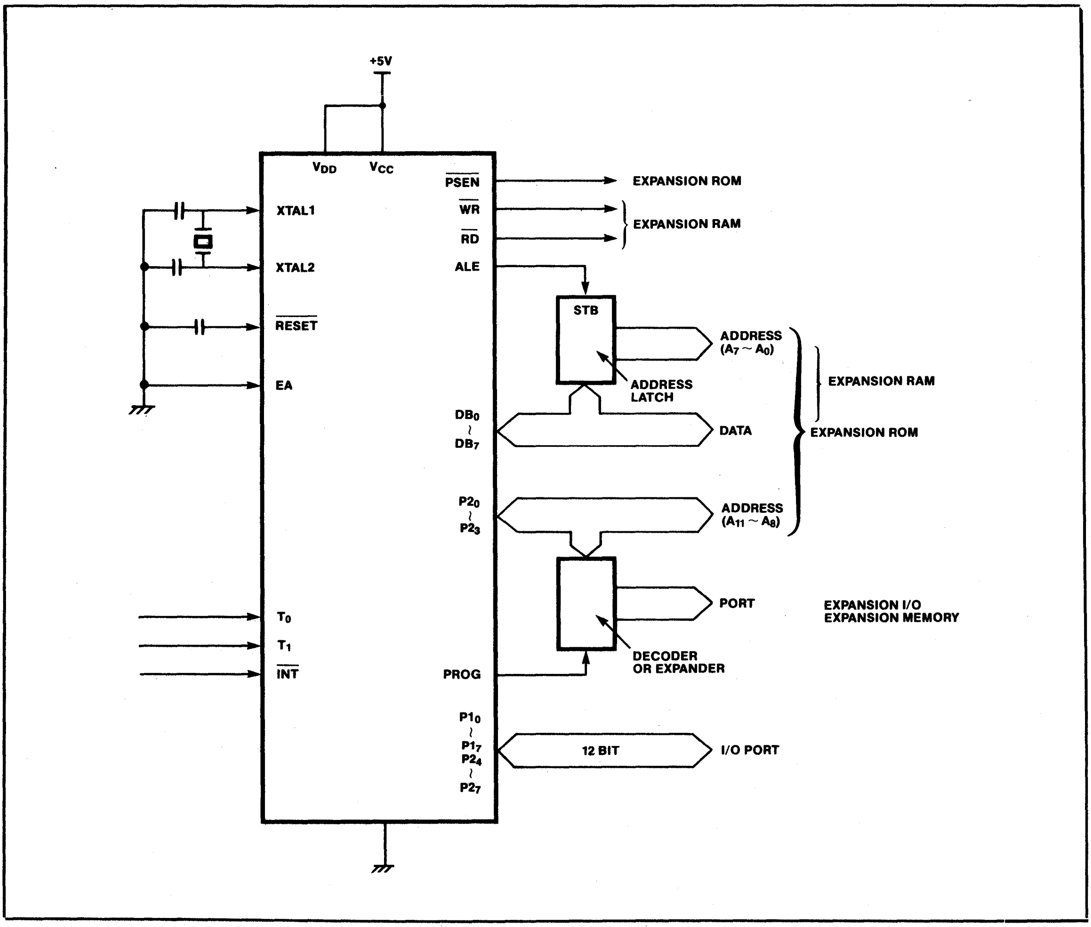
FUNCTIONAL DESCRIPTION

Block Name	Function
Clock Generation Circuitry	Using a capacitor, a crystal, or an external clock source, the on-chip clock generator produces a master clock within a frequency range of 1-to-6 MHz for N-version parts and 11 MHz for H-version parts. The master clock frequency is divided by three to produce a state clock signal which, in turn, is divided by five to produce a cycle clock signal. The cycle clock is used for all internal operations and is available on the ALE pin. When an ENT0 CLK instruction is executed, the state clock is output on the T0 pin.
I/O Port	Three bidirectional or quasi-bidirectional 8-bit I/O ports and three input terminals are provided for signal inputs and outputs. Port 0 (Bus Port) and the lower 4 bits of Port 2 shown in the Block Diagram are used for access to external memories or I/O expanders.
On-chip ROM and RAM	Programs are stored in the on-chip EPROM (2K bytes). Also, the contents of ROM can be used as data for some instructions. The on-chip RAM (256 bytes) is used for general-purpose registers, the 16-byte stack, and scratch-pad memory (refer to RAM memory map that follows). ROM can be expanded up to 4K bytes by memory addons and by switching memory banks; RAM can be expanded an additional 256 bytes by simple addons. A standalone system and one designed for memory addons are shown following the "Functional Description."
Program Counter	The program counter is a 12-bit register that holds the address in program memory from which the next instruction is to be fetched and is incremented by every execution of an instruction.
Instruction Register	The Instruction Register is an 8-bit register that holds the next instruction to be executed.
Instruction Decoder	The Instruction Decoder decodes the instruction stored in the Instruction Register and generates various control signals for both internal circuits and external peripherals.
Arithmetic Logic Unit (ALU)	Various operations such as addition, subtraction, comparison, etc. are executed in the ALU. Operations to be executed are determined from the instruction decoding process.
Interval Timer/ Event Counter	The Interval Timer/Event Counter is an 8-bit register under instruction control. The interval timer mode or event counter mode can be designated by instruction execution, as well. This register is not initialized by the RESET signal. In the interval timer mode, the register counts up the frequency signal which is generated by dividing the cycle clock frequency by 32. When the source frequency is 6MHz, this enables the register to count a time interval of up to 20.48ms with a resolution of 80μs. In this mode, the register generates an interrupt vector address (Address 07), if the register overflows from $(FF)_{16}$ to $(00)_{16}$. Even if an oveflow occurs, the register continues to count up. This enables the register to count a longer time interval by using proper software. In the event counter mode, the register counts on the falling edge of the T_1 input. In this mode, the features of the register other than the counting trigger are the same as those in the interval timer mode. (Note. The T_1 input pulse has a minimum width of 500-nanoseconds and, at 6MHz, a minimum cycle time of 7.5-microseconds.)
Status Register Including Stack Pointer	The Status Register is an 8-bit register which consists of four bits for flags, three bits for the Stack Pointer, and an unused bit. The flag bits indicate the status of the MPU. The Stack Pointer specifies an address in the stack to be used in the next subroutine call or interrupt.

STANDALONE SYSTEM



EXPANDED SYSTEM



RESIDENT DATA MEMORY MAP (RAM)

Address (Hex)						
0	R_0 Register 0					Register Bank 0
1	R_1 Register 1					
2	R_2 Register 2					
3	R_3 Register 3					
4	R_4 Register 4					
5	R_5 Register 5					
6	R_6 Register 6					
7	R_7 Register 7					
8						Stack Register (16 Bytes) (8 Level Stack)
9						
.						
.	PC_L					
.	CY	HC	F0	BS	PC_H	
.						
.						
16						
17						
18	R_0 Register 0					Register Bank 1
19	R_1 Register 1					
1A	R_2 Register 2					
1B	R_3 Register 3					
1C	R_4 Register 4					
1D	R_5 Register 5					
1E	R_6 Register 6					
1F	R_7 Register 7					
20	Working Area (224 Bytes)					
21						
22						
.						
.						
.						
FD						
FE						
FF						

STATUS REGISTER

The Status Register is an 8-bit register that holds the Program Status Word (PSW). The register is configured as shown. The upper four bits are used for flags to indicate the status of the MPU. When a subroutine call or an interrupt occurs, the contents of the program counter are transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining bit is unused.

7	6	5	4	3	2	1	0
CY	HC	F_0	BS	Blank (Unused Bit)	SP_2	SP_1	SP_0
Flags					Stack Pointer		

FLAGS

CY (Carry): When an overflow occurs in the Accumulator during an ALU operation, this bit is set to "1".

HC (Half Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator as a result of an addition, this bit is set to "1".

F_0 (User Flag): This flag is instruction-controlled by the user.

BS (Bank Select): This flag is used for register-bank identification. When BS = 0, Register Bank 0 is selected; when BS = 1, Register Bank 1 is selected.

STACK REGISTER

The Stack Register uses 16 bytes of memory in the on-chip RAM. The Stack Register consists of eight levels, that is, a stack level consists of two bytes as shown.

	7	6	5	4	3	2	1	0
SP-3								
SP-2	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
SP-1	CY	HC	F_0	BS	PC_{11}	PC_{10}	PC_9	PC_8
SP								
SP+1								

} A Set of 2 Bytes

← This level will be used at the next sub-routine call or interrupt.

↑
RAM Address

Stack Position
$SP = 00001SP_2SP_1SP_0$

SP (Stack Pointer): In the above figure, "SP" indicates an address in the stack pointer that will be used for the next subroutine call or interrupt. "SP" is given as an 8-bit code from the lower three bits of the status register as follows:

$$SP = 00001\underbrace{SP_2SP_1SP_0}$$

→Status Register bits 0 to 2.

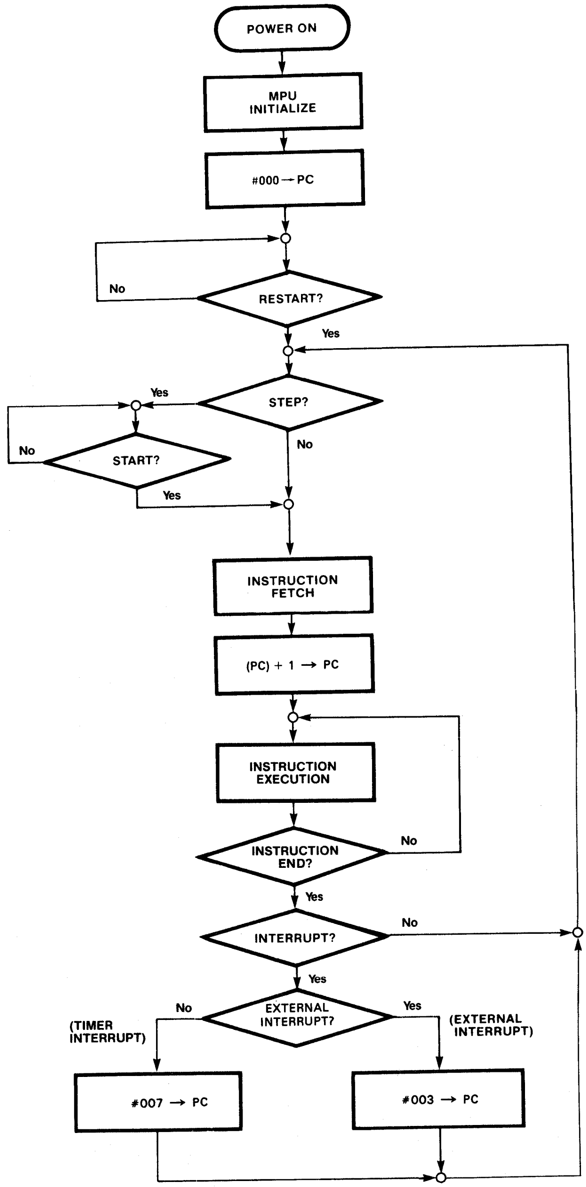
PC_n (Program Counter): In the above figure, "PC_n" indicates the content of the n^{th} bit in the Program Counter.

INTERRUPT OPERATION

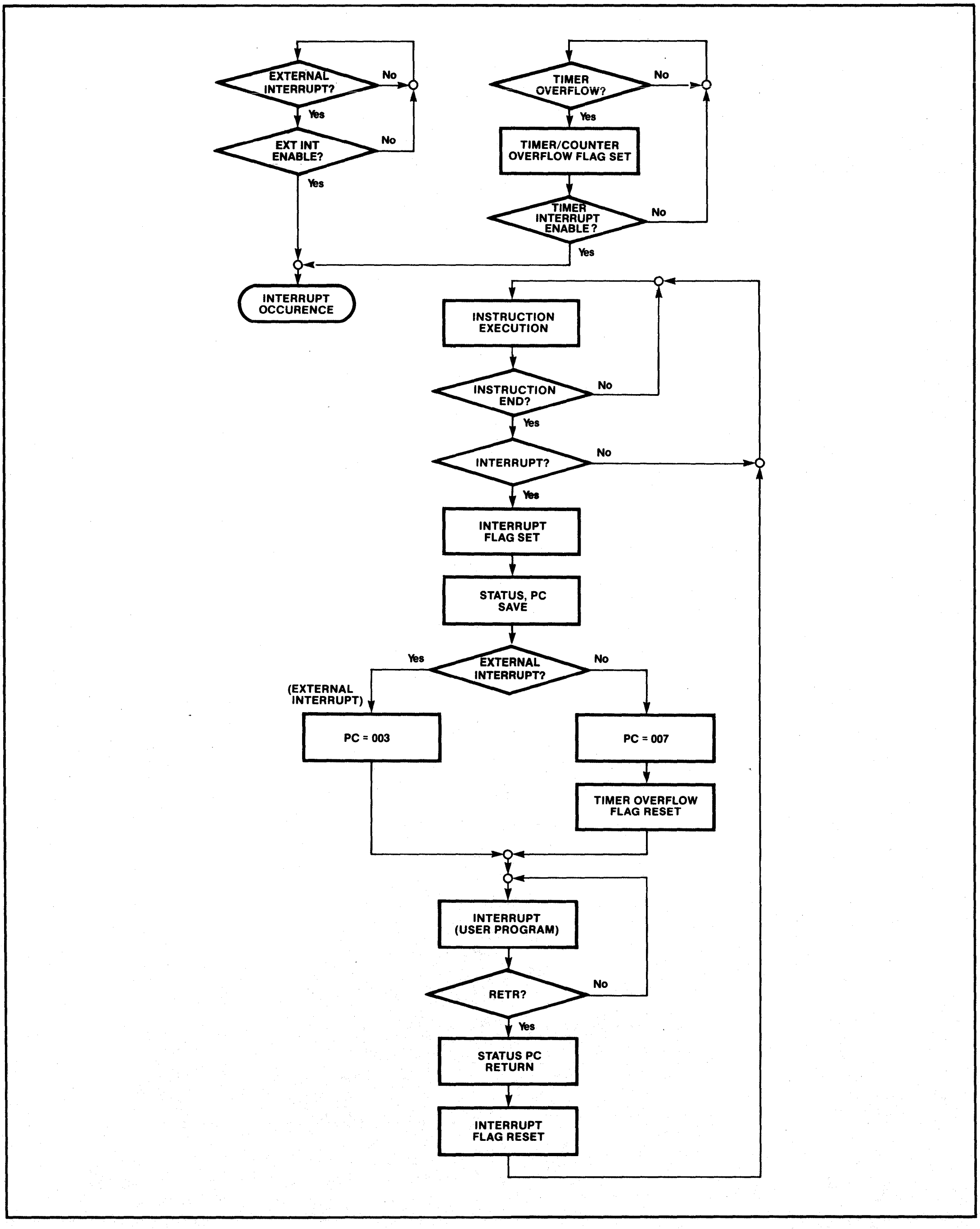
There are two modes for interrupt operation: external interrupts and timer/counter interrupts. A timer/counter interrupt is masked by an external input; thus, external interrupts always have priority. The basic operation for both types of interrupts are the same, except a timer/counter interrupt is initiated on overflow of the counter. Subsequent flowcharts provide operational detail for the interrupt procedures that follow.

- Upon executing the current instruction, the interrupt flag is set.
- Contents of the Status Register and Program Counter are saved in the stack.
- For an external interrupt, the Program Counter is loaded with address 003; for a timer/counter interrupt, address 007 is loaded in the PC.
- After the interrupt is serviced, a RETR instruction is executed which restores the pre-interrupt contents of the Status Register and Program Counter.
- The interrupt flag is reset.

OPERATION FLOWCHART



INTERRUPT FLOWCHART



PROGRAMMING AND VERIFYING EPROM MEMORY

Internal program memory of the MBL8749 is a 2K × 8-bit EPROM that can be electrically written into, and erased by using an ultraviolet (UV) light source. Pin functions for programming and verifying the EPROM are repeated here for convenience of the user.

Pin Descriptions

Name	Function
XTAL1, XTAL2	Clock signal (1 to 3MHz) input
$\overline{\text{RESET}}$	Initialize and address-latch signal input: Address data input to the data bus is internally latched on the rising edge of the $\overline{\text{RESET}}$ signal.
T0	Program mode is selected when this signal is low and verify mode is selected when it is high.
EA	Program and verify enable signal input: Either mode is enabled when 18 volts is applied to this pin.
BUS (D7 to D0)	Address and data inputs in the program mode and data output in the verify mode.
V_{DD}	Power supply
PROG	Input pulses for programming

PROGRAMMING PROCEDURE

Step 1: Initialization
V_{CC} and V_{DD} = 5V
Clock signal = 1 to 3MHz (Internal or external clock)
$\overline{\text{RESET}}$ = 0V
T0, EA = 5V
BUS and PROG pins floating.

Step 2: T0 = 0V
Select program mode.

Step 3: EA = 18V
Enable program or verify mode

Step 4: Input address signals.
BUS = 8 low-order bits
P22 to P20: = 3 high-order bits

Step 5: $\overline{\text{RESET}}$ = 5V
Internally latch the address inputs.

Step 6: Input write data to BUS.

Step 7: V_{DD} = 21V
Turn on programming power supply.

Step 8: Apply 0 volts to the PROG pin and then apply a programming pulse of 18 volts for 50 ms. Again apply 0 volts to the pin and then let it float.

Step 9: V_{DD} = 5V, BUS floating
Turn off programming power supply (V_{DD} = 21V → 5V), and let BUS float.

Step 10: T0 = 5V
Select verify mode.

Step 11: Externally read BUS data to verify data.

Step 12: T0 = 0V
Terminate verify mode and select program mode.

Step 13: $\overline{\text{RESET}}$ = 0V
Go to the next step when data has been written. If data is not valid, repeat procedures, beginning with Step 4.

Step 14: EA = 5V
Disable program or verify mode.

ERASING EPROM

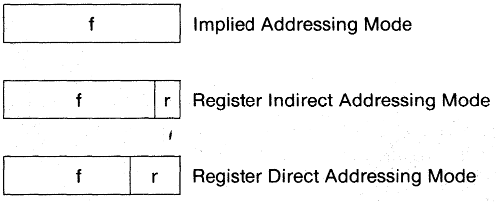
Data written into the EPROM can be erased by applying ultraviolet light rays with a wavelength of 2537 angstroms. With UV light source directly above the transparent lid at a distance of 2-to-3 centimeters, the time for complete erasure is between 15-and-20 minutes for most commercial lamps. The recommended amount of UV radiation is 10Wsec/cm^2; the luminous intensity on the package surface is designed to be approximately 12000μW/cm^2.

If the package surface is soiled by grease, adhesives, or other light inhibitors, the erasing time will increase. Before attempting to erase data, it is recommended that surface be cleaned with alcohol or some other detergent that will not damage the package.

INSTRUCTIONS

All instructions are one or two bytes and also execute in either one or two cycles. Addresing modes are classified as direct, expanded, indirect, immediate and implied. Single-byte and double-byte instruction formats are as follows:

1-Byte Instruction:


f
Implied Addressing Mode
f
r
Register Indirect Addressing Mode
f
r
Register Direct Addressing Mode

2-Byte Instruction:

f	OP

Immediate Addressing Mode

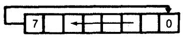
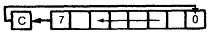
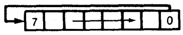
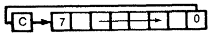
A_H	f	A_L

Expanded Addressing Mode

f: Instruction Operation Set
r: Register Set
OP: Operand Data
A_H, A_L: Operand Address

Table 1. Instruction Set Summary

Accumulator and Memory Instructions

Operation	Mnemonic	OP code	Byte	Cycle	Flag				Notes
					C	AC	F0	F1	
Add register to A	ADD A, Rr	6X	1	1	*	*	—	—	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	*	*	—	—	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	*	*	—	—	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	*	*	—	—	(A) ← (A) + data
Add register to A with carry	ADDC A, Rr	7X	1	1	*	*	—	—	(A) ← (A) + (Rr) + (C)
Add data memory to A with carry	ADDC A, @R0	70	1	1	*	*	—	—	(A) ← (A) + ((R0)) + (C)
	ADDC A, @R1	71	1	1	*	*	—	—	(A) ← (A) + ((R1)) + (C)
Add immediate to A with Carry	ADDC A, #data	13	2	2	*	*	—	—	(A) ← (A) + data + (C)
And register to A	ANL A, Rr	5X	1	1	—	—	—	—	(A) ← (A) ∩ (Rr)
And data memory to A	ANL A, @R0	50	1	1	—	—	—	—	(A) ← (A) ∩ ((R0))
	ANL A, @R1	51	1	1	—	—	—	—	(A) ← (A) ∩ ((R1))
And immediate to A	ANL A, #data	53	2	2	—	—	—	—	(A) ← (A) ∩ data
Clear A	CLR A	27	1	1	—	—	—	—	(A) ← 0
Complement A	CPL A	37	1	1	—	—	—	—	(A) ← $(\overline{A})$
Decimal Adjust A	DA A	57	1	1	*	—	—	—	Note 1
Decrement A	DEC A	07	1	1	—	—	—	—	(A) ← (A) - 1
Increment A	INC A	17	1	1	—	—	—	—	(A) ← (A) + 1
Or register to A	ORL A, Rr	4X	1	1	—	—	—	—	(A) ← (A) ∪ (Rr)
Or data memory to A	ORL A, @R0	40	1	1	—	—	—	—	(A) ← (A) ∪ ((R0))
	ORL A, @R1	41	1	1	—	—	—	—	(A) ← (A) ∪ ((R1))
Or immediate to A	ORL A, #data	43	2	2	—	—	—	—	(A) ← (A) ∪ data
Rotate A left	RL A	E7	1	1	—	—	—	—	
Rotate A left through carry	RLC A	F7	1	1	*	—	—	—	
Rotate A right	RR A	77	1	1	—	—	—	—	
Rotate A right through carry	RRC A	67	1	1	*	—	—	—	
SWAP nibles of A	SWAP A	47	1	1	—	—	—	—	(A7~4) ⇄ (A3~0)
Exclusive or register to A	XRL A, Rr	DX	1	1	—	—	—	—	(A) ← (A) ⊕ (Rr)
Exclusive or data memory to A	XRL A, @R0	D0	1	1	—	—	—	—	(A) ← (A) ⊕ ((R0))
	XRL A, @R1	D1	1	1	—	—	—	—	(A) ← (A) ⊕ ((R1))
Exclusive or immediate to A	XRL A, #data	D3	2	2	—	—	—	—	(A) ← (A) ⊕ data

Operation	Mnemonic	OP code	Byte	Cycle	Flag				Notes
					C	AC	F0	F1	
Input/Output Instructions (Cont)									
And immediate to BUS	ANL BUS, #data	98	2	2	—	—	—	—	(BUS) ← (BUS) ∩ data
P1	ANL P1, #data	99	2	2	—	—	—	—	(P1) ← (P1) ∩ data
P2	ANL P2, #data	9A	2	2	—	—	—	—	(P2) ← (P2) ∩ data
And A to Expander Port	ANLD P_p, A	9X	1	2	—	—	—	—	(P_p) ← (P_p) ∩ (A3~0)
Input BUS to A	INS A, BUS	08	1	2	—	—	—	—	(A) ← (BUS)
Port 1 to A	IN A, P1	09	1	2	—	—	—	—	(A) ← (P1)
Port 2 to A	IN A, P2	0A	1	2	—	—	—	—	(A) ← (P2)
Input Expander Port to A	MOVD A, P_p	0X	1	2	—	—	—	—	(A3~0) ← (P_p) (A7~0) ← 0
Or immediate to BUS	ORL BUS, #data	88	2	2	—	—	—	—	(BUS) ← (BUS) ∪ data
P1	ORL P1, #data	89	2	2	—	—	—	—	(P1) ← (P1) ∪ data
P2	ORL P2, #data	8A	2	2	—	—	—	—	(P2) ← (P2) ∪ data
Or A to Expander Port	ORLD P_p, A	8X	1	2	—	—	—	—	(P_p) ← (P_p) ∪ (A3~0)
Output A to BUS	OUTL BUS, A	02	1	2	—	—	—	—	(BUS) ← (A)
P1	OUTL P1, A	39	1	2	—	—	—	—	(P1) ← (A)
P2	OUTL P2, A	3A	1	2	—	—	—	—	(P2) ← (A)
Output A to Expander Port	MOVD P_p, A	3X	1	2	—	—	—	—	(P_p) ← (A3~0)
Data Move Instructions									
Move register to A	MOV A, Rr	FX	1	1	—	—	—	—	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	—	—	—	—	(A) ← ((R0))
	MOV A, @R1	F1	1	1	—	—	—	—	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	—	—	—	—	(A) ← data
Move A to register	MOV Rr, A	AX	1	1	—	—	—	—	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	—	—	—	—	((R0)) ← (A)
	MOV @R1, A	A1	1	1	—	—	—	—	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX	2	2	—	—	—	—	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	—	—	—	—	((R0)) ← data
	MOV @R1, #data	B1	2	2	—	—	—	—	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	—	—	—	—	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*	*	*	—	(PSW) ← (A)
Move external data memory to A	MOVX A, @R0	80	1	2	—	—	—	—	(A) ← ((R0))
	MOVX A, @R1	81	1	2	—	—	—	—	(A) ← ((R1))
Move A to external data memory	MOVX @R0, A	90	1	2	—	—	—	—	((R0)) ← (A)
	MOVX @R1, A	91	1	2	—	—	—	—	((R1)) ← (A)
Move to A from current page	MOVP A, @A	A3	1	2	—	—	—	—	(A) ← ((A))
Move to A from Page 3	MOVP3A, @A	E3	1	2	—	—	—	—	(A) ← ((A)) within page 3
Exchange A and register	XCH A, Rr	2X	1	1	—	—	—	—	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	—	—	—	—	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	—	—	—	—	(A) ⇄ ((R1))
Exchange nibble of A and data memory	XCHD A, @R0	30	1	1	—	—	—	—	(A3~0) ⇄ ((R0)3~0)
	XCHD A, @R1	31	1	1	—	—	—	—	(A3~0) ⇄ ((R1)3~0)
Register Instructions									
Decrement register	DEC Rr	CX	1	1	—	—	—	—	(Rr) ← (Rr) - 1
Increment register	INC Rr	1X	1	1	—	—	—	—	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	—	—	—	—	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	—	—	—	—	((R1)) ← ((R1)) + 1

Timer/Counter Instructions (Cont)

Operation	Mnemonic	OP code	Byte	Cycle	Flag				Notes
					C	AC	F0	F1	
Disable Timer/Counter Interrupt	DIS TCNTI	35	1	1	—	—	—	—	
Enable Timer/Counter Interrupt	EN TCNTI	25	1	1	—	—	—	—	
Read Timer/Counter	MOV A, T	42	1	1	—	—	—	—	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	—	—	—	—	(T) ← (A)
Start Time	STRT T	55	1	1	—	—	—	—	
Start Counter	STRT CNT	45	1	1	—	—	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	—	—	
Control Instructions									
Disable external interrupt	DIS I	15	1	1	—	—	—	—	
Enable external interrupt	EN I	05	1	1	—	—	—	—	
Enable Clock output on T0	ENT0 CLK	75	1	1	—	—	—	—	
No Operation	NOP	00	1	1	—	—	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	—	—	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	—	—	—	—	(BS) ← 1
Select memory bank 0	SEL MB0	E5	1	1	—	—	—	—	(MBF) ← 0
Select memory bank 1	SEL MB1	F5	1	1	—	—	—	—	(MBF) ← 1
Branch and Jump Instructions									
Decrement register and test	DJNZ Rr, addr	EX	2	2	—	—	—	—	(Rr) ≠ 0 (Note 4)
Jump unconditional	JMP addr	%4	2	2	—	—	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	—	—	Unconditional Branch (Note 5)
Jump on Carry = 1	JC addr	F6	2	2	—	—	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	—	—	(C) = 0
Jump on A zero	JZ addr	C6	2	2	—	—	—	—	(A) = 0
Jump on A not zero	JNZ addr	96	2	2	—	—	—	—	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	—	—	—	—	(T0) = 1
Jump on T0 = 0	JNT0 addr	26	2	2	—	—	—	—	(T0) = 0
Jump on T1 = 1	JT1 addr	56	2	2	—	—	—	—	(T1) = 1
Jump on T1 = 0	JNT1 addr	46	2	2	—	—	—	—	(T1) = 0
Jump on F0 = 1	JF0 addr	B6	2	2	—	—	—	—	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	—	—	—	—	(F1) = 1
Jump on timer flag	JTF addr	16	2	2	—	—	—	—	(TF) = 1
Jump on $\overline{\text{INT}}$ = 0	JNI addr	86	2	2	—	—	—	—	($\overline{\text{INT}}$) = 0
Jump on accumulator bit	JBr addr	%2	2	2	—	—	—	—	(Ar) = 1
Subroutine Instructions									
Jump to subroutine	CALL addr	%4	2	2	—	—	—	—	(Note 6)
Return	RET	83	1	2	—	—	—	—	(Note 7)
Return and restore status	RETR	93	1	2	*	*	*	—	(Note 8)
Flag Instructions									
Clear carry	CLR C	97	1	1	Z	—	—	—	(C) ← 0
Complement carry	CPL C	A7	1	1	CP	—	—	—	(C) ← ($\overline{\text{C}}$)
Clear Flag 0	CLR F0	85	1	1	—	—	Z	—	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	—	—	CP	—	(F0) ← ($\overline{\text{F0}}$)
Clear Flag 1	CLR F1	A5	1	1	—	—	—	Z	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	—	—	—	CP	(F1) ← ($\overline{\text{F1}}$)

Table 2. OP Codes for Register Access

Mnemonic Rr	R0	R1	R2	R3	R4	R5	R6	R7
INC Rr	18	19	1A	1B	1C	1D	1E	1F
XCH A, Rr	28	29	2A	2B	2C	2D	2E	2F
ORL A, Rr	48	49	4A	4B	4C	4D	4E	4F
ANL A, Rr	58	59	5A	5B	5C	5D	5E	5F
ADD A, Rr	68	69	6A	6B	6C	6D	6E	6F
ADDC A, Rr	78	79	7A	7B	7C	7D	7E	7F
MOV Rr, A	A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data	B8	B9	BA	BB	BC	BD	BE	BF
DEC Rr	C8	C9	CA	CB	CC	CD	CE	CF
XRL A, Rr	D8	D9	DA	DB	DC	DD	DE	DF
DJNZ Rr, M	E8	E9	EA	EB	EC	ED	EE	EF
MOV A, Rr	F8	F9	FA	FB	FC	FD	FE	FF

7	6	5	4	3	2	1	0
					R2	R1	R0

Table 3. OP Codes for Expander

Mnemonic Pp	P4	P3	P2	P1
MOVD A, Pp	0C	0D	0E	0F
MOVD Pp, A	3C	3D	3E	3F
ORLD Pp, A	8C	8D	8E	8F
ANLD Pp, A	9C	9D	9E	9F

7	6	5	4	3	2	1	0
						P1	P0

Table 4. OP Codes for JMP, CALL, and JBr Instructions

	7 6 5	4	3	2	1	0	7 6 5 4 3 2 1 0
JMP	AH	0	0	1	0	0	AL
	First Byte						Second Byte
CALL	AH	1	0	1	0	0	AL
	First Byte						Second Byte
JBr	Br	1	0	0	1	0	AL
	First Byte						Second Byte

A_L : Address A_7 to A_0
A_H: Address A_{10}, A_9, A_8
B_r : r^{th} Bit on Accumulator

Notes:

1. Refer to Tables 1 and 2 for OP Code suffixes of "X"; refer to Table 3 for OP Code prefixes of "%".
2. Flag status:
   * = Set, or reset flag bit to the state it was in before instruction execution.
   z = Reset flag bit.
   CP = Complement flag bit.
3. The accumulator value is adjusted to form BCD digits following the binary addition of BCD number.
4. DJNZ R_r addr: $(R_r) - 1 \rightarrow (R_r)$
   if $(R_r) \neq 0$, add $\rightarrow$ (PC_0 to PC_7).
   if $(R_r) = 0$, execute next instruction.
5. JMPP @A: ((A)) → (PC_0 to PC_7)
6. CALL addr
   (PC_0 to PC_7) → ((SP))
   (SP) + 1 → (SP)
   (PC_8 to PC_{11}), (MBF), (PSW_4 to PSW_7) → ((SP))
   (SP) + 1 → (SP)
   A_L → (PC_0 to PC_7)
   A_H → (PC_8 to PC_{10})
   MBF → (PC_{11})
7. RET
   (SP) - 1 → (SP)
   ($(SP)_0$ to $(SP)_3$) → $(PC)_8$ to $(PC)_{11}$)
   (SP) - 1 → (SP)
   ((SP)) → (PC_0 to PC_7)
8. RETR
   (SP) - 1 → (SP)
   (($SP)_0$ to $(SP)_3$ → (PC_8 to PC_{11})
   (($SP)_4$ to $(SP)_7$ → (PSW_4 to PSW_7)
   (SP) - 1 → (SP)
   ((SP)) → (PC_0 to PC_7)
   A_L : Lower 8 Bits of Address
   A_H : A_8, A_9, A_{10} of Address
   MBF: Memory Bank Flag

INSTRUCTION CODES

L H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		◤ OUT (BSU, A)	◥ ADD A, #	◥ JMP 0 x x	EN 1		DEC A	◤ INS (A, BUS)	◤ IN A, P1	◤ IN A, P2		◤ MOVD A, P4	◤ MOVD A, P5	◤ MOVD A, P6	◤ MOVD A, P7
1	INC @R0	INC @R1	◥ JB0 addr	◥ ADDC A, #	◥ CALL 0 x x	DIS 1	◥ JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A, @R0	XCH A, @R1		◥ MOV A, #	◥ JMP 1 x x	EN TCNT1	◥ JNT0 addr	CLR A	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
3	XCHD A, @R0	XCHD A, @R1	◥ JB1 addr		◥ CALL 1 x x	DIS TCNT1	◥ JT0 addr	CPL A		◤ OUTL P1, A	◤ OUTL P2, A		◤ MOVD P4, A	◤ MOVD P5, A	◤ MOVD P6, A	◤ MOVD P7, A
4	ORL A, @R0	ORL A, @R1	MOV A, T	◥ ORL A, #	◥ JMP 2 x x	STRT CNT	◥ JNT1 addr	SWAP A	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	OPL A, R6	ORL A, R7
5	ANL A, @R0	ANL A, @R1	◥ JB2 addr	◥ ANL A, #	◥ CALL 2 x x	STRT T	◥ JT1 addr	DA A	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6	ADD A, @R0	ADD A, @R1	MOV T, A		◥ JMP 3 x x	STOP TCNT		RRC A	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
7	ADDC A, @R0	ADDC A, @R1	◥ JB3 addr		◥ CALL 3 x x	ENT0 CLK	◥ JF1 addr	RR A	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
8	◤ MOVX (A, @ R0)	◤ MOVX (A, @ R1)		◤ RET	◥ JMP 4 x x	CLR F0	◥ JNI addr		ORL (BUS, #)	◥ ORL P1, #	◥ ORL P2, #		◤ ORLD P4, A	◤ ORLD P5, A	◤ ORLD P6, A	◤ ORLD P7, A
9	◤ MOVX @R0, A	◤ MOVX @R1, A	◥ JB4 addr	◤ RETR	◥ CALL 4 x x	CPL F0	◥ JNZ addr	CLR C	ANL (BUS, #)	◥ ANL P1, #	◥ ANL P2, #		◤ ANLD P4, A	◤ ANLD P5, A	◤ ANLD P6, A	◤ ANLD P7, A
A	MOV @R0, A	MOV @R1, A		◤ MOVP A, @A	◥ JMP 5 x x	CLR F1		CPL C	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A
B	◥ MOV @R0, #	◥ MOV @R1, #	◥ JB5 addr	◤ JMPP @A	◥ CALL 5 x x	CPL F1	◥ JF0 addr		◥ MOV R0, #	◥ MOV R1, #	◥ MOV R2, #	◥ MOV R3, #	◥ MOV R4, #	◥ MOV R5, #	◥ MOV R6, #	◥ MOV R7, #
C					◥ JMP 6 x x	SEL RB0	◥ JZ addr	MOV A, PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A, @R0	XRL A, @R1	◥ JB6 addr	◥ XRL A, #	◥ CALL 6 x x	SEL RB1	◥ JNIBF addr	MOV PSW, A	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
E				◤ MOVP3 A.@A	◥ JMP 7 x x	SEL MB0	◥ JNC addr	RL A	◥ DJNZ R0, M	◥ DJNZ R1, M	◥ DJNZ R2, M	◥ DJNZ R3, M	◥ DJNZ R4, M	◥ DJNZ R5, M	◥ DJNZ R6, addr	◥ DJNZ R7, M
F	MOV A, @R0	MOV A, @R1	◥ JB7 addr		◥ CALL 7 x x	SEL MB1	◥ JC addr	RLC A	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7

Legend:

#	Immediate data
□	= 1 Byte, 1 Cycle Instruction
◤	= 1 Byte, 2 Cycle Instruction
◥	= 2 Byte, 2 Cycle Instruction

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}, V_{DD}	$V_{SS} - 0.3$ to $V_{SS} + 7$	V
Input Voltage	V_{IN}	$V_{SS} - 0.3$ to $V_{SS} + 7$	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}, V_{DD}	4.5	5.0	5.5	V
	V_{SS}		0		V
Operating Temperature	T_A	0		+70	°C

DC CHARACTERISTICS (T_A = 0°C to +70°C, $V_{CC} = V_{DD}$ = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Applicable Pin/Device	Value		Unit	Test Conditions
			Min	Max		
Input Low Voltage	V_{IL}	All Except XTAL1, XTAL2, $\overline{\text{RESET}}$	-0.3	0.8	V	
	V_{IL1}	XTAL1, XTAL2, $\overline{\text{RESET}}$	-0.3	0.6	V	
Input High Voltage	V_{IH}	All Except XTAL1, XTAL2, $\overline{\text{RESET}}$	2.0	V_{CC}	V	
	V_{IH1}	XTAL1, XTAL2, $\overline{\text{RESET}}$	3.8	V_{CC}	V	
Output Low Voltage	V_{OL}	BUS		0.45	V	I_{OL} = 2.0mA
	V_{OL1}	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE		0.45	V	I_{OL} = 2.0mA
	V_{OL2}	PROG		0.45	V	I_{OL} = 1.0mA
	V_{OL3}	All Other Outputs		0.45	V	I_{OL} = 1.6mA
Output High Voltage	V_{OH}	BUS	2.4		V	I_{OH} = –400μA
	V_{OH1}	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE	2.4		V	I_{OH} = –100μA
	V_{OH2}	All Other Outputs	2.4		V	I_{OH} = -50μA
Input Leakage Current	I_{LI}	T1, $\overline{\text{INT}}$		±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
	I_{LI1}	P10-P17, P20-P27, EA, $\overline{\text{SS}}$		-500	μA	$V_{SS} + 0.45V \leq V_{IN} \leq V_{CC}$
Output Leakage Current	I_{LO}	BUS, T0		±10	μA	$V_{SS} + 0.45V \leq V_{IN} \leq V_{CC}$, In High-Z state
V_{DD} Supply Current	I_{DD}	V_{DD}		50	mA	
Total Supply Current	$I_{CC} + I_{DD}$	V_{CC}, V_{DD}		170	mA	

DC CHARACTERISTICS (Programming Mode)

(T_A = 25 ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21 ±0.5V or 5V ±5%)

Parameter	Symbol	Value		Unit
		Min	Max	
V_{DD} Program Voltage High Level	V_{DDH}	20.5	21.5	V
V_{DD} Program Voltage Low Level	V_{DDL}	4.75	5.25	
PROG Program Voltage High Level	V_{PH}	17.5	18.5	V
PROG Program Voltage Low Level	V_{PL}	—	0.2	
EA Program/Verify Voltage High Level	V_{EAH}	17.5	18.5	V
EA Program/Verify Voltage Low Level	V_{EAL}	—	5.25	
V_{DD} High Voltage Supply Current	I_{DD}	—	30.0	mA
PROG High Voltage Supply Current	I_{PROG}	—	16.0	
EA High Voltage Supply Current	I_{EA}	—	1.0	

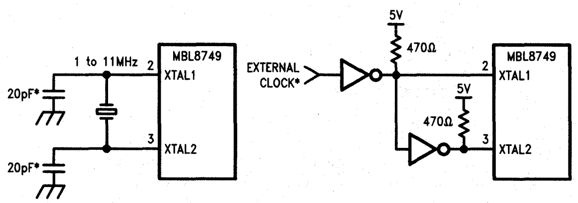
Notes:

1. High Level Voltage (V_{DDH}, V_{PH}) should not be applied to V_{DD} and PROG pins unless V_{CC} = 5V ±5% and EA = 18V ±0.5V.
2. V_{DD}, PROG, and EA should not exceed the above specified range, including overshoot and undershoot.

Oscillator Circuits

Crystal Oscillator

External Clock Drive



*Including stray capacitances

*Both high and low times should be more than 35% of the cycle time, and the rise and fall times should be less than 20ns.

AC CHARACTERISTICS (T_A = 0°C to +70°C, $V_{CC} = V_{DD}$ = +5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Value (MBL8749H)		Value (MBL8749N)		Unit	Test Conditons
		Min	Max	Min	Max		
ALE Pulse Width	t_{LL}	150		410		ns	Note 1
Address Setup Time (to ALE↓)	t_{AL}	70		230		ns	
Address Hold Time (from ALE↓)	t_{LA}	50		120		ns	
$\overline{RD}$ & $\overline{WR}$ Pulse Width	t_{CC1}	480		1050		ns	
$\overline{PSEN}$ Pulse Width	t_{CC2}	350		800		ns	
Data Setup Time (to $\overline{WR}$↑)	t_{DW}	390		880		ns	
Data Hold Time (from $\overline{WR}$↑)	t_{WD}	40		120		ns	Note 2
Data Hold Time (from $\overline{RD}$↑, $\overline{PSEN}$↑)	t_{DR}	0	110	0	220	ns	Note 1
Data Delay Time (from $\overline{RD}$↓)	t_{RD1}		350		800	ns	
Data Delay Time (from $\overline{PSEN}$↓)	t_{RD2}		210		550	ns	
Address Setup Time (to $\overline{WR}$↓)	t_{AW}	310		680		ns	
Data Delay Time ($\overline{RD}$)	t_{AD1}		760		1590	ns	
Data Delay Time ($\overline{PSEN}$)	t_{AD2}		480		1090	ns	
Address Floating Time (to $\overline{RD}$↓, $\overline{WR}$↓)	t_{AFC1}	140		290		ns	
Address Floating Time (to $\overline{PSEN}$↓)	t_{AFC2}	10		40		ns	
$\overline{RD}$ & $\overline{WR}$ Output Delay Time (from ALE↓)	t_{LAFC1}	200		420		ns	
PSEN Output Delay Time (from ALE↓)	t_{LAFC2}	60		170		ns	
ALE Delay Time (from $\overline{RD}$↑, $\overline{WR}$↑, PROG↑)	t_{CA1}	50		120		ns	
ALE Delay Time (from $\overline{PSEN}$↑)	t_{CA2}	320		620		ns	
Port Control Setup Time (to PROG↓)	t_{CP}	100		250		ns	
Port Control Hold Time (from PROG↓)	t_{PC}	160		460		ns	
Port 2 Input Data Delay Time (from PROG↓)	t_{PR}		700		1380	ns	
Port 2 Input Data Hold Time (from PROG↑)	t_{PF}	0	140	0	250	ns	
Output Data Setup Time (to PROG↑)	t_{DP}	400		850		ns	
Output Data Hold Time (from PROG↑)	t_{PD}	90		200		ns	
PROG Pulse Width	t_{PP}	700		1500		ns	
Port 2 I/O Data Setup Time (to ALE↑)	t_{PL}	160		460		ns	
Port 2 I/O Data Hold Time (from ALE↑)	t_{LP}	40		80		ns	
Port Data Output Time (from ALE↓)	t_{PV}		510		850	ns	
Cycle Time	t_{CY}	1.36		2.5		µs	
T0 Output Frequency	t_{OPRR}	270		500		ns	

Notes:
1. Load Conditions: BUS C_L = 150pF, Other Outputs C_L = 80pF, 1 TTL
2. Load Conditions C_L = 20pF, High impedance

↓ Falling edge
↑ Rising edge

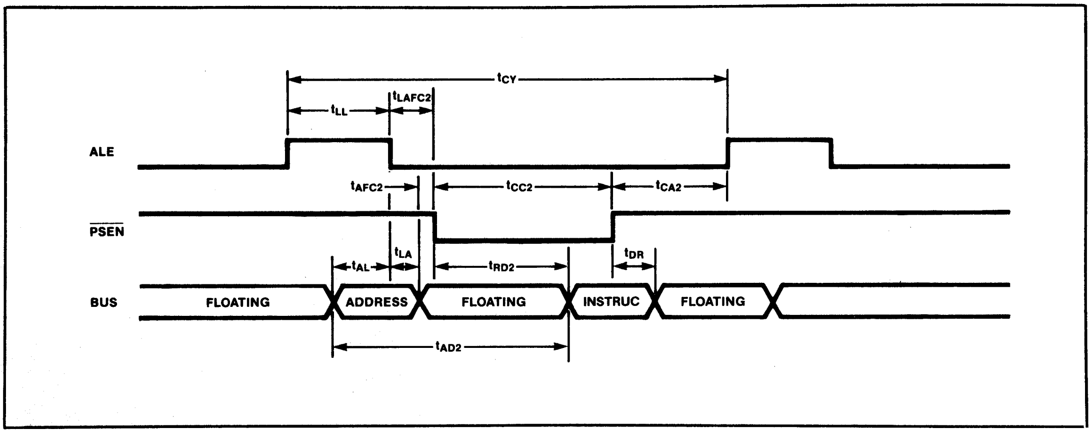
AC CHARACTERISTICS (Programming Mode)

(T_A = 25 ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21V ±0.5V or 5V ±5%)

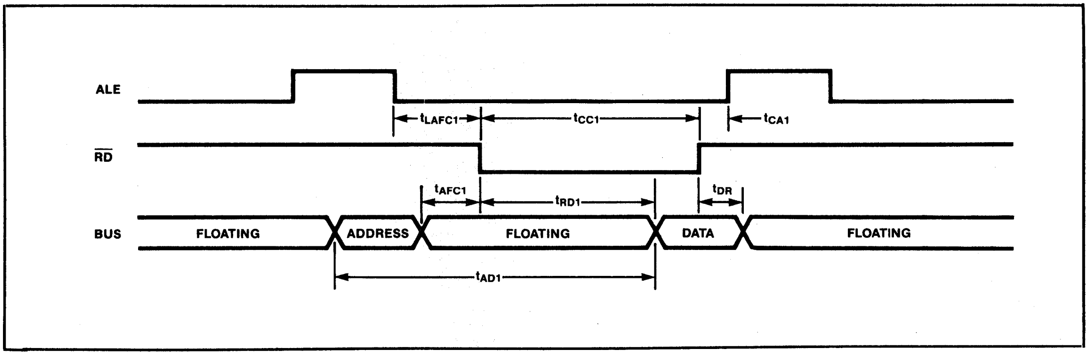
Parameter	Symbol	Value	
		Min	Max
Address setup time (before $\overline{\text{RESET}}$↑)	t_{AW}	$4 \cdot t_{CY}$	—
Address hold time (after $\overline{\text{RESET}}$↑)	t_{WA}	$4 \cdot t_{CY}$	—
Input data setup time (before PROG↑)	t_{DW}	$4 \cdot t_{CY}$	—
Input data hold time (after PROG↓)	t_{WD}	$4 \cdot t_{CY}$	—
$\overline{\text{RESET}}$ hold time (after EA↓)	t_{PH}	$4 \cdot t_{CY}$	—
V_{DD} setup time (before PROG↑)	t_{VDDW}	$4 \cdot t_{CY}$	—
V_{DD} hold time (after PROG↓)	t_{VDDH}	0	—
Program Pulse width	t_{PW}	50 ms	60 ms
T0 setup time (before $\overline{\text{RESET}}$↑)	t_{TW}	$4 \cdot t_{CY}$	—
T0 hold time (after V_{DD}↓)	t_{WT}	$4 \cdot t_{CY}$	—
Data output delay time (after T0↑)	t_{DO}	—	$4 \cdot t_{CY}$
RESET pulse width (to latch Address)	t_{WW}	$4 \cdot t_{CY}$	—
V_{DD} and PROG rise/fall time	t_r, t_f	0.5μs	2.0μs
MPU cycle time	t_{CY}	5.0μs	—
$\overline{\text{RESET}}$ setup time (before EA↑)	t_{RE}	$4 \cdot t_{CY}$	—
EA setup time (before $\overline{\text{RESET}}$↑)	t_{EA}	10 ms	—

TIMING DIAGRAMS

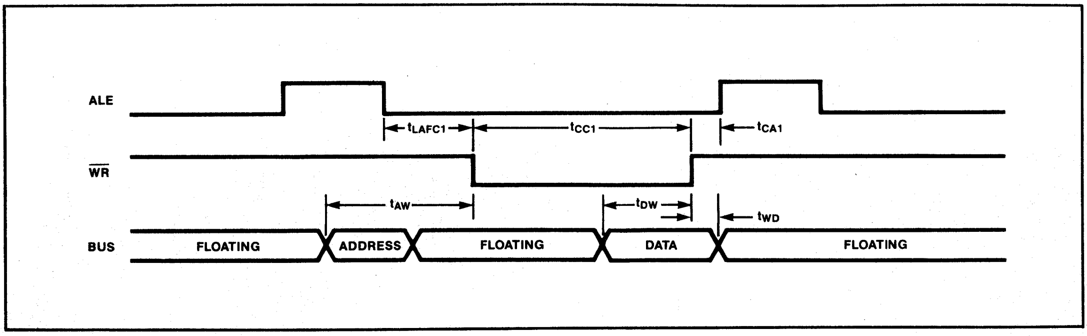
External Program Memory Operations (Instruction Fetch)



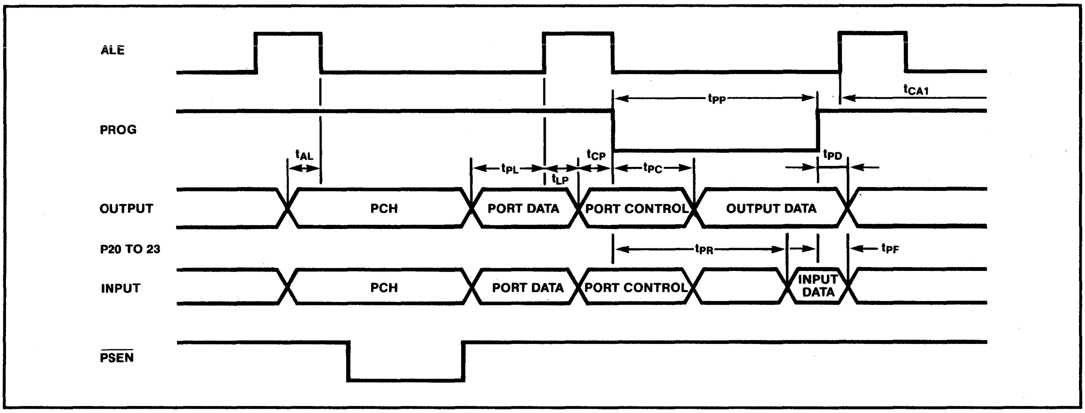
External Data Memory Read Operation



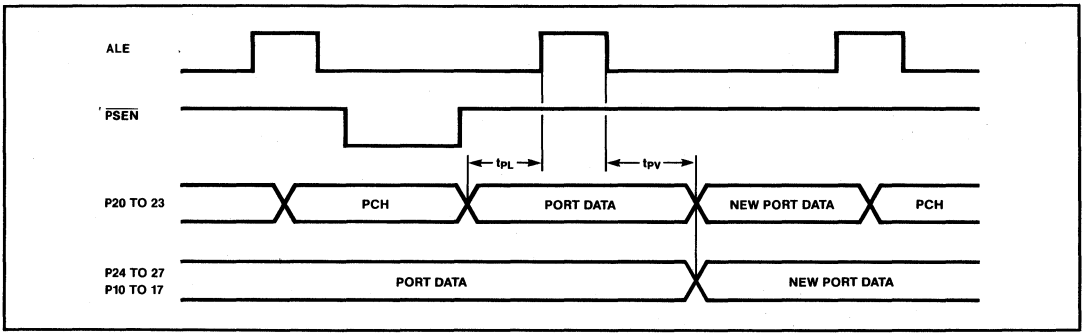
External Data Memory Write Operation



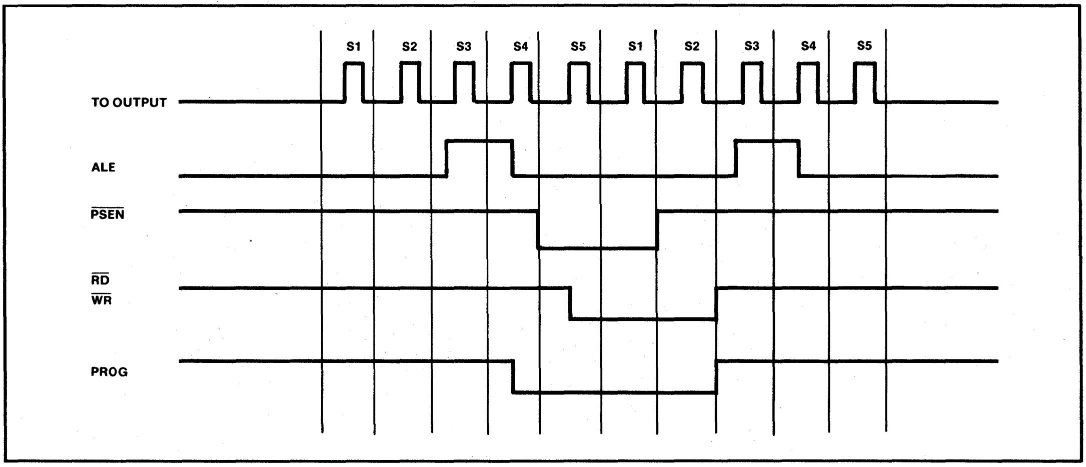
TIMING DIAGRAMS (continued)
Four Low-Order Bits of Port 2 When Expander Port And External Program Memory Are Used



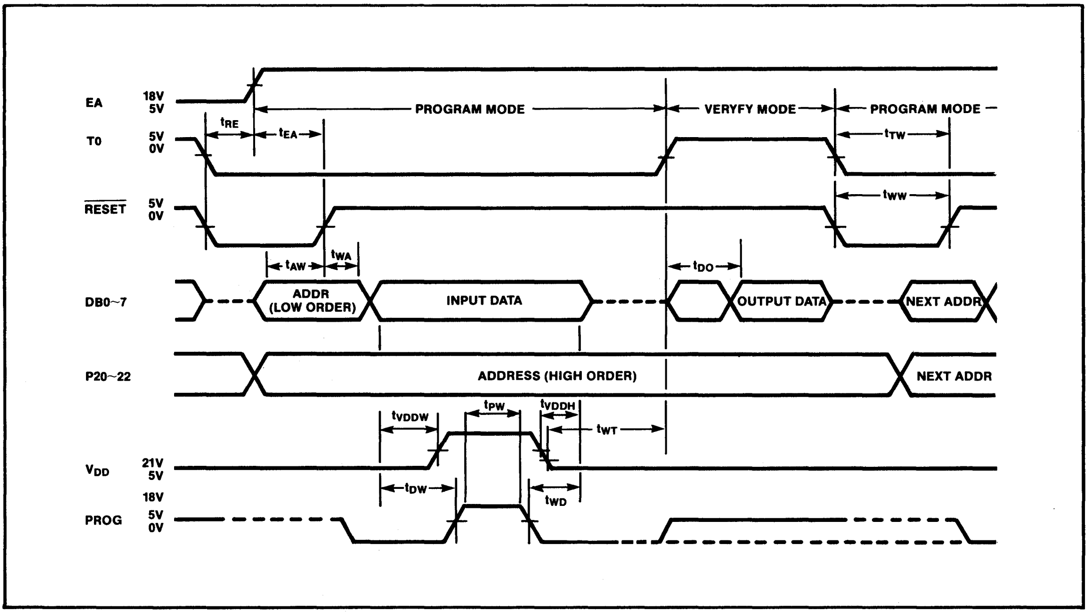
I/O Port Output Timing



Clock Output Timing

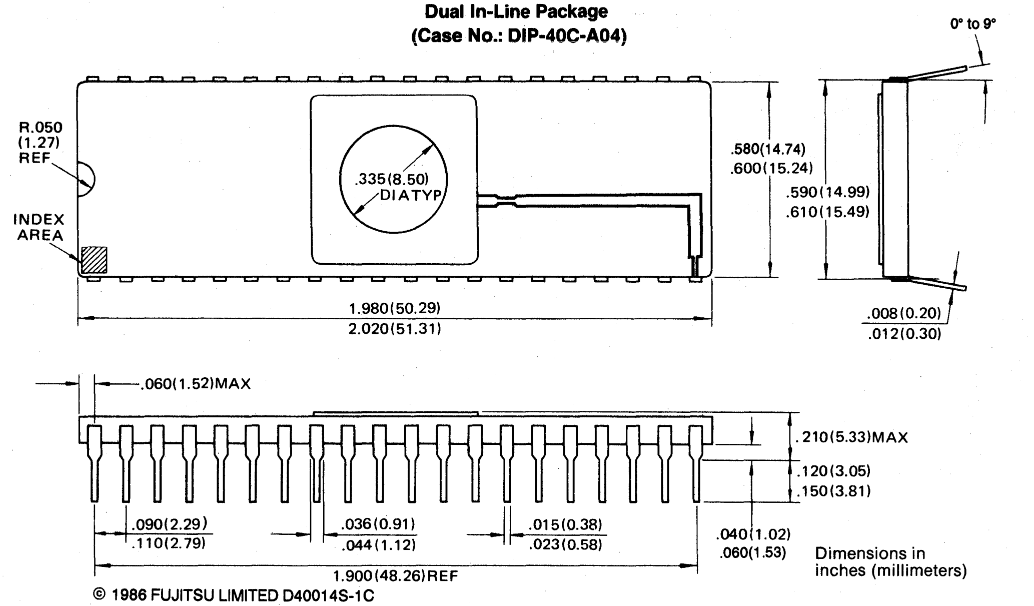


TIMING DIAGRAM (Programming the EPROM)



PACKAGE DIMENSIONS

40-Lead Ceramic (Metal Seal)
Dual In-Line Package
(Case No.: DIP-40C-A04)



Dimensions in inches (millimeters)

Advanced Products

FUJITSU

October 1986
Edition 3.0

MBL8051AH, MBL8031AH

NMOS Single-Chip 8-Bit Microcomputer

Description

The Fujitsu MBL8051AH/8031AH are single-chip 8-bit microcomputers developed as members of the MBL8051 Series. These microcomputers have powerful architecture and instruction set designed for controller applications.

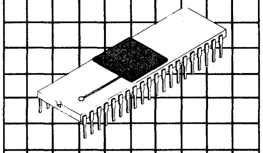
The MBL8051AH contains a 4K x 8-bit program memory (mask ROM), a 128 x 8-bit data memory (static RAM), 32 I/O lines configured as four 8-bit parallel ports, two programmable 16-bit timer/counters, a programmable serial I/O port, a five-source two-priority-level multi-interrupt function, and on-chip oscillator with clock circuitry. The MBL8031AH has all of these features except the on-chip memory.

The MBL8051AH/MBL8031AH can have up to 64K x 8-bit program memory and up to (64K + 128) x 8-bit data memory in expanded system configuration. Both microcomputers can use standard TTL compatible memories and most byte-oriented Intel MCS-80* and MCS-85* peripherals for additional memory and I/O capability.

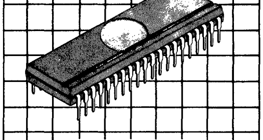
As a control-oriented feature, the MBL8051AH/MBL8031AH have a bit handling hardware: 128 bit-locations in the data memory and the special function registers can be directly addressable by the user with bit manipulation instructions. This is very useful for control type applications.

The instruction set is designed for efficient use of the program memory space: consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. At 12MHz clock, over half of the instructions execute in just 1.0μs, while the longest instructions, multiply and divide, require only 4μs.

The MBL8051AH/MBL8031AH are fabricated by Fujitsu's N-channel poly-silicon-gate E/D MOS process, and packaged in a 40-pin ceramic or plastic DIP. They have TTL compatible inputs/outputs and operate with a single +5V power supply and a 12MHz to 3.5MHz clock.



Ceramic DIP (DIP-40C-A01)

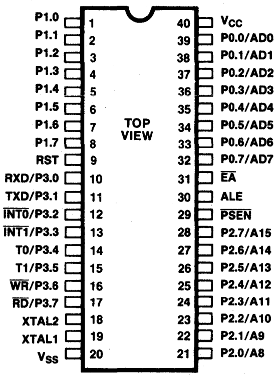


Plastic DIP (DIP-40P-M01)

*Trademark of Intel Corporation

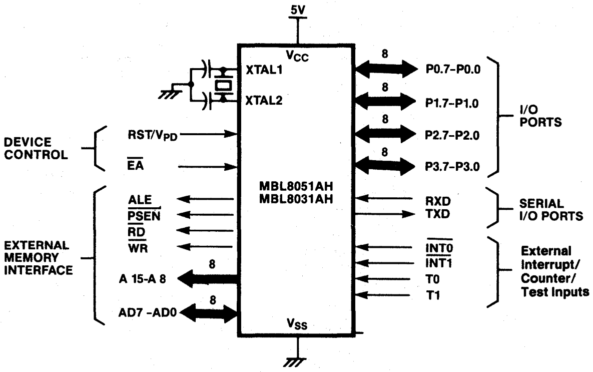
Features and Pin Assignment

- Control-Oriented 8-Bit CPU
- 4K x 8-Bit Program Memory (ROM for MBL8051AH Only)
- 128 x 8-Bit Data Memory (RAM)
- 32 I/O Lines (Four 8-Bit Ports)
- 128 x 8-Bit Special Function Registers
- Two Programmable 16-Bit Timer/Counters
- Programmable Full-Duplex Serial Channel
- Five-Source Maskable Two-Priority-Level Multi-Interrupt
- Expandability:
  - —Program Memory: Up to 64K x 8-Bits
  - —Data Memory } Up to (64K + 128) x 8 Bits
  - —I/O Ports }
- Boolean Processor:
  - —218 User Bit-Addressable Locations
  - —Bit Manipulation Instructions
- Minimum Instruction Execution Time: 1μs (at 12MHz)
- 4μs (at 12MHz) Multiply and Divide
- On-chip Oscillator (3.5MHz-12MHz)
- Power-Down Mode: 10mA at V_{PD}=5V
- TTL Compatible I/O
- Single +5V Power Supply
- N-Channel Silicon-Gate E/D MOS Process
- Two Package Options:
  - —40-Pin Ceramic DIP (Suffix C)
  - —40-Pin Plastic DIP (Suffix P)
- Compatible with Intel MCS-80*/MCS-85* Peripherals
- MBL8048 Series (equivalent to Intel MCS-48*) Architecture Enhanced with:
  - —Non-Paged Jumps
  - —Direct Addressing
  - —Four 8-Register Banks
  - —Stack Depth up to 128 Bytes
  - —Multiply, Divide, Subtract, Compare



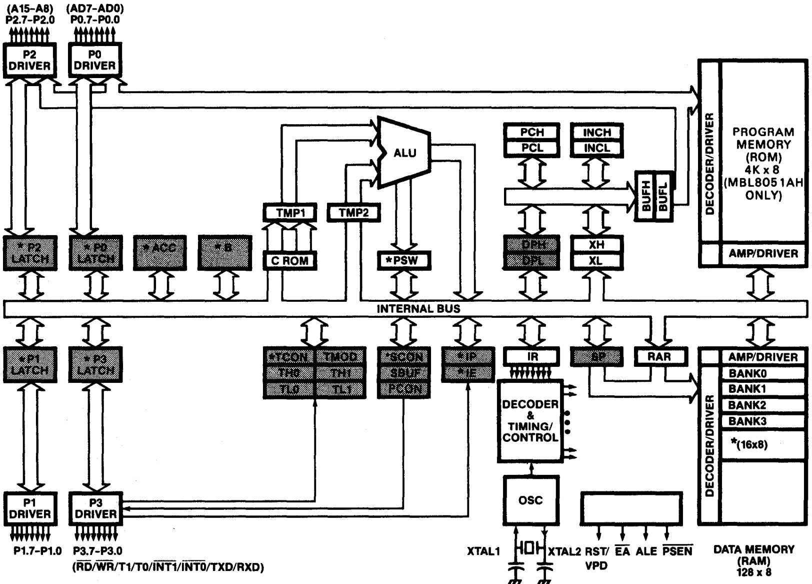
*Trademark of Intel Corporation

Logic Symbol



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Block Diagram



▨ : Members of Special Function Registers (S.F.R.)

*: Bit addressable location

Pin Description

	Symbol	Pin No.	Type	Name & Function
Power Supply	V_{CC}	40	—	+5V power supply pin.
	V_{SS}	20	—	Ground pin.
Clock	XTAL1	19	I	Crystal 1: Input to the inverting amplifier that forms part of the oscillator. This pin should be connected to ground when an external oscillator is used.
	XTAL2	18	O	Crystal 2: Output of the inverting amplifier, and input to internal clock generator. This pin receives the oscillator signal when an external oscillator is used.
I/O Ports	P0.7/AD7- P0.0/AD0	32-39	I/O	Port 0: Port 0 is an 8-bit open-drain bidirectional I/O port. As an open-drain output port, each pin can sink 8 LS-TTL loads. Port 0 pins that have 1s written to them float, and in that state will function as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1s.
	P1.7-P1.0	8-1	I/O	Port 1: Port 1 is an 8-bit quasi-bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS-TTL loads. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Pin Description
(continued)

	Symbol	Pin No.	Type	Name & Function
I/O Ports (Continued)	P2.7/A15- P2.0/A8	28-21	I/O	Port 2: Port 2 is an 8-bit quasi-bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS-TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses. In this application it uses the strong internal pullups when emitting 1s. Port 2 also receives the high-order address and control bits during program verification.
	P3.7-P3.0	17-10	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the MBL8051AH, as listed below: **Port Pin** **Alternate Function** P3.0 RXD (Serial input port) P3.1 TXD (Serial output port) P3.2 INT0 (External interrupt 0) P3.3 INT1 (External interrupt 1) P3.4 T0 (Timer 0 external input) P3.5 T1 (Timer 1 external input) P3.6 WR (External data memory write strobe) P3.7 RD (External data memory read strobe) The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The Port 3 output buffers can source/sink 4 LS-TTL loads.
Other Ports	RST	9	I	Reset input: A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor (≈8.2kΩ) from RST to V_{SS} permits power-on reset when a capacitor (≈10pF) is also connected from RST to V_{CC}.
	ALE	30	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory: ALE is emitted at a constant rate of 1/6 of the oscillator frequency, for external timing or clocking purposes, even when there are no accesses to external memory. However, one ALE pulse is skipped during each access to external data memory. ALE can sink/source 8 LS-TTL inputs.
	$\overline{\text{PSEN}}$	29	O	Program Store Enable is the read strobe to external program memory. When the device is executing out of external program memory, PSEN is activated twice each machine cycle (except that two PSEN activations are skipped during accesses to external data memory). PSEN is not activated; remaining high, during internal program memory execution.
	$\overline{\text{EA}}$	31	I	External Address Enable input: When $\overline{\text{EA}}$ is held high the CPU executes out of internal program memory (unless the program counter exceeds OFFFH). Holding $\overline{\text{EA}}$ low forces the CPU to execute out of external memory regardless of the program counter value. In the MBL8031AH, $\overline{\text{EA}}$ must be externally wired low.

Instruction Set Description

The MBL8051AH instruction set includes 111 instructions, 49 of which are single-byte, 45 two-byte and 17 three-byte. The instruction op code format consists of a function mnemonic followed by a "destination, source" operand field. This field specifies the data type and addressing method(s) to be used.

The MBL8051AH instruction set is divided into five functional groups:

- Arithmetic Operations
- Logical Operations
- Data Transfer
- Boolean Variable Manipulation
- Program & Machine Control (subroutine control/branch)

The following table summarizes the MBL8051AH instruction set.

Instruction Set Summary (1)

Arithmetic Operations

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word C	AC	F0	RS1	RS0	OV	—	P
ADD A, Rn	Add register to accumulator	2X	1/1	↕	↕	•	•	•	↕		↕
ADD A, direct	Add direct byte to accumulator	25	2/1	↕	↕	•	•	•	↕		↕
ADD A, @Ri	Add indirect RAM to accumulator	26 27	1/1	↕	↕	•	•	•	↕		↕
ADD A, #data	Add immediate data to accumulator	24	2/1	↕	↕	•	•	•	↕		↕
ADDC A, Rn	Add register to accumulator with carry	3X	1/1	↕	↕	•	•	•	↕		↕
ADDC A, direct	Add direct byte to accumulator with carry	35	2/1	↕	↕	•	•	•	↕		↕
ADDC A, @Ri	Add indirect RAM to accumulator with carry	36 37	1/1	↕	↕	•	•	•	↕		↕
ADDC A, #data	Add immediate data to accumulator with carry	34	2/1	↕	↕	•	•	•	↕		↕
SUBB A, Rn	Subtract register from accumulator with borrow	9X	1/1	↕	↕	•	•	•	↕		↕
SUBB A, direct	Subtract direct byte from accumulator with borrow	95	2/1	↕	↕	•	•	•	↕		↕
SUBB A, @Ri	Subtract indirect RAM from accumulator with borrow	96 97	1/1	↕	↕	•	•	•	↕		↕
SUBB A, #data	Subtract immediate data from accumulator with borrow	94	2/1	↕	↕	•	•	•	↕		↕
INC A	Increment accumulator	04	1/1	•	•	•	•	•	•		↕
INC Rn	Increment register	0X	1/1	•	•	•	•	•	•		•

Instruction Set Summary (1)(Continued)

Arithmetic Operations (continued)

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word							
				C	AC	FO	RS1	RSO	OV	—	P
INC direct	Increment direct byte	05	2/1	•	•	•	•	•	•		•
INC @Ri	Increment indirect RAM	06 07	1/1	•	•	•	•	•	•		•
INC DPTR	Increment data pointer	A3	1/2	•	•	•	•	•	•		•
DEC A	Decrement accumulator	14	1/1	•	•	•	•	•	•		↕
DEC Rn	Decrement register	1X	1/1	•	•	•	•	•	•		•
DEC direct	Decrement direct byte	15	2/1	•	•	•	•	•	•		•
DEC @Ri	Decrement indirect RAM	16 17	1/1	•	•	•	•	•	•		•
MUL AB	Multiply A and B	A4	1/4	↕	•	•	•	•	↕		↕
DIV AB	Divide A by B	84	1/4	↕	•	•	•	•	↕		↕
DA A	Decimal adjust accumulator	D4	1/1	↕	•	•	•	•	•		↕

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Instruction Set Summary (2)

Logical Operations

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word							
				C	AC	FO	RS1	RSO	OV	—	P
ANL A, Rn	AND register to accumulator	5X	1/1	•	•	•	•	•	•		↕
ANL A, direct	AND direct byte to accumulator	55	2/1	•	•	•	•	•	•		↕
ANL A, @Ri	AND indirect RAM to accumulator	56 57	1/1	•	•	•	•	•	•		↕
ANL A, #data	AND immediate data to accumulator	54	2/1	•	•	•	•	•	•		↕
ANL direct, A	AND accumulator to direct byte	52	2/1	•	•	•	•	•	•		•
ANL direct, #data	AND immediate data to a direct byte	53	3/2	•	•	•	•	•	•		•
ORL A, Rn	OR register to accumulator	4X	1/1	•	•	•	•	•	•		↕
ORL A, direct	OR direct byte to accumulator	45	2/1	•	•	•	•	•	•		↕
ORL A, @Ri	OR indirect RAM to accumulator	46 47	1/1	•	•	•	•	•	•		↕
ORL A, #data	OR immediate data to accumulator	44	2/1	•	•	•	•	•	•		↕
ORL direct, A	OR accumulator to direct byte	42	2/1	•	•	•	•	•	•		•
ORL direct, #data	OR immediate data to direct byte	43	3/2	•	•	•	•	•	•		•
XRL A, Rn	Exclusive-OR register to accumulator	6X	1/1	•	•	•	•	•	•		↕
XRL A, direct	Exclusive-OR direct byte to accumulator	65	2/1	•	•	•	•	•	•		↕

Instruction Set Summary (2)(Continued)

Logical Operations (continued)

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word							
				C	AC	F0	RS1	RS0	OV	—	P
XRL A, @Ri	Exclusive-OR indirect RAM to accumulator	66 67	1/1	●	●	●	●	●	●		↕
XRL A, #data	Exclusive-OR immediate data to accumulator	64	2/1	●	●	●	●	●	●		↕
XRL direct, A	Exclusive-OR accumulator to direct byte	62	2/1	●	●	●	●	●	●		●
XRL direct, #data	Exclusive-OR immediate data to direct byte	63	3/2	●	●	●	●	●	●		●
CLR A	Clear accumulator	E4	1/1	●	●	●	●	●	●		↕
CPL A	Complement accumulator	F4	1/1	●	●	●	●	●	●		●
RL A	Rotate accumulator left	23	1/1	●	●	●	●	●	●		●
RLC A	Rotate accumulator left through carry	33	1/1	↕	●	●	●	●	●		↕
RR A	Rotate accumulator right	03	1/1	●	●	●	●	●	●		●
RRC A	Rotate accumulator right through carry	13	1/1	↕	●	●	●	●	●		↕
SWAP A	Swap nibbles within accumulator	C4	1/1	●	●	●	●	●	●		●

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Instruction Set Summary (3)

Data Transfer

Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word							
				C	AC	F0	RS1	RS0	OV	—	P
MOV A, Rn	Move register to accumulator	EX	1/1	●	●	●	●	●	●		↕
*MOV A, direct	Move direct byte to accumulator	E5	2/1	●	●	●	●	●	●		↕
MOV A, @Ri	Move indirect RAM to accumulator	E6 E7	1/1	●	●	●	●	●	●		↕
MOV A, #data	Move immediate data to accumulator	74	2/1	●	●	●	●	●	●		↕
MOV Rn, A	Move accumulator to register	FX	1/1	●	●	●	●	●	●		●
MOV Rn, direct	Move direct byte to register	AX	2/2	●	●	●	●	●	●		●
MOV Rn, #data	Move immediate data to register	7X	2/1	●	●	●	●	●	●		●
MOV direct, A	Move accumulator to direct byte	F5	2/1	●	●	●	●	●	●		●
MOV direct, Rn	Move register to to direct byte	8X	2/2	●	●	●	●	●	●		●
MOV direct, direct	Move direct byte to direct byte	85	3/2	●	●	●	●	●	●		●

* MOV A, ACC is not a valid instruction

Instruction Set Summary (3)(Continued)

Data Transfer (continued)

Mnemonic		Op Code	Byte/	Program Status Word							
+ Operand	Operation	(Hex)	Cycle	C	AC	FO	RS1	RSO	OV	—	P
MOV direct, @Ri	Move indirect RAM to direct byte	86 87	2/2	●	●	●	●	●	●		●
MOV direct, #data	Move immediate data to direct byte	75	3/2	●	●	●	●	●	●		●
MOV @Ri, A	Move accumulator to indirect RAM	F6 F7	1/1	●	●	●	●	●	●		●
MOV @Ri, direct	Move direct byte to indirect RAM	A6 A7	2/2	●	●	●	●	●	●		●
MOV @Ri, #data	Move immediate data to indirect RAM	76 77	2/1	●	●	●	●	●	●		●
MOV DPTR, #data 16	Load data pointer with a 16-bit constant	90	3/2	●	●	●	●	●	●		●
MOVC A, @A+DPTR	Move code byte relative to data pointer to accumulator	93	1/2	●	●	●	●	●	●		↕
MOVC A, @A+PC	Move code byte relative to program counter to accumulator	83	1/2	●	●	●	●	●	●		↕
MOVX A, @Ri	Move external RAM (8-bit addr) to accumulator	E2 E3	1/2	●	●	●	●	●	●		↕
MOVX A, @DPTR	Move external RAM (16-bit addr) to accumulator	E0	1/2	●	●	●	●	●	●		↕
MOVX @Ri, A	Move accumulator to external RAM (8-bit addr)	F2 F3	1/2	●	●	●	●	●	●		●
MOVX @DPTR, A	Move accumulator to external RAM (16-bit addr)	F0	1/2	●	●	●	●	●	●		●

Instruction Set Summary (3)(Continued)

	Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word							
					C	AC	FO	RS1	RSO	OV	—	P
Data Transfer (continued)	PUSH direct	Push direct byte onto stack	C0	2/2	●	●	●	●	●	●		●
	POP direct	Pop direct byte from stack	D0	2/2	●	●	●	●	●	●		●
	XCH A, Rn	Exchange register with accumulator	CX	1/1	●	●	●	●	●	●		↕
	XCH A, direct	Exchange direct byte with accumulator	C5	2/1	●	●	●	●	●	●		↕
	XCH A, @Ri	Exchange indirect RAM with accumulator	C6 C7	1/1	●	●	●	●	●	●		↕
	XCHD A, @Ri	Exchange low-order digit indirect RAM with A	D6 D7	1/1	●	●	●	●	●	●		↕
Boolean Variable Manipulation	CLR C	Clear carry flag	C3	1/1	↕	●	●	●	●	●		●
	CLR bit	Clear direct bit	C2	2/1	●	●	●	●	●	●		●
	SETB C	Set carry flag	D3	1/1	↕	●	●	●	●	●		●
	SETB bit	Set direct bit	D2	2/1	●	●	●	●	●	●		●
	CPL C	Complement carry flag	B3	1/1	↕	●	●	●	●	●		●
	CPL bit	Complement direct bit	B2	2/1	●	●	●	●	●	●		●
	ANL C, bit	AND direct bit to carry flag	82	2/2	↕	●	●	●	●	●		●
	ANL C, 1 bit	AND complement of direct bit to carry flag	B0	2/2	↕	●	●	●	●	●		●
	ORL C/bit	OR direct bit to carry flag	72	2/2	↕	●	●	●	●	●		●
	ORL C, 1 bit	OR complement of direct bit to carry flag	A0	2/2	↕	●	●	●	●	●		●
	MOV C/bit	Move direct bit to carry flag	A2	2/1	↕	●	●	●	●	●		●
	MOV bit, C	Move carry flag to direct bit	92	2/2	●	●	●	●	●	●		●

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Instruction Set Summary (4)

	Mnemonic + Operand	Operation	Op Code (Hex)	Byte/ Cycle	Program Status Word							
					C	AC	FO	RS1	RSO	OV	—	P
Program and Machine Control	ACALL addr 11	Absolute subroutine call	*1	2/2	●	●	●	●	●	●		●
	CALL addr	ACALL addr 11 or LCALL addr 16			●	●	●	●	●	●		●
	LCALL addr 16	Long subroutine call	12	3/2	●	●	●	●	●	●		●
	RET	Return from subroutine	22	1/2	●	●	●	●	●	●		●
	RETI	Return from interrupt	32	1/2	●	●	●	●	●	●		●
	AJMP addr 11	Absolute jump	*1	2/2	●	●	●	●	●	●		●
	LJMP addr 16	Long jump	02	3/2	●	●	●	●	●	●		●
	SJMP rel	Short jump (relative addr)	80	2/2	●	●	●	●	●	●		●
	JMP @A+DPTR	Jump indirect relative to data pointer	73	1/2	●	●	●	●	●	●		●
	JZ rel	Jump if accumulator is zero	60	2/2	●	●	●	●	●	●		●
	JNZ rel	Jump if accumulator is not zero	70	2/2	●	●	●	●	●	●		●
	JC rel	Jump if carry flag is set	40	2/2	●	●	●	●	●	●		●
	JNC rel	Jump if carry flag is not set	50	2/2	●	●	●	●	●	●		●
	JB bit, rel	Jump if direct bit is set	20	3/2	●	●	●	●	●	●		●
	JNB bit, rel	Jump if direct bit is not set	30	3/2	●	●	●	●	●	●		●
	JBC bit, rel	Jump if direct bit is set & clear bit	10	3/2	●	●	●	●	●	●		●
	CJNE A, direct, rel	Compare direct to accumulator & jump if not equal	B5	3/2	↕	●	●	●	●	●		●
	CJNE A, #data, rel	Compare immediate data to A & jump if not equal	B4	3/2	↕	●	●	●	●	●		●
	CJNE Rn, #data, rel	Compare immediate data to reg. & jump if not equal	B6 B7	3/2	↕	●	●	●	●	●		●
	CJNE @Ri, #data, rel	Compare immediate data to indirect RAM & jump if not equal	BX	3/2	↕	●	●	●	●	●		●
	DJNZ Rn, rel	Decrement register & jump if not zero	DX	2/2	●	●	●	●	●	●		●
	DJNZ direct, rel	Decrement direct byte & jump if not zero	D5	3/2	●	●	●	●	●	●		●
	NOP	No operation	00	1/1	●	●	●	●	●	●		●

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Instruction Set Description (Continued)

Notes on Data Addressing Modes:

Rn	— Working register R0-R7 (See Table 1 below)
direct	— 128 internal RAM locations, any I/O port, control status register
@Ri	— Indirect internal RAM location addressed by register R0 or R1
#data	— 8-bit constant included in instruction
#data 16	— 16-bit constant included as bytes 2 & 3 of instruction
bit	— 128 software flags, any I/O pin, control status bit

Notes on Program Addressing Modes:

addr 16	— Destination address for LCALL & LJMP may be anywhere within the 64K program memory address space.
addr 11	— Destination address for ACALL & AJMP will be within the same 2K page of program memory as the first byte of the following instruction.
rel	— SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 to -128 bytes relative to first byte of the following instruction.

Notes on Affecting Flag Setting:

↕ — Affected (set or reset)
• — Not affected

Notes on Instruction Set Op Codes:
1. See Table 1 for op code X.
2. *The first 3 bits of op code are determined by operand (addr 11).

Table 1 Op codes of Register Access Instructions

Mnemonic + Operand	**Rn**	**R0**	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**
ADD A, Rn		28	29	2A	2B	2C	2D	2E	2F
ADDC A, Rn		38	39	3A	3B	3C	3D	3E	3F
SUBB A, Rn		98	99	9A	9B	9C	9D	9E	9F
INC Rn		08	09	0A	0B	0C	0D	0E	0F
DEC Rn		18	19	1A	1B	1C	1D	1E	1F
ANL A, Rn		58	59	5A	5B	5C	5D	5E	5F
ORL A, Rn		48	49	4A	4B	4C	4D	4E	4F
XRL A, Rn		68	69	6A	7B	6C	6D	6E	6F
MOV A, Rn		E8	E9	EA	EB	EC	ED	EE	EF
MOV Rn, A		F8	F9	FA	FB	FC	FD	FE	FF
MOV Rn, #data		78	79	7A	7B	7C	7D	7E	7F
MOV Rn, direct		A8	A9	AA	AB	AC	AD	AE	AF
MOV direct, Rn		88	89	8A	8B	8C	8D	8E	8F
XCH A, Rn		C8	C9	CA	CB	CC	CD	CE	CF

Instruction Set Description (Continued)

Instruction Code Summary

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	JBC bit, rel	JB bit, rel	JNB bit, rel	JC rel	JNC rel	JZ rel	JNZ rel	SJMP rel	MOV DPTR,# data 16	ORL C, /bit	ANL C, /bit	PUSH dir	POP dir	MOVX A, @DPTR	MOVX @ DPTR, A
1	AJMP (P0)	ACALL (P0)	AJMP (P1)	ACALL (P1)	AJMP (P2)	ACALL (P2)	AJMP (P3)	ACALL (P3)	AJMP (P4)	ACALL (P4)	AJMP (P5)	ACALL (P5)	AJMP (P6)	ACALL (P6)	AJMP (P7)	ACALL (P7)
2	LJMP addr16	LCALL addr16	RET	RETI	ORL dir, A	ANL dir, A	XRL dir, A	ORL C, bit	ANL C, bit	MOV bit, C	MOV C, bit	CPL bit	CLR bit	SETB bit	MOVX A, @R0	MOVX @R0, A
3	RR A	RRC A	RL A	RLC A	ORL dir, #data	ANL dir, #data	XRL dir, #data	JMP @A+DPTR	MOVCA, @A+PC	MOVCA, @A+DPTR	INC DPTR	CPL C	CLR C	SETB C	MOVX A, @R1	MOVX @R1, A
4	INC A	DEC A	ADD A, #data	ADDC A, #data	ORL A, #data	ANL A, #data	XRL A, #data	MOV A, #data	DIV AB	SUBB A, #data	MUL AB	CJNE, A, #data, rel	SWAP A	DA A	CLR A	CPL A
5	INC dir	DEC dir	ADD A, dir	ADDC A, dir	ORL A, dir	ANL A, dir	XRL A, dir	MOV dir, #data	MOV dir, dir	SUBB A, dir		CJNE A, dir, rel	XCH A, dir	DJNZ dir, rel	MOV A, dir	MOV dir, A
6	INC @R0	DEC @R0	ADD A, @R0	ADDC A, @R0	ORL A, @R0	ANL A, @R0	XRL A, @R0	MOV @R0, #data	MOV dir, @R0	SUBB A, @R0	MOV @R0, dir	CJNE @R0, #data, rel	XCH A, @R0	XCHD A, @R0	MOV A, @R0	MOV @ R0, A
7	INC @R1	DEC @R1	ADD A, @R1	ADDC A, @R1	ORL A, @R1	ANL A, @R1	XRL A, @R1	MOV @R1, # data	MOV dir, @R1	SUBB A, @R1	MOV @R1, dir	CJNE @R1, #data, rel	XCH A, @R1	XCHD A, @R1	MOV A, @R1	MOV @ R1, A
8	INC R0	DEC R0	ADD A, R0	ADDC A, R0	ORL A, R0	ANL A, R0	XRL A, R0	MOV R0, #data	MOV dir, R0	SUBB A, R0	MOV R0, dir	CJNE R0, #data, rel	XCH A, R0	DJNZ R0, rel	MOV A, R0	MOV R0, A
9	INC R1	DEC R1	ADD A, R1	ADDC A, R1	ORL A, R1	ANL A, R1	XRL A, R1	MOV R1, #data	MOV dir, R1	SUBB A, R1	MOV R1, dir	CJNE R1, #data, rel	XCH A, R1	DJNZ R1, rel	MOV A, R1	MOV R1, A
A	INC R2	DEC R2	ADD A, R2	ADDC A, R2	ORL A, R2	ANL A, R2	XRL A, R2	MOV R2, #data	MOV dir, R2	SUBB A, R2	MOV R2, dir	CJNE R2, #data, rel	XCH A, R2	DJNZ R2, rel	MOV A, R2	MOV R2, A
B	INC R3	DEC R3	ADD A, R3	ADDC A, R3	ORL A, R3	ANL A, R3	XRL A, R3	MOV R3, #data	MOV dir, R3	SUBB A, R3	MOV R3, dir	CJNE R3, #data, rel	XCH A, R3	DJNZ R3, rel	MOV A, R3	MOV R3, A
C	INC R4	DEC R4	ADD A, R4	ADDC A, R4	ORL A, R4	ANL A, R4	XRL A, R4	MOV R4, #data	MOV dir, R4	SUBB A, R4	MOV R4, dir	CJNE R4, #data, rel	XCH A, R4	DJNZ R4, rel	MOV A, R4	MOV R4, A
D	INC R5	DEC R5	ADD A, R5	ADDC A, R5	ORL A, R5	ANL A, R5	XRL A, R5	MOV R5, #data	MOV dir, R5	SUBB A, R5	MOV R5, dir	CJNE R5, #data, rel	XCH A, R5	DJNZ R5, rel	MOV A, R5	MOV R5, A
E	INC R6	DEC R6	ADD A, R6	ADDC A, R6	ORL A, R6	ANL A, R6	XRL A, R6	MOV R6, #data	MOV dir, R6	SUBB A, R6	MOV R6, dir	CJNE R6, #data, rel	XCH A, R6	DJNZ R6, rel	MOV A, R6	MOV R6, A
F	INC R7	DEC R7	ADD A, R7	ADDC A, R7	ORL A, R7	ANL A, R7	XRL A, R7	MOV R7, #data	MOV dir, R7	SUBB A, R7	MOV R7, dir	CJNE R7, #data, rel	XCH A, R7	DJNZ R7, rel	MOV A, R7	MOV R7, A

◤ 2Byte		3Byte ◥
◣ 2Cycle	Boolean Manipulation	4Cycle ◢

Absolute Maximum Ratings

Parameter	Symbol	Rating Min.	Rating Max.	Unit
Supply Voltage	V_{CC}	V_{SS}-0.3	V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{SS}+7.0	V
Output Voltage	V_{OUT}	V_{SS}-0.3	V_{SS}+7.0	V
Power Dissipation	P_D		1.5	W
Operating Ambient Temperature	T_A	0	+70	°C
Storage Temperature	Tstg	-55	+150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}		0		V
Operating Ambient Temperature	T_A	0		+70	°C

DC Characteristics

(V_{CC} = 5V ±10%,
V_{SS} = 0V, T_A = 0°C to 70°C)

Parameter	Pin	Symbol	Value Min.	 Max.	Unit	Test Conditions
Input High Voltage	All Inputs except RST and XTAL2	V_{IH}	2.0	V_{CC}+0.5	V	
	RST and XTAL2	V_{IH1}	2.5	V_{CC}+0.5	V	XTAL1=0V
Input Low Voltage		V_{IL}	V_{SS}-0.3	0.8	V	
Power-Down Voltage	VPD	V_{PD}	4.5	5.5	V	V_{CC}=0V
Output High Voltage	Ports 1, 2, 3	V_{OH}	2.4		V	I_{OH}=-80μA
	Port 0, ALE, $\overline{\text{PSEN}}$	V_{OH1}	2.4		V	I_{OH}=-400μA
Output Low Voltage	Ports 1, 2, 3	V_{OL}		0.45	V	I_{OL}=1.6mA
	Port 0, ALE, $\overline{\text{PSEN}}$	V_{OL1}		0.45	V	I_{OL}=3.2mA
Low Level Input Leakage Current	Ports 1, 2, 3	I_{IL}		-500	μA	V_{IN}=0.45V
	XTAL2	I_{IL2}		-3.2	mA	XTAL1=0V, VIN=0.45V
High Level Input Leakage Current	RST	I_{IH1}		500	μA	$V_{IN} < V_{CC}$-1.5V
Input Leakage Current	Port 0, $\overline{\text{EA}}$	I_{LI}	-10	+10	μA	0.45V<V_{IN}<V_{CC}
Power Supply Current	V_{CC}	I_{CC}		125	mA	All outputs open; $\overline{\text{EA}}$ = V_{CC}
Power-Down Current	VPD	I_{PD}		10	mA	V_{CC}=0V, V_{PD}=5V
Capacitance of I/O Buffer		C_{IO}		10	pF	f_C=1.0MHz,

Note: Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases, the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

AC Characteristics

($V_{CC}=5V\pm10\%$, $V_{SS}=0V$; $T_A=0°C$ to $70°C$, $C_L=100pF$ for Port 0, ALE and $\overline{\text{PSEN}}$ outputs, $C_L=80pF$ for all other outputs)

External Program Memory Characteristics

		fc = 12 MHz			fc = 3.5MHz to 12 MHz		
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Min.**	**Max.**	**Unit**
Oscillation Period	TCLCL	83		ns	1/fc (Max.)	1/fc (Min.)	
Cycle Time	TCY	1.0		µs	12TCLCL (Min.)	12TCLCL (Max.)	
ALE Pulse Width	TLHLL	127		ns	2TCLCL-40		ns
Address Setup Time (To ALE)	TAVLL	43		ns	TCLCL-40		ns
Address Hold Time (After ALE)	TLLAX	48		ns	TCLCL-35		ns
Instr In Delay Time (After ALE)	TLLIV		233	ns		4TCLCL-100	ns
ALE to $\overline{\text{PSEN}}$	TLLPL	58		ns	TCLCL-25		ns
$\overline{\text{PSEN}}$ Pulse Width	TPLPH	215		ns	3TCLCL-35		ns
Instr In Delay Time (After $\overline{\text{PSEN}}$)	TPLIV		125	ns		3TCLCL-125	ns
Input Instr Hold Time (After $\overline{\text{PSEN}}$)	TPXIX	0		ns	0		ns
Input Instr Float Time (After $\overline{\text{PSEN}}$)	TPXIZ		63	ns		TCLCL-20	ns
Address Delay Time (After $\overline{\text{PSEN}}$)	TPXAV	75		ns	TCLCL-8		ns
Input Instr Delay Time (After Address)	TAVIV		302	ns		5TCLCL-115	ns
Address Float Time (To $\overline{\text{PSEN}}$)	TPLAZ		20	ns		20	ns

External Data Memory Characteristics

$\overline{\text{RD}}$ Pulse Width	TRLRH	400		ns	6TCLCL-100		ns
$\overline{\text{WR}}$ Pulse Width	TWLWH	400		ns	6TCLCL-100		ns
Address Hold Time (After ALE)	TLLAX	48		ns	TCLCL-35		ns
Data In Delay Time (After $\overline{\text{RD}}$)	TRLDV		252	ns		5TCLCL-165	ns
Data Hold Time (After $\overline{\text{RD}}$)	TRHDX	0		ns	0		ns
Data Float Time (After $\overline{\text{RD}}$)	TRHDZ		97	ns		2TCLCL-70	ns
Data In Delay Time (After ALE)	TLLDV		517	ns		8TCLCL-150	ns
Data In Delay Time (After Address)	TAVDV		585	ns		9TCLCL-165	ns
ALE To $\overline{\text{RD}}$ or $\overline{\text{WR}}$	TLLWL	200	300	ns	3TCLCL-50	3TCLCL+50	ns
Address Setup Time (To $\overline{\text{RD}}$ or $\overline{\text{WR}}$)	TAVWL	203		ns	4TCLCL-130		ns
$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High To ALE High	TWHLH	43	123	ns	TCLCL-40	TCLCL+40	ns

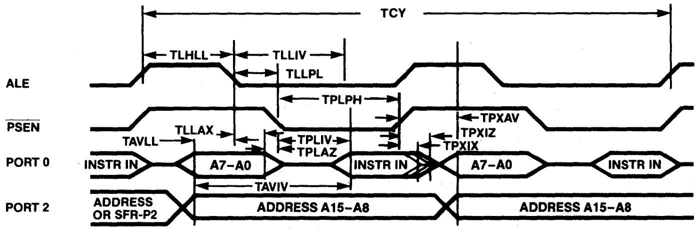
AC Characteristics

(V_{CC} = 5V ±10%, V_{SS} = 0V; T_A = 0°C to 70°C, C_L = 100pF for Port 0, ALE and $\overline{PSEN}$ outputs, C_L = 80pF for all other outputs)

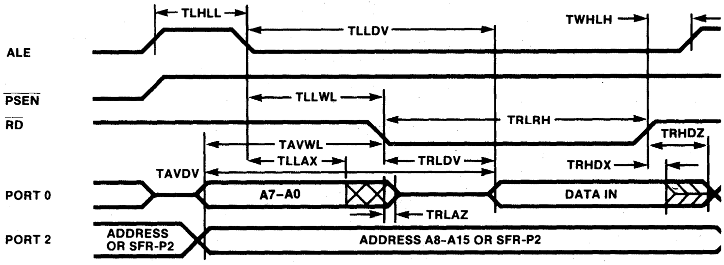
External Data Memory Characteristics (Continued)

		fc = 12 MHz			fc = 3.5MHz to 12 MHz		
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Min.**	**Max.**	**Unit**
Data Valid To $\overline{WR}$ Transition	TQVWX	23		ns	TCLCL-60		ns
Data Setup Time (Before $\overline{WR}$)	TQVWH	433		ns	7TCLCL-150		ns
Data Hold Time (After $\overline{WR}$)	TWHQX	33		ns	TCLCL-50		ns
Address Float Time (After $\overline{RD}$)	TRLAZ		20	ns		20	ns

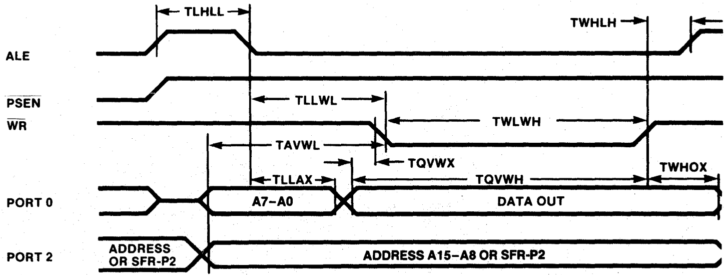
External Program Memory Read Cycle Timing Diagram



External Data Memory Read Cycle Timing Diagram



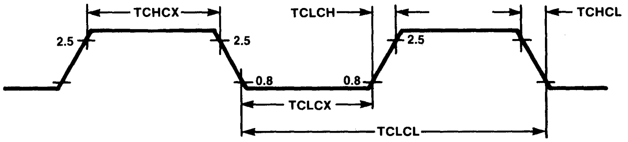
External Data Memory Write Cycle Timing Diagram



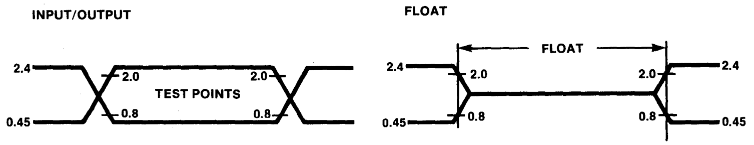
External Clock Drive Characteristics

		fc = 3.5 MHz to 12 MHz		
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Oscillation Frequency	1/TCLCL	3.5	12	ns
High Time	TCHCX	20		ns
Low Time	TCLCX	20		ns
Rise Time	TCLCH		20	ns
Fall Time	TCHCL		20	ns

External Clock Timing Diagram

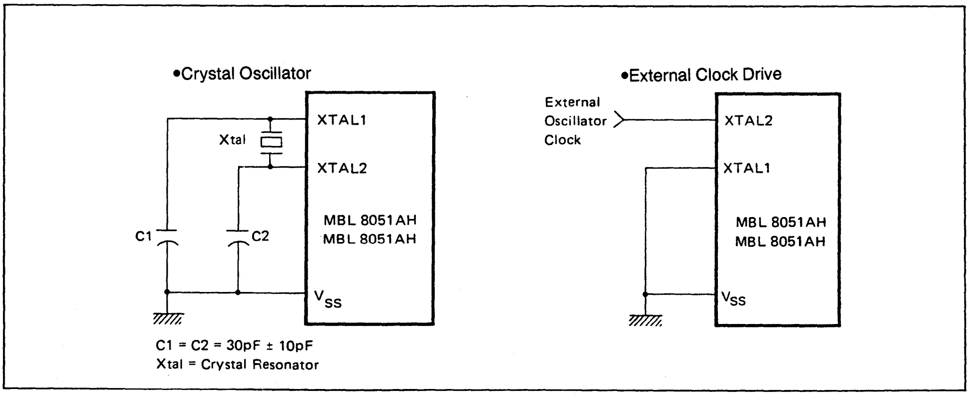


AC Testing Input/Output and Float Waveforms



AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400μA at the voltage test levels.

Oscillator Configurations

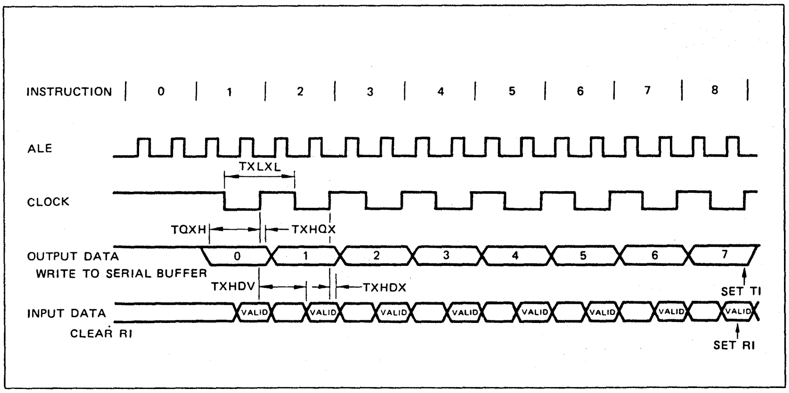


Serial Port Timing—Shift Register Mode

(Test Conditions: $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0°C$ to $70°C$, $C_L = 80$ pF)

Symbol	Parameter	f_C = 12MHz		f_c = 3.5MHz to 12MHz		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL-133	ns

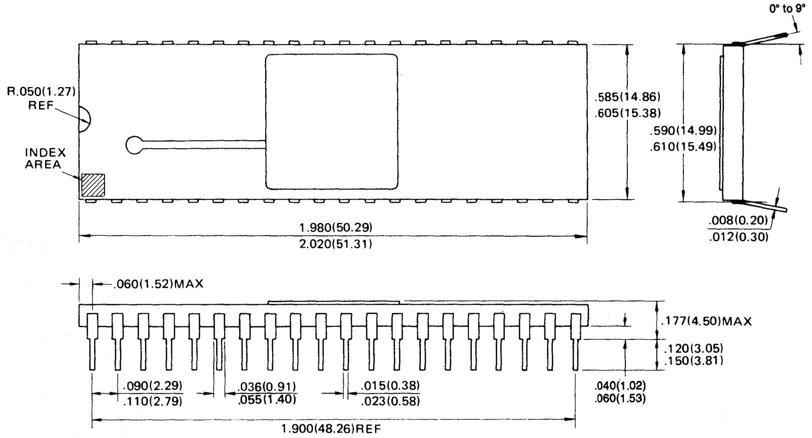
Serial Port Timing Diagram



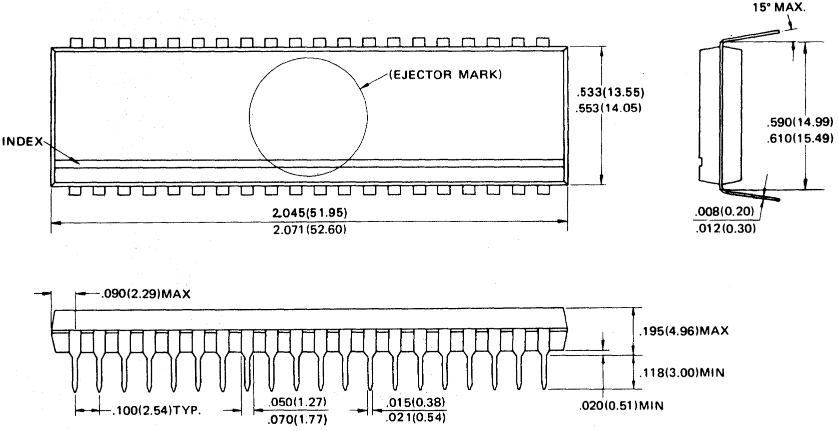
Package Dimensions

Dimensions in inches (millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)



40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



Advanced Products

FUJITSU

MBL80C49H/N
MBL80C39H/N
CMOS Single-Chip 8-Bit Microcomputer

November 1984
Edition 1.0

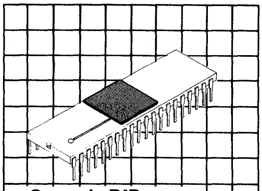
Description

The Fujitsu MBL80C49/MBL80C39 is a totally self-contained 8-bit single-chip microcomputer fabricated with silicon-gate CMOS technology. The MBL80C49 has an 8-bit MPU, a 2K × 8 ROM program memory, and 128 × 8 RAM data memory, 27 I/O ports, an 8-bit timer/counter, and clock generator on chip. The MBL80C39 is identical to the MBL80C49 except without internal program memory. It can be used with external memory for system prototyping and preproduction systems.

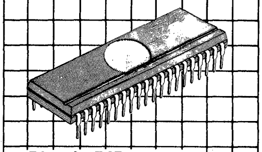
The design is optimized for low cost and high performance applications because the MBL80C49/MBL80C39 is fabricated on a single silicon chip and can be used for applications that require additional expansion of ROM, RAM, I/O ports, and so on.

This microcomputer permits external program operation and single-step operation. Low power applications are possible by using the standby-mode feature. The software is upward compatible with the MBL8049/MBL8039 and Intel 8049/8039.

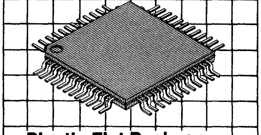
The MBL80C49/MBL80C39 uses a single power supply of +5V. It is packaged in a 40-pin DIP or a 48-pin Flat Package. Operation of N version (6 MHz) is guaranteed over the range of -40°C to +85°C, and H version (11 MHz), 0°C to +70°C.



Ceramic DIP (DIP-40C-A01)



Plastic DIP (DIP-40P-M01)



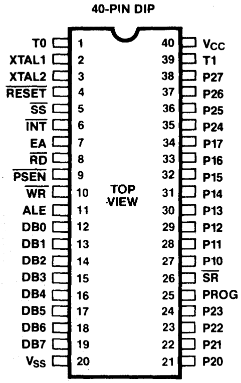
Plastic Flat Package (FPT-48P-M02)

Features

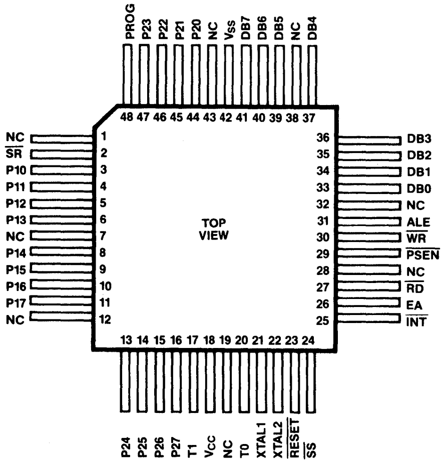
- **8-bit Single-chip Microcomputer**
- **12-bit Addressing**
- **98 Instructions (232 Instruction Codes): 70% of Instructions are Single Byte.**
- **2.5 μs Instruction Cycle for N version, 1.36 μs instruction cycle for H version: All instructions are 1 or 2 cycle.**
- **ALU Functions: Addition, Decimal Adjust Addition, and Logic Operations**
- **2K x 8-bit ROM**
- **128 x 8-bit RAM**
- **8-level Stack**
- **8 pairs of Working Registers**
- **8-bit Interval Timer/Event Counter**
- **27 I/O Lines: Two 8-bit I/O Ports, One Data Bus, Two Test Pins and One Interrupt**
- **Easily Expandable Memory and I/O**
- **On-chip Clock Generator (or External Clock)**
- **Single-level Interrupt Capability**
- **Single-step Operation Capability**
- **External Program Mode Capability**
- **Low-power Standby Mode Capability by HALT and STOP Instructions**
- **Single +5V Power Supply**
- **Silicon-gate CMOS Technology**
- **Standard 40-pin DIP (Ceramic/Plastic)**
- **Standard 48-pin Flat Package**
- **Compatible with Intel 8049/8039 and Fujitsu MBL8049/MBL8039**

Pin Assignment

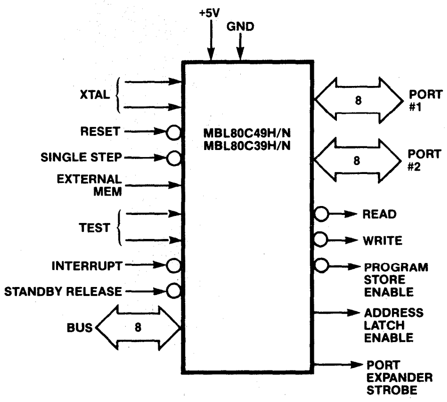
40-PIN DIP



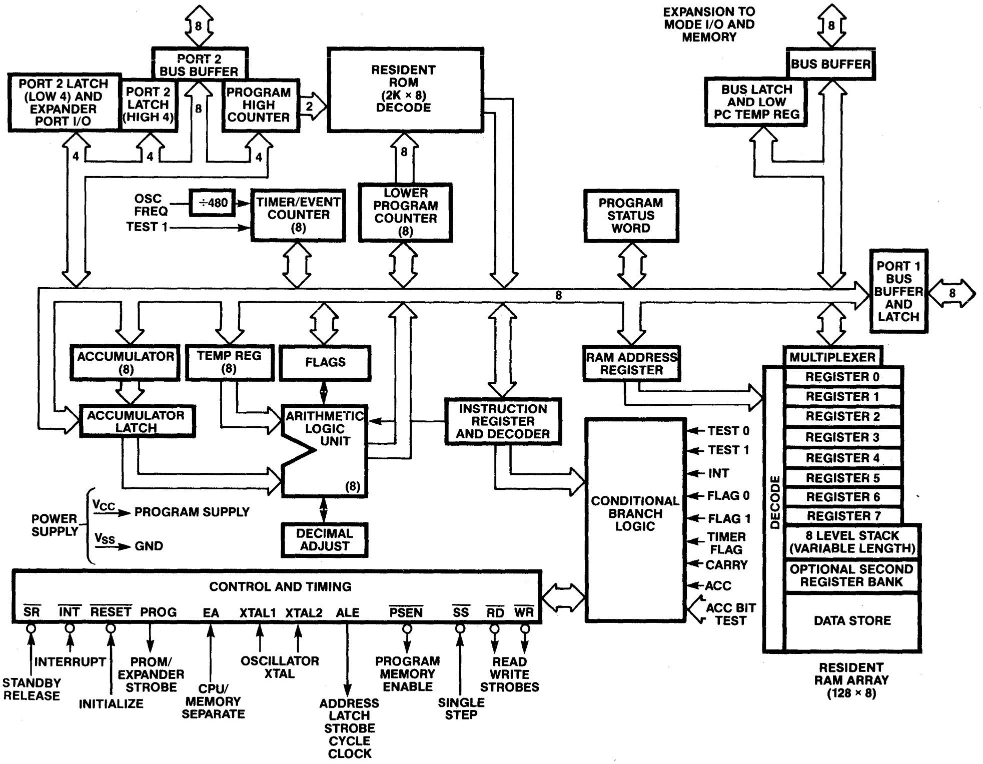
48-PIN FLAT PACK



Logic Symbol



Block Diagram



Pin Description

Symbol	Name	Pin No.*	Type	Function
V_{CC}	Power Supply	40 (18)	—	Main power supply; +5V during operation.
V_{SS}	Ground	20 (42)	—	Circuit GND potential.
XTAL1	Crystal 1	2 (21)	I	One side of crystal input for internal oscillator. Also input for external source. (Non-TTL level input)
XTAL2	Crystal 2	3 (22)	I	Other side of crystal input.
PROG	Program	25 (48)	O	Output strobe for MBL82C43 I/O expander.
P10-P17	Port 1**	27-34 (3-6, 8-11)	I/O	8-bit quasi-bidirectional port.
P20-P23	Port 2**	21-24 (44-47)	I/O	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for MBL82C43.
P24-P27		35-38 (13-16)		

Pin Description
(Continued)

Symbol	Name	Pin No.*	Type	Function
DB0-DB7	Data Bus	12-19 (33-37, 39-41)	I/O	True bidirectional port which can be written or read synchronously using the $\overline{\text{RD}}$, $\overline{\text{WR}}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction under control of ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.
T0	Test 0	1 (20)	I/O	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	Test 1	39 (17)	I	Input pin testable uising the JT1, and JNT1 instructions. Can be designated as the event counter input using the STRT CNT instruction.
$\overline{\text{INT}}$	Interrupt Request	6 (25)	I	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. (Active low). Interrupt must remain low for at least 3 machine cycles to ensure proper operation.
$\overline{\text{RESET}}$	Reset**	4 (23)	I	Input used to initialize the processor. (Active low) (Non-TTL level input)
$\overline{\text{RD}}$	Read	8 (27)	O	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. (Active low) Used as a read strobe to external data memory.
$\overline{\text{WR}}$	Write	10 (30)	O	Output strobe during a BUS write. (Active low) Used as write strobe to external data memory.
ALE	Address Latch Enable	11 (31)	O	This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{\text{PSEN}}$	Program Store Enable	9 (29)	O	This output occurs only during a fetch to external program memory. (Active low)
$\overline{\text{SS}}$	Single Step**	5 (24)	I	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	External Access	7 (26)	O	External Access forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
$\overline{\text{SR}}$	Standby Release**	26 (2)	I	This is the control input for standby operation. A low level on this input releases the MPU from the standby mode.

Note: *Bracketed value is applied to Flat Package.
**These pins are internally pulled up.

Functional Description

Architecture

The following sections break the MBL80C49 into function blocks and describe each in detail. See Block Diagram.

Arithmetic Section

The arithmetic section of the processor contains the basic data manipulation functions of the MBL80C49 and can be divided into the following blocks:

- Arithmetic Logic Unit (ALU)
- Accumulator
- Carry Flag
- Instruction Decoder

In a typical operation, data stored in the accumulator is combined in the ALU with data from another source on the internal bus (such as a register or I/O port). The result is stored in the accumulator or another register.

The following is a detailed description of the function of each block.

Instruction Decoder

The operation code (op code) portion of each program instruction is stored in the Instruction Decoder and converted to outputs which control the function of each of the blocks of the Arithmetic Section. These lines control the source of data and the destination register as well as the function performed in the ALU.

Arithmetic Logic Unit

The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under control of the Instruction Decoder. The ALU can perform the following functions:

- Add With or Without Carry
- AND, OR, Exclusive OR
- Increment/Decrement
- Bit Complement
- Rotate Left, Right
- Swap Nibbles
- BCD Decimal Adjust

If the operation performed by the ALU results in a value represented by more than 8 bits (overflow of most significant bit), a Carry Flag is set in the Program Status Word.

Accumulator

The accumulator is the single most important data register in the processor, being one of the sources of input to the ALU and often the destination of the result of operations performed in the ALU. Data to and from I/O ports and memory also normally passes through the accumulator.

Program Memory

Resident program memory consists of 2048 words eight bits wide which are addressed by the program counter. In the MBL80C49 the memory is ROM which is mask programmable at the factory. The MBL80C39 has no internal program memory and is used with external memory devices. Program code is completely interchangeable among the various versions. To access the upper 2K of program memory in the MBL80C49, a select memory bank and a JUMP or CALL instruction must be executed to cross the 2K boundary.

There are three Program Memory locations of special importance as shown in Fig. 1.

Location 0

Activating the Reset line of the processor causes the first instruction to be fetched from location 0.

Location 3

Activating the Interrupt input line of the processor (if interrupt is enabled) causes a jump to subroutine at location 3.

Location 7

A timer/counter interrupt resulting from timer/counter overflow (if enabled) causes a jump to subroutine at location 7.

Therefore, the first instruction to be executed after initialization is stored in location 0, the first word of an external interrupt service subroutine is stored in location 2, and the first word of a timer/counter service routine is stored in location 7. Program memory can be used to store constants as well as program instructions. Instructions such as MOVP and MOVP3 allow easy access to data "look-up" tables.

Data Memory

Resident data memory is organized as 128 words 8-bits wide in the MBL80C49/MBL80C39. All locations are indirectly addressable through either of two RAM Pointer Registers which reside at address 0 and 1 of the register array. In addition, as shown in Fig. 2, the first 8 locations (0–7) of the array are designated as working registers and are directly addressable by several instructions. Since these registers are more easily addressed, they are usually used to store frequently accessed intermediate results. The DJNZ instruction makes very efficient use of the working registers as program loop counters by allowing the programmer to decrement and test the register in a single instruction.

By executing a Register Bank Switch instruction (SEL RB) RAM location 24–31 are designated as the working registers in place of locations 0–7 and are then directly addressable. This second bank of working registers may be used as an extension of the first bank or reserved for use during interrupt service subroutines allowing the registers of Bank 0 used in the main program to be instantly "saved" by a Bank Switch. Note that if this second bank is not used, locations 24–31 are still addressable as general purpose RAM. Since the two RAM pointer Registers R0 and R1 are a part of the working register array, bank switching

Functional Description
(Continued)

effectively creates two more pointer registers (R0/ and R1/) which can be used with R0 and R1 to easily access up to four separate working areas in RAM at one time. RAM locations (8–23) also serve a dual role in that they contain the program counter stack. These locations are addressed by the Stack Pointer during subroutine calls as well as by RAM Pointer Registers R0 and R1. If the level of subroutine nesting is less than 8, all stack registers are not required and can be used as general purpose RAM locations. Each level of subroutine nesting not used provides the user with two additional RAM locations.

Input/Output

The MBL80C49 has 27 lines which can be used for input or output functions. These lines are grouped as 3 ports of 8 lines each which serve as either inputs, outputs of bidirectional ports and 3 "test" inputs which can alter program sequences when tested by conditional jump instructions.

Ports 1 and 2

Ports 1 and 2 are each 8 bits wide and have identical characteristics. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction. Inputs are fully TTL compatible and outputs will drive one standard TTL load.

The lines of ports 1 and 2 are called quasi-bidirectional because of special output circuit structure which allows each line to serve as an input, and output, or both even though outputs are statically latched. Each line is continuously pulled up to V_{CC} through a resistive device of relatively high impedance.

This pullup is sufficient to provide the source current for a TTL high level yet can be pulled low by a standard TTL gate thus allowing the same pin to be used for both input and output. To provide fast switching times in a "0" to "1" transition to relatively low impedance device is switched in momentarily (≈1/5 of a machine cycle) whenever a "1" is written to the line. When a "0" is written to the line a low impedance device overcomes the light pullup and provides TTL current sinking capability. Since the pulldown transistor is a low impedance device a "1" must first be written to any line which is to be used as an input. Reset initializes all lines to the high impedance "1" state.

It is important to note that the ORL and ANL are read/write operations. When executed, the μC "reads" the port, modifies the data according to the instruction, then "writes" the data back to the port. The "writing" (essentially an OUTL instruction) enables the low impedance pullup momentarily again even if the data was unchanged from a "1". This specifially applies to the configurations that have inputs and outputs mixed together on the same port.

Bus

Bus is also an 8-bit port which is a true bidirectional port with associated input and output strobes. If the bidirectional feature is not needed, Bus can serve as either a statically latched output port or non-latched input port. Input and output lines on this port cannot be mixed however.

As a static port, data is written and latched using the OUTL instruction and inputted using the INS instruction. The INS and OUTL instructions generate pulses on the corresponding $\overline{\text{RD}}$ and $\overline{\text{WR}}$ output strobe lines; however, in the static port mode they are generally not used. As a bidirectional port the MOVX instructions are used to read and write the port. A write to the port generates a pulse on the $\overline{\text{WR}}$ output line and output data is valid at the trailing edge of $\overline{\text{WR}}$. A read of the port generates a pulse on the $\overline{\text{RD}}$

Figure 1. Program Memory Map

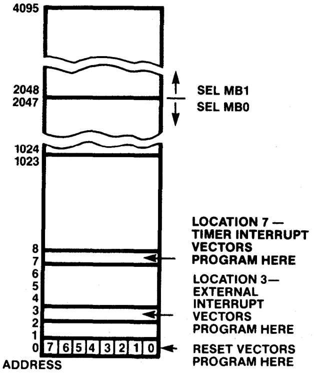
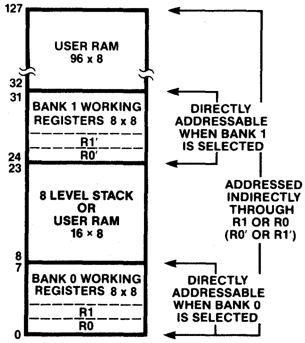

4095
2048
2047
1024
1023
SEL MB1
SEL MB0
8
7
6
5
4
3
2
1
0
7 6 5 4 3 2 1 0
ADDRESS
LOCATION 7 — TIMER INTERRUPT VECTORS PROGRAM HERE
LOCATION 3— EXTERNAL INTERRUPT VECTORS PROGRAM HERE
RESET VECTORS PROGRAM HERE

Figure 2. Data Memory Map


127
USER RAM 96 x 8
32
31
BANK 1 WORKING REGISTERS 8 x 8
R1'
R0'
24
23
8 LEVEL STACK OR USER RAM 16 × 8
8
7
BANK 0 WORKING REGISTERS 8 x 8
R1
R0
0
DIRECTLY ADDRESSABLE WHEN BANK 1 IS SELECTED
ADDRESSED INDIRECTLY THROUGH R1 OR R0 (R0' OR R1')
DIRECTLY ADDRESSABLE WHEN BANK 0 IS SELECTED

IN ADDITION R0 OR R1 (R0' OR R1') MAY BE USED TO ADDRESS 256 WORDS OF EXTERNAL RAM.

Functional Description
(Continued)

output line and input data must be valid at the trailing edge of $\overline{\text{RD}}$. When not being written or read, the BUS lines are in a high impedance state.

Test and INT Inputs

Three pins serve as inputs and are testable with the conditional jump instruction. These are T0, T1, and $\overline{\text{INT}}$. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. The T0, T1, and $\overline{\text{INT}}$ pins have other possible functions as well. See the pin description in page 3.

Program Counter and Stack

The Program Counter is an independent counter while the Program Counter Stack is implemented using pairs of registers in the Data Memory Array. Only 11 bits of the Program Counter are used to address the 2048 words of on-board program memory of the MBL80C49, while the most significant bits can be used for external Program Memory fetches. See Fig. 3. The Program Counter is initialized to zero by activating the Reset line.

An interrupt or CALL to a subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the Program Counter Stack as shown in Fig. 7. The pair to be used is determined by a 3-bit Stack Pointer which is part of the Program Status Word (PSW).

Data RAM locations 8–23 are available as stack registers and are used to store the Program Counter and 4 bits of PSW as shown in Fig. 7. The Stack Pointer when initialized to 000 points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transfered to locations 8 and 9 of the RAM array. The stack pointer is then incremented by one to point to locations 10 and 11 in anticipation of another CALL. Nesting of subroutines within subroutines can continue up to 8 times without oveflowing the stack.

If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

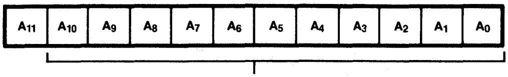
The end of a subroutine, which is signalled by a return instruction (RET or RETR), causes the Stack Pointer to be decremented and the contents of the resulting register pair to be transferred to the Program Counter.

Program Status Word

An 8-bit status word which can be loaded to and from the accumulator is called the Program Status Word (PSW). Fig. 5 shows the information available in the word. The Program Status Word is actually a collection of flip-flops throughout the machine which can be read or written as a whole. The ability to write to PSW allows for easy restoration of machine status after a power down sequence.

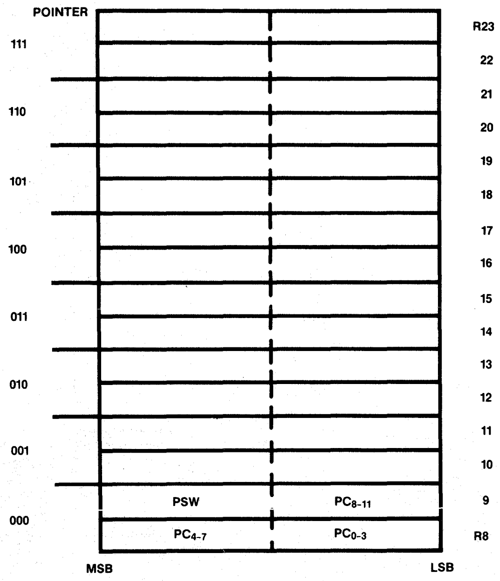
The upper four bits of PSW are stored in the Program Counter Stack with every call to subroutine or interrupt vector and are optionally restored upon return with the RETR instruction. The RET return instruction does not update PSW.

Figure 3. Program Counter



CONVENTIONAL PROGRAM COUNTER
*COUNTS 000H to 7FFH
*OVERFLOWS 7FFH TO 000H

Figure 4. Program Counter Stack



Functional Description
(Continued)

The PSW bit definitions are as follows:

Bits 0-2: Stack Pointer bits (S_0, S_1, S_2)

Bit 3: Not used ("1" level when read)

Bit 4: Working Register Bank Switch Bit (BS)
0 = Bank 0
1 = Bank 1

Bit 5: Flag 0 bit (F0) user controlled flag which can be complemented or cleared, and tested with the conditional jump instruction JF0.

Bit 6: Auxiliary Carry (AC) carry bit generated by an ADD instruction and used by the decimal adjust instruction DAA.

Bit 7: Carry (CY) carry flag which indicates that the previous operation has resulted in overflow of the accumulator.

Conditional Branch Logic

The conditional branch logic within the processor enables several conditions internal and external to the processor to be tested by the users program. By using the conditional jump instruction the conditions that are listed in Table 2 can effect a change in the sequence of the program execution.

Timer/Counter

The MBL80C49 contains a counter to aid the user in counting external events and generating accurate time delays without placing a burden on the processor for these functions. In both modes the counter operation is the same, the only difference being the source of the input to the counter. The timer/event counter is shown in Fig. 6.

Counter

The 8-bit binary counter is presettable and readable with two MOV instructions which transfer the contents of the accumulator to the counter and vice versa. The counter content may be affected by Reset and should be initialized by software. The counter is stopped by a Reset or STOP TCNT instruction and remains stopped until started as a timer by a START T instruction or as an event counter by a START CNT instruction. Once started the counter will increment to this maximum count (FF) and overflow to zero continuing its count until stopped by a STOP TCNT instruction or Reset.

The increment from maximum count to zero (overflow) results in the setting of an overflow flag flip-flop and in the generation of an interrupt request. The state of the overflow flag is testable with the conditional jump instruction JTF. The flag is reset by executing a JTF or by Reset. The interrupt request is stored in a latch and then ORed with the external interrupt input INT. The timer interrupt may be enabled or disabled independently of external interrupt by the EN TCNTI and DISTCNTI instructions. If enabled, the counter overflow will cause a subroutine call to location 7 where the timer or counter service routine may be stored.

If timer and external interrupts occur simultaneously, the external source will be recognized and the Call will be to location 3. Since the timer interrupt is latched it will remain pending until the external device is serviced and immediately be recognized upon return from the service routine. The pending timer interrupt is reset by the Call to location 7 or may be removed by executing a DIS TCNTI instruction.

As An Event Counter

Execution of a START CNT instruction connects the T1 input pin to the counter input and enables the counter. The T1 input is sampled at the beginning of state 3 or in state time 4. Subsequent high to low transistions on T1 will cause the counter to increment. T1 must be held low for at least 1 machine cycle to insure it won't be missed. The maximum

Figure 5. Program Status Word (PSW)

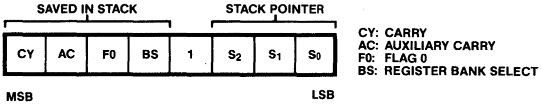


Figure 6. Timer/Event Counter

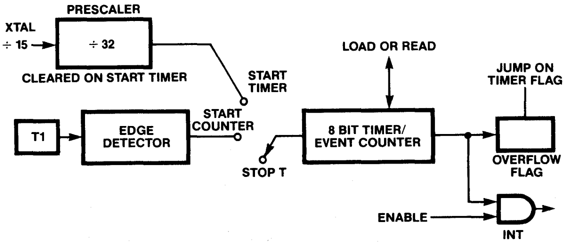


Table 2

Device Testable	Jump Conditions (Jump On)	
Accumulator	All zeros	Not all zeros
Accumulator Bit	—	1
Carry Flag	0	1
User Flags (F0, F1)	—	1
Timer Overflow Flag	—	1
Test Inputs (T0, $\overline{T1}$)	0	1
Interrupt Input ($\overline{INT}$)	0	—

Functional Description
(Continued)

rate at which the counter may be incremented is once per three instruction cycles (every 5.7 μsec when using an 8 MHz crystal)—there is no minimum frequency. T1 input must remain stable for at least 1/5 machine cycle after each transition.

As A Timer

Execution of a START T instruction connects an internal clock to the counter input and enables the counter. The internal clock is derived by passing the basic machine cycle clock through a ÷ 32 prescaler. The prescaler is reset during the START T instruction. The resulting clock increments the counter every 32 machine cycle. Various delays from 1 to 256 counts can be obtained by presetting the counter and detecting overflow. Times longer than 256 counts may be achieved by accumulating multiple overflows in a register under software control. For time resolution less than 1 count, an external clock can be applied to the T1 input and the counter operated in the event counter mode. ALE divided by 3 or more can serve as this external clock. Very small delays or "fine tuning" of larger delays can be easily accomplished by software delay loops.

Clock and Timing Circuits

Timing generation for the MBL80C49 is completely self-contained with the exception of a frequency reference which can be XTAL, ceramic resonator, or external clock source. The clock and Timing circuitry can be divided into the following functional blocks.

Oscillator

The on-board oscillator is a high gain parallel resonant circuit with a frequency range of 1 to 11 MHz. The X1 external pin is the input to the amplifier stage while X2 is the output. A crystal or ceramic resonator connected between X1 and X2 provides the feedback and phase shift required for oscillatin. If an accurate frequency reference is not required, ceramic resonator may be used in place of the crystal.

For accurate clocking a crystal should be used. An externally generated clock may also be applied to X1-X2 as the frequency source.

State Counter

The output of the oscillator is divided by 3 in the State counter to create a clock which defines the state times of the machine (CLK). CLK can be made available on the external pin T0 by executing an ENT0 CLK instruction. The output of CLK on T0 is disabled by Reset of the processor.

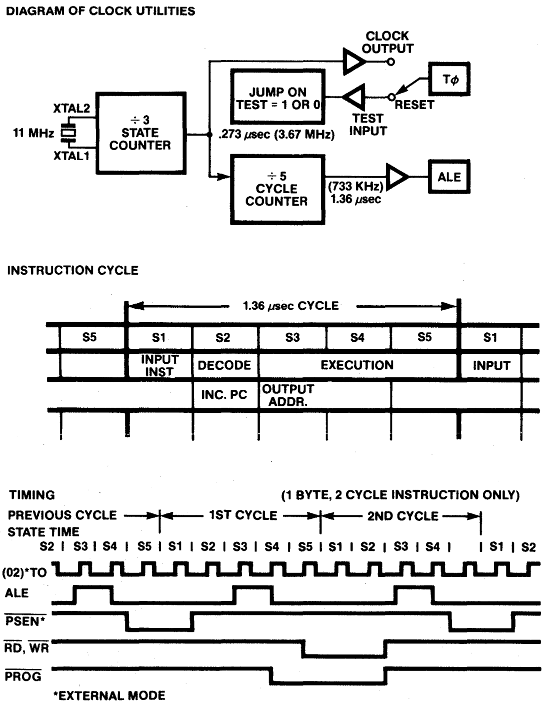
Cycle Counter

CLK is then divided by 5 in the Cycle Counter to provide a clock which defines a machine cycle consisting of 5 machine states as shown in Fig. 7. This clock is called Address Latch Enable (ALE) because of its function in MBL80C49 with external memory. It is provided continously on the ALE output pin.

Reset

The reset input provides a means for initialization for the processor. This Schmitt-trigger input has an internal pull-up device, which in combination with an external 1μfd capacitor, provides an internal reset pulse of sufficient length to guarantee all circuitry is reset, as shown in Fig. 8. If the reset pulse is generated externally the RESET pin must be held low for at least 10 milliseconds after the power supply is within tolerance. Only 5 machine cycles (6.8 μs @ 11 MHz) are required if power is already on and the oscillator has stablized. ALE and PSEN (if EA = 1) are active while in Reset.

Figure 7. Timing Generation and Cycle Timing



S5	S1	S2	S3	S4	S5	S1
	INPUT INST	DECODE	EXECUTION			INPUT
		INC. PC	OUTPUT ADDR.			

Functional Description
(Continued)

Reset performs the following functions:

1) Sets program counter to zero.
2) Sets stack pointer to zero.
3) Selects register bank 0.
4) Selects memory bank 0.
5) Sets BUS to high impedance state (except when EA = 5V).
6) Sets Ports 1 and 2 to input mode.
7) Disables interrupts (timer and external).
8) Stops timer.
9) Clears timer flag.
10) Clears F0 and F1.
11) Disables clock output from T0.

Interrupt

An interrupt sequence is initiated by applying a low ("0") level input to the INT pin. Interrupt is level triggered and active low to allow "WIRE ORing" of several interrupt sources at the input pin. Fig. 9 shows the interrupt logic of the MBL80C49. The interrupt line is sampled every instruction cycle and when detected causes a "call to subroutine" at location 3 in program memory as soon as all cycles of the current instruction are complete. On 2-cycle instructions, the interrupt line is sampled on the 2nd cycle only. $\overline{\text{INT}}$ must be held low for at least 3 machine cycles to ensure proper interrupt operations. As in any CALL to subroutine, the Program Counter and Program Status word are saved in the stack. For a description of this operation see the previous section, Program Counter and Stack. Program Memory location 3 usually contains an unconditional jump to an interrupt service subroutine elsewhere in program memory. The end of an interrupt service subroutine is signalled by the execution of a Return and Restore Status instruction RETR. The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of an RETR reenables the interrupt input logic. This occurs at the beginning of the second cycle of the RETR instruction. This sequence holds true also for an internal interrupt generated by timer overflow. If an internal timer/counter generated interrupt and an external interrupt are detected at the same time, the external source will be recognized. See the following Timer/Counter section for a description of timer interrupt. If needed, a second external interrupt can be created by enabling the timer/counter interrupt, loading FFH in the Counter (one less than terminal count), and enabling the event counter mode. A "1" to "0" transition on the T1 input will then cause an interrupt vector to location 7.

Interrupt Timing

The interrupt input may be enabled or disabled under Program Control using the EN I and DIS I instructions. Interrupts are disabled by Reset and remain so until enabled by the users program. An interrupt request must be removed before the RETR instruction is executed upon return from the service routine

Figure 8. Reset Circuit

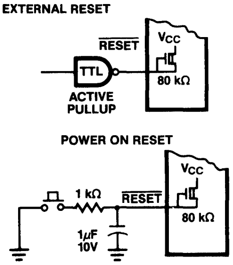
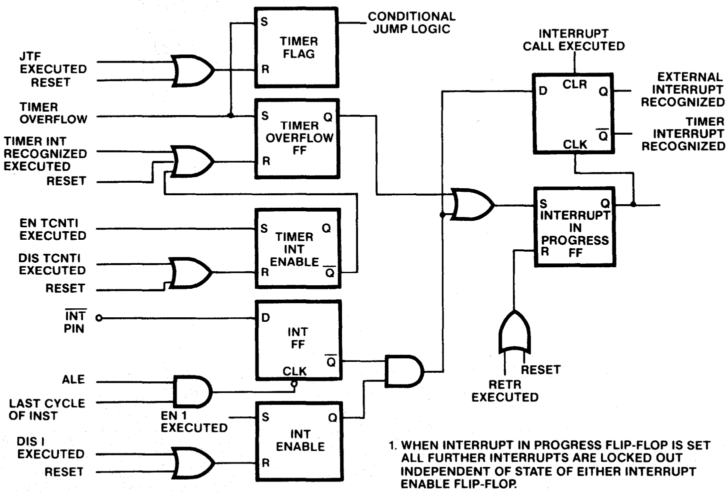


Figure 9. Interrupt Logic



1. WHEN INTERRUPT IN PROGRESS FLIP-FLOP IS SET ALL FURTHER INTERRUPTS ARE LOCKED OUT INDEPENDENT OF STATE OF EITHER INTERRUPT ENABLE FLIP-FLOP.
2. WHILE TIMER INTERRUPTS ARE DISABLED TIMER OVERFLOW f/f WILL NOT STORE ANY OVERFLOW THAT OCCURS. TIMER FLAG WILL BE SET, HOWEVER.

Functional Description
(Continued)

otherwise the processor will re-enter the service routine immediately. Many peripheral devices prevent this situation by resetting their interrupt request line whenever the processor accesses (Reads or Writes) the peripherals data buffer register. If the interrupting device does not require access by the processor, one output line of the MBL80C49 may be designated as an "interrupt acknowledge" which is activated by the service subroutine to reset the interrupt request. The $\overline{INT}$ pin may also be tested using the conditional jump instruction JNI. This instruction may be used to detect the presence of a pending interrupt before interrupts are enabled. If interrupt is left disabled $\overline{INT}$ may be used as another test input like T0 and T1.

Single-Step

This feature, as pictured in Fig. 10, provides the user with a debug capability in that the processor can be stepped through the program one instruction at a time. When stopped, the address of the next instruction to be fetched is available concurrently on BUS and the lower half of Port 2. The user can therefore follow the program through each of the instruction steps. A timing diagram, showing the interaction between output ALE and input $\overline{SS}$, is shown. The BUS buffer contents are lost during single step; however, a latch may be added to reestablish the lost I/O capability if needed. Data is valid at the leading edge of ALE.

Timing

The MBL80C49 operates in a single-step mode as follows:
1) The processor is requested to stop by applying a low level on $\overline{SS}$.
2) The processor responds by stopping during the address fetch portion of the next instruction. If a double cycle instruction is in progress when the single step command is received, both cycles will be completed before stopping.
3) The processor acknowledges it has entered the stopped state by raising ALE high. In this state (which can be maintained indefinitely) the address of the next instruction to be fetched is present on BUS and the lower half of port 2.
4) $\overline{SS}$ is then raised high to bring the processor out of the stopped mode allowing it to fetch the next instruction. The exit from stop is indicated by the processor bringing ALE low.
5) To stop the processor at the next instruction $\overline{SS}$ must be brought low again soon after ALE goes low. If $\overline{SS}$ is left high the processor remains in a "Run" mode.

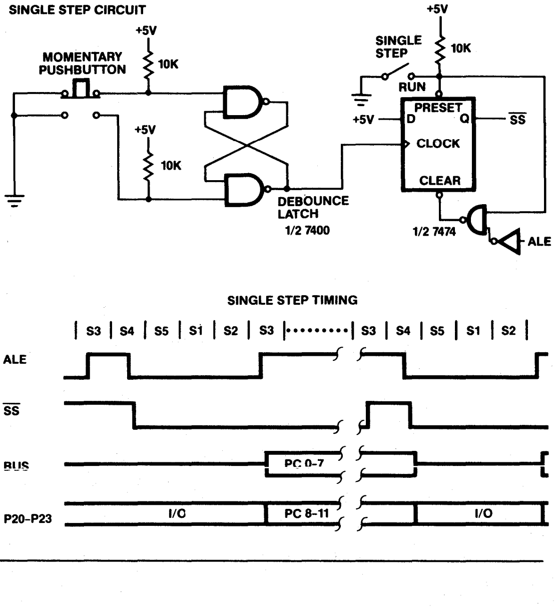
A diagram for implementing the single-step function of the MBL80C49 is shown in Fig. 10. A D-type flip-flop with preset and clear is used to generate $\overline{SS}$. In the run mode, $\overline{SS}$ is held high by keeping the flip-flop preset (preset has precedence over the clear input). To enter single step, preset is removed allowing ALE to bring $\overline{SS}$ low via the clear input. ALE should be buffered since the clear input of an SN7474 is the equivalent of 3 TTL loads. The processor is now in the stopped state. The next instruction is initiated by clocking a "1" into the flip-flop. This "1" will not appear on $\overline{SS}$ unless ALE is high, removing clear from the flip-flop. In response to $\overline{SS}$ going high the processor begins an instruction fetch which brings ALE low, resetting $\overline{SS}$ through the clear input and causing the processor to again enter the stopped state.

External Access Mode

Normally the first 2K words of program memory are automatically fetched from internal ROM. The EA input pin however allows the user to effectively disable internal program memory by forcing all program memory fetches to reference external memory. The following chapter explains how access to external program memory is accomplished.

The External Access mode is very useful in system test and debug because it allows the user to disable his internal applications program and substitute an external program of his choice—a diagnostic routine for instance. In addition, the section on Test

Figure 10. Single Step Operation


SINGLE STEP CIRCUIT

SINGLE STEP TIMING

Functional Description
(Continued)

and Debug explains how internal program memory can be read externally, independent of the processor. A "1" level on EA initiates the external access mode. For proper operation, Reset should be applied while the EA input is changed.

Low Power Standby Operation

MBL80C49 has two low-power standby modes, HALT and STOP modes. Both are initiated by software and are released by hardware.

Halt Mode

This mode is initiated by the HALT instruction (OP code: 01H). When the HALT instruction is executed, the device enters the HALT mode and stops executing instructions after that.

During the HALT mode all the other internal circuits stop, except the on-chip oscillator. The oscillator idles and the clock is inhibited to the internal circuits. This time the program counter holds the address next to the HALT instruction, and the internal RAM, internal registers, and flags keep the states executing the HALT instruction. The input/output ports hold the states shown below:

Type	Pin	State
Input	XTAL1, XTAL2, EA, $\overline{\text{RESET}}$, $\overline{\text{INT}}$, $\overline{\text{SR}}$	Active
	T1, $\overline{\text{SS}}$	Inactive
Output	$\overline{\text{RD}}$, $\overline{\text{WR}}$, PSEN, ALE	High Level
	P10-17, P20-27, DB0-DB7, T0, PROG	High Impedance

In this mode, the supply voltage, V_{CC} can be lowered to 3.5V, and the supply current reduced to 2mA for N version and 4mA for H version.

A negative pulse at one of $\overline{\text{RESET}}$, $\overline{\text{INT}}$, and $\overline{\text{SR}}$ inputs releases the device from the HALT mode. When a pulse is applied, the device restarts executing instructions from an address shown below, depending on the applied pin. Before applying the negative pulse, the supply voltage must be returned to the value (+5V ±10%) to guarantee normal operation.

$\overline{\text{RESET}}$ (Low level sense):

A negative pulse with minimum 12 instruction cycle width is needed for the standby release. The low level releases the device from the standby state, and initializes the device to the reset state. Approximately 8200 instruction cycles later $\overline{\text{RESET}}$ returns to high and the device restarts the execution from address #0.

$\overline{\text{INT}}$ (Low level sense):

The low level releases the device from the standby state, and after a dummy cycle of approximately 5 instruction cycles the device restarts the execution from an address next to the HALT instruction executed. If the external interrupt is enabled, the control jumps at address #3 after executing the instruction next to the HALT instruction executed. The $\overline{\text{INT}}$ pulse must be kept low until the interrupt is accepted.

$\overline{\text{SR}}$ (Low level sense):

A negative pulse with minimum 2 instruction cycle is required for the standby release. The low level releases the device from the standby state, and after a dummy cycle of approximately 5 instruction cycles the device restarts the execution from an address next to the HALT instruction executed.

Stop Mode

This mode is initiated by the STOP instruction (OP code: C1H). When the STOP instruction is executed, the device enters the STOP mode and stops executing instructions after that.

During the STOP mode all the internal circuits stop. Only the internal RAM is retained. The internal registers and flags are not kept. The input/output ports hold the states shown below:

Type	Pin	State
Input	EA, $\overline{\text{RESET}}$, $\overline{\text{INT}}$, $\overline{\text{SR}}$	Active
	XTAL1, XTAL2, T1, $\overline{\text{SS}}$	Inactive
Output	$\overline{\text{RD}}$, $\overline{\text{WR}}$, PSEN, ALE	High Level
	P10-17, P20-27, DB0-DB7, T0, PROG	High Impedance

In this mode, the supply voltage, V_{CC} can be lowered to 2.0V, and the supply current reduced to 50μA.

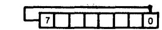
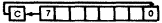
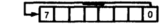
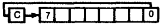
A negative pulse at $\overline{\text{RESET}}$ input releases the device from the STOP mode. When a $\overline{\text{RESET}}$ pulse is applied, the device restarts executing instructions from an address #0. Before applying the negative pulse,the supply voltage must be returned to the value (+5V ±10%) to guarantee normal operation.

$\overline{\text{RESET}}$ (Low level sense):

A negative pulse with minimum 12 instruction cycle width is needed for the standby release. The low level releases the device from the standby state, and initializes the device to the reset state. Approximately 8200 instruction cycles after $\overline{\text{RESET}}$ returns to high, the device restarts the execution from address #0.

Instruction Set Summary†

Accumulator and Memory Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Add Register to A	ADD A, Rr	6X	1	1	*	*	—	—	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	*	*	—	—	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	*	*	—	—	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	*	*	—	—	(A) ← (A) + data
Add register to A with carry	ADDC A, Rr	7X	1	1	*	*	—	—	(A) ← (A) + (Rr) + (C)
Add data memory to A with carry	ADDC A, @R0	70	1	1	*	*	—	—	(A) ← (A) + ((R0)) + (C)
	ADDC A, @R1	71	1	1	*	*	—	—	(A) ← (A) + ((R1)) + (C)
Add immediate to A with carry	ADDC A, #data	13	2	2	*	*	—	—	(A) ← (A) + data + (C)
And register to A	ANL A, Rr	5X	1	1	—	—	—	—	(A) ← (A) ∩ (Rr)
And data memory to A	ANL A, @R0	50	1	1	—	—	—	—	(A) ← (A) ∩ ((R0))
	ANL A, @R1	51	1	1	—	—	—	—	(A) ← (A) ∩ ((R1))
And immediate to A	ANL A, #data	53	2	2	—	—	—	—	(A) ← (A) ∩ data
Clear A	CLR A	27	1	1	—	—	—	—	(A) ← 0
Complement A	CPL A	37	1	1	—	—	—	—	(A) ← (A)
Decimal Adjust A	DA A	57	1	1	*	—	—	—	(Note 1)
Decrement A	DEC A	07	1	1	—	—	—	—	(A) ← (A) - 1
Increment A	INC A	17	1	1	—	—	—	—	(A) ← (A) + 1
Or register to A	ORL A, Rr	4X	1	1	—	—	—	—	(A) ← (A) ∪ (Rr)
Or data memory to A	ORL A, @R0	40	1	1	—	—	—	—	(A) ← (A) ∪ ((R0))
	ORL A, @R1	41	1	1	—	—	—	—	(A) ← (A) ∪ ((R1))
Or immediate to A	ORL A, #data	43	2	2	—	—	—	—	(A) ← (A) ∪ data
Rotate A left	RL A	E7	1	1	—	—	—	—	
Rotate A left through carry	RLC A	F7	1	1	*	—	—	—	
Rotate A right	RR A	77	1	1	—	—	—	—	
Rotate A right through carry	RRC A	67	1	1	*	—	—	—	
SWAP nibbles of A	SWAP A	47	1	1	—	—	—	—	$(A_{4\sim7}) \rightleftarrows (A_{0\sim3})$
Exclusive Or register to A	XRLA, Rr	DX	1	1	—	—	—	—	(A) ← (A) + (Rr)
Exclusive Or data memory to A	XRL A, @R0	D0	1	1	—	—	—	—	(A) ← (A) + ((R0))
	XRL A, @R1	D1	1	1	—	—	—	—	(A) ← (A) + ((R1))
Exclusive Or immediate to A	XRL A, #data	D3	2	2	—	—	—	—	(A) ← (A) + data

†Mnemonic copyright Intel Corporation 1983. (except HALT and STOP)
Operation Code X: See Tables 1 and 2.
%: See Table 3.
Flags*: This flag is set or reset in the state after executed instruction.
Z: This flag is reset.
CP: This flag is complemented.
Note: (1) The accumulator value is adjusted to form BCD digits following the binary addition of BCD number.

Instruction Set Summary
(Continued)

Input/Output Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
And immediate to BUS	ANL BUS, #data	98	2	2	—	—	—	—	(BUB) ← (BUS) ∩ data
And immediate to P1	ANL P1, #data	99	2	2	—	—	—	—	(P1) ← (P1) ∩ data
And immediate to P2	ANL P2, #data	9A	2	2	—	—	—	—	(P2) ← (P2) ∩ data
And A to Expander Port	ANLD P_P, A	9X	1	2	—	—	—	—	(P_P) ← (P_P) ∩ (A3~0)
Input BUS to A	INS A, BUS	08	1	2	—	—	—	—	(A) ← (BUS)
Input P1 to A	IN A, P1	09	1	2	—	—	—	—	(A) ← (P1)
Input P2 to A	IN A, P2	0A	1	2	—	—	—	—	(A) ← (P2)
Input Expander Port to A	MOVD A, P_P	0X	1	2	—	—	—	—	(A3~0) ← (P_P), (A7~4) ← 0
Or immediate to BUS	ORL BUS, #data	88	2	2	—	—	—	—	(BUS) ← (BUS) ∪ data
Or immediate to P1	ORL P1, #data	89	2	2	—	—	—	—	(P1) ← (P1) ∪ data
Or immediate to P2	ORL P2, #data	8A	2	2	—	—	—	—	(P2) ← (P2) ∪ data
Or A to Expander Port	ORLD P_P, A	8X	1	2	—	—	—	—	(P_P) ← (P_P) ∪ (A3~0)
Output A to BUS	OUTL BUS, A	02	1	2	—	—	—	—	(BUS) ← (A)
Output A to P1	OUTL P1, A	39	1	2	—	—	—	—	(P1) ← (A)
Output A to P2	OUTL P2, A	3A	1	2	—	—	—	—	(P2) ← (A)
Output A to Expander Port	MOVD P_P, A	3X	1	2	—	—	—	—	(P_P) ← (A3~0)

Data Move Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Move register to A	MOV A, Rr	FX	1	1	—	—	—	—	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	—	—	—	—	(A) ← ((R0))
	MOV A, @R1	F1	1	1	—	—	—	—	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	—	—	—	—	(A) ← data
Move A to register	MOV Rr, A	AX	1	1	—	—	—	—	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	—	—	—	—	((R0)) ← (A)
	MOV @R1, A	A1	1	1	—	—	—	—	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX	2	2	—	—	—	—	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	—	—	—	—	((R0)) ← data
	MOV @R1, #data	B1	2	2	—	—	—	—	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	—	—	—	—	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*	*	*	—	(PSW) ← (A)
Move external data memory to A	MOVX A, @R0	80	1	2	—	—	—	—	(A) ← ((R0))
	MOVX A, @R1	81	1	2	—	—	—	—	(A) ← ((R1))
Move A to external data memory	MOVX @R0, A	90	1	2	—	—	—	—	((R0)) ← (A)
	MOVX @R1, A	91	1	2	—	—	—	—	((R1)) ← (A)
Move to A from current page	MOVP A, @A	A3	1	2	—	—	—	—	(PC7~0) ← (A), (A) ← ((PC))
Move to A from page 3	MOVP3 A, @A	E3	1	2	—	—	—	—	(PC7~0) ← (A), (PC11~8) ← 3, (A) ← ((PC))
Exchange A and register	XCH A, Rr	2X	1	1	—	—	—	—	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	—	—	—	—	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	—	—	—	—	(A) ⇄ ((R1))
Exchange nibble of A and data memory	XCHD A, @R0	30	1	1	—	—	—	—	(A3~0) ⇄ ((R0)3~0)
	XCHD A, @R1	31	1	1	—	—	—	—	(A3~0) ⇄ ((R1)3~0)

Instruction Set Summary
(Continued)

Branch and Jump Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Decrement register and test	DJNZ Rr, addr	EX	2	2	—	—	—	—	(Rr) ≠ 0 Note (1)
Jump unconditional	JMP addr	%4	2	2	—	—	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	—	—	Unconditional Branch Note (2)
Jump on carry = 1	JC addr	F6	2	2	—	—	—	—	(C) = 1
Jump on carry = 0	JNC addr	E6	2	2	—	—	—	—	(C) = 0
Jump on A zero	JZ addr	C6	2	2	—	—	—	—	(A) = 0
Jump on A no zero	JNZ addr	96	2	2	—	—	—	—	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	—	—	—	—	(T0) = 1
Jump on T0 = 0	JNT0 addr	26	2	2	—	—	—	—	(T0) = 0
Jump on T1 = 1	JT1 addr	56	2	2	—	—	—	—	(T1) = 1
Jump on T1 = 0	JNT1 addr	46	2	2	—	—	—	—	(T1) = 0
Jump on F0 = 1	JF0 addr	B6	2	2	—	—	—	—	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	—	—	—	—	(F1) = 1
Jump on timer flag, Clear flag	JTF addr	16	2	2	—	—	—	—	(TF) = 1
Jump on $\overline{\text{INT}}$ = 0	JNI addr	86	2	2	—	—	—	—	($\overline{\text{INT}}$) = 0
Jump on accumulator bit	JBb addr	%2	2	2	—	—	—	—	(Ab) = 1

Subroutine Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Jump to subroutine	CALL addr	%4	2	2	—	—	—	—	Note (3)
Return	RET	83	1	2	—	—	—	—	Note (4)
Return and restore status	RETR	93	1	2	*	*	*	—	Note (5)

Flags Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Clear carry	CLR C	97	1	1	Z	—	—	—	(C) ← 0
Complement carry	CPL C	A7	1	1	CP	—	—	—	(C) ← ($\overline{C}$)
Clear flag 0	CLR F0	85	1	1	—	—	Z	—	(F0) ← 0
Complement flag 0	CPL F0	95	1	1	—	—	CP	—	(F0) ← ($\overline{F0}$)
Clear flag 1	CLR F1	A5	1	1	—	—	—	Z	(F1) ← 0
Complement flag 1	CPL F1	B5	1	1	—	—	—	CP	(F1) ← ($\overline{F1}$)

(1) DJNZ Rr, Addr: (Rr) - 1 → (Rr)
if (Rr) ≠ 0, addr → (PC_0 to PC_7).
if (R_r) = 0, execute next instruction.
(2) JMPP @ A: ((A)) → (PC_0 to PC_7)

Register Instructions

		OP			Flag				
Operation	**Mnemonic**	**Code**	**Byte**	**Cycle**	**CY**	**HC**	**F_0**	**F_1**	**Note**
Decrement register	DEC Rr	CX	1	1	—	—	—	—	(Rr) ← (Rr) - 1
Increment register	INC Rr	1X	1	1	—	—	—	—	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	—	—	—	—	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	—	—	—	—	((R1)) ← ((R1)) + 1

Instruction Set Summary
(Continued)

Timer/Counter Instructions

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Disable Timer/ Counter Interrupt	DIS TCNTI	35	1	1	—	—	—	—	
Enable Timer/ Counter Interrupt	EN TCNTI	25	1	1	—	—	—	—	
Read Timer/Counter	MOV A, T	42	1	1	—	—	—	—	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	—	—	—	—	(T) ← (A)
Start Timer	STRT T	55	1	1	—	—	—	—	
Start Counter	STRT CNT	45	1	1	—	—	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	—	—	

Control Instructions

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Disable external Interrupt	DIS I	15	1	1	—	—	—	—	
Enable external Interrupt	EN I	05	1	1	—	—	—	—	
Enable Clock output on T0	ENT0 CLK	75	1	1	—	—	—	—	
No Operation	NOP	00	1	1	—	—	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	—	—	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	—	—	—	—	(BS) ← 1
Select memory bank 0	SEL MB0	E5	1	1	—	—	—	—	(MBF) ← 0
Select memory bank 1	SEL MB1	F5	1	1	—	—	—	—	(MBF) ← 1

Standby Instructions

Operation	Mnemonic	OP Code	Byte	Cycle	Flag CY	HC	F_0	F_1	Note
Halt	HALT	01	1	1	—	—	—	—	
Stop	STOP	C1	1	1	—	—	—	—	

Instruction Set Summary
(Continued)

Table 1. O.P. Code of Register Access Instruction

Mnemonic	Rr	R0	R1	R2	R3	R4	R5	R6	R7
INC Rr		18	19	1A	1B	1C	1D	1E	1F
XCH A, Rr		28	29	2A	2B	2C	2D	2E	2F
ORL A, Rr		48	49	4A	4B	4C	4D	4E	4F
ANL A, Rr		58	59	5A	5B	5C	5D	5E	5F
ADD A, Rr		68	69	6A	6B	6C	6D	6E	6F
ADDC A, Rr		78	79	7A	7B	7C	7D	7E	7F
MOV Rr, A		A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data		B8	B9	BA	BB	BC	BD	BE	BF
DEC Rr		C8	C9	CA	CB	CC	CD	CE	CF
XRL A, Rr		D8	D9	DA	DB	DC	DD	DE	DF
DJNZ Rr, M		E8	E9	EA	EB	EC	ED	EE	EF
MOV A, Rr		F8	F9	FA	FB	FC	FD	FE	FF

7	6	5	4	3	2	1	0
					r_2	r_1	r_0

Table 2. OP Code Of Expander Port Instruction

Mnemonic	P_P	P4	P5	P6	P7
MOVD A.P_P		0C	0D	0E	0F
MOVD P_P, A		3C	3D	3E	3F
ORLD P_P, A		8C	8D	8E	8F
ANLD P_P, A		9C	9D	9E	9F

7	6	5	4	3	2	1	0
						P_1	P_0

OP Code of JMP/CALL/JB$_b$

	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
JMP	A_H			0	0	1	0	0	A_L							
	First Byte								Second Byte							
CALL	A_H			1	0	1	0	0	A_L							
	First Byte								Second Byte							
JB$_b$	B_b			1	0	0	1	0	A_L							
	First Byte								Second Byte							

A_L: Address A_7 to A_0
A_H: Address A_{10}, A_9, A_8
B_b: b-th Bit on Accumulator

Notes:

(3) CALL addr:
(PC_0 to PC_7) → ((SP))
(PC_8 to PC_{11}), (MBF), (PSW_5 to PSW_7) → ((SP))
(SP) + 1 → (SP)
A_L → (PC_0 to PC_7)
A_H → (PC_8 to PC_{10})
MBF → (PC_{11})

(4) RET:
(SP) - 1 → (SP)
((SP)) → (PC_0 to PC_7), (PC_8 to PC_{11})

(5) RETR:
(SP) -1 → (SP)
$((SP))_0$ to $(SP)_3$ → (PC_8 to PC_{11})
$((SP))_4$ to $(SP)_7$ → (PSW_4 to PSW_7)
((SP)) → (PC_0 to PC_7), (PC_8 to PC_{11})
((SP)) → (PSW_5 to PSW_7), (MBF)

Instruction Codes

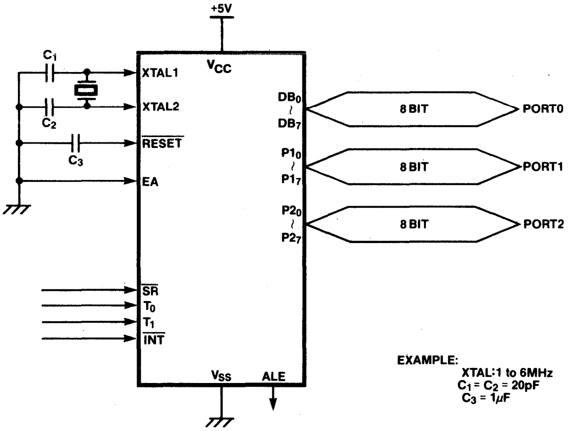
L H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	HALT	◤ OUT (BSU, A)	ADD ◥ (A,#)	JMP ◥ 0	EN I		DEC (A)	◤ INS (A,BUS)	◤ IN (A,P1)	◤ IN (A,P2)		◤ MOVD (A,P4)	◤ MOVD (A,P5)	◤ MOVD (A,P6)	◤ MOVD (A,P7)
1	INC @R0	INC @R1	JB ◥ 0	ADDC ◥ (A,#)	CALL ◥ 0	DIS I	JTF ◥	INC (A)	INC (R0)	INC (R1)	INC (R2)	INC (R3)	INC (R4)	INC (R5)	INC (R6)	INC (R7)
2	XCH (A,@R0)	XCH (A,@R1)		MOV ◥ (A,#)	JMP ◥ 1	EN TCNTI	JNT0 ◥	CLR (A)	XCH (A,R0)	XCH (A,R1)	XCH (A,R2)	XCH (A,R3)	XCH (A,R4)	XCH (A,R5)	XCH (A,R6)	XCH (A,R7)
3	XCHD (A, @ R0)	XCHD (A, @ R1)	JB ◥ 1		CALL ◥ 1	DIS TCNTI	JT0 ◥	CPL (A)		◤ OUTL (P1,A)	◤ OUTL (P2,A)		◤ MOVD (P4,A)	◤ MOVD (P5,A)	◤ MOVD (P6,A)	◤ MOVD (P7,A)
4	ORL (Ac@R0)	ORL (A, @R1)	MOV (A,T)	ORL ◥ (A,#)	JMP ◥ 2	STRT CNT	JNT1 ◥	SWAP (A)	ORL (A,R0)	ORL (A,R1)	ORL (A,R2)	ORL (A,R3)	ORL (A,R4)	ORL (A,R5)	ORL (A,R6)	ORL (A,R7)
5	ANL (A,@R0)	ANL (A,@R1)	JB ◥ 2	ANL ◥ (A,#)	CALL ◥ 2	STRT T	JT1 ◥	DA (A)	ANL (A,R0)	ANL (A,R1)	ANL (A,R2)	ANL (A,R3)	ANL (A,R4)	ANL (A,R5)	ANL (A,R6)	ANL (A,R7)
6	ADD (A,@R0)	ADD (A,@R1)	MOV (T,A)		JMP ◥ 3	STOP TCNT		RRC (A)	ADD (A,R0)	ADD (A,R1)	ADD (A,R2)	ADD (A,R3)	ADD (A,R4)	ADD (A,R5)	ADD (A,R6)	ADD (A,R7)
7	ADDC (A,@R0)	ADDC (A,@R1)	JB ◥ 3		CALL ◥ 3	ENT0 CLK	JF1 ◥	RR (A)	ADDC (A,R0)	ADDC (A,R1)	ADDC (A,R2)	ADDC (A,R3)	ADDC (A,R4)	ADDC (A,R5)	ADDC (A,R6)	ADDC (A,R7)
8	◤ MOVX (A,@R0)	◤ MOVX (A,@R1)		◤ RET	JMP ◥ 4	CLR F0	JNI ◥		ORL ◥ (BUS,#)	ORL ◥ (P1,#)	ORL ◥ (P2,#)		◤ ORLD (P4,A)	◤ ORLD (P5,A)	◤ ORLD (P6,A)	◤ ORLD (P7,A)
9	◤ MOVX (@R0,A)	◤ MOVX (@R1,A)	JB ◥ 4	◤ RETR	CALL ◥ 4	CPL F0	JNZ ◥	CLR C	ANL ◥ (BUS,#)	ANL ◥ (P1,#)	ANL ◥ (P2,#)		◤ ANLD (P4,A)	◤ ANLD (P5,A)	◤ ANLD (P6,A)	◤ ANLD (P7,A)
A	MOV (@R0,A)	MOV (@R1,A)		◤ MOVP (A,@A)	JMP ◥ 5	CLR F1		CPL C	MOV (R0,A)	MOV (R1,A)	MOV (R2,A)	MOV (R3,A)	MOV (R4,A)	MOV (R5,A)	MOV (R6,A)	MOV (R7,A)
B	MOV (@R0,#)	MOV (@R1,#)	JB ◥ 5	◤ JMPP (@A)	CALL ◥ 5	CPL F1	JF0 ◥		MOV ◥ (R0,#)	MOV ◥ (R1,#)	MOV ◥ (R2,#)	MOV ◥ (R3,#)	MOV ◥ (R4,#)	MOV ◥ (R5,#)	MOV ◥ (R6,#)	MOV ◥ (R7,#)
C		STOP			JMP ◥ 6	SEL RB0	JZ ◥	MOV (A,PSW)	DEC (R0)	DEC (R1)	DEC (R2)	DEC (R3)	DEC (R4)	DEC (R5)	DEC (R6)	DEC (R7)
D	XRL (A,@R0)	XRL (A,@R1)	JB ◥ 6	XRL ◥ (A,#)	CALL ◥ 6	SEL RB1		MOV (PSW,A)	XRL (A,R0)	XRL (A,R1)	XRL (A,R2)	XRL (A,R3)	XRL (A.R4)	XRL (A,R5)	XRL (A,R6)	XRL (A,R7)
E				◤ MOVP3 (A,@A)	JMP ◥ 7	SEL MB0	JNC ◥	RL (A)	DJNZ ◥ (R0,M)	DJNZ ◥ (R1,M)	DJNZ ◥ (R2,M)	DJNZ ◥ (R3,M)	DJNZ ◥ (R4,M)	DJNZ ◥ (R5,M)	DJNZ ◥ (R6,M)	DJNZ ◥ (R7,M)
F	MOV (A,@R0)	MOV (A,@R1)	JB ◥ 7		CALL ◥ 7	SEL MB1	JC ◥	RLC (A)	MOV (A,R0)	MOV (A,R1)	MOV (A,R2)	MOV (A,R3)	MOV (A,R4)	MOV (A,R5)	MOV (A,R6)	MOV (A,R7)

#: Immediate data
H; Higher 4 Bits
L; Lower Bits

□	1 Byte, 1 Cycle Instruction
◤	1 Byte, 2 Cycles Instruction
◥	2 Byte, 2 Cycles Instruction

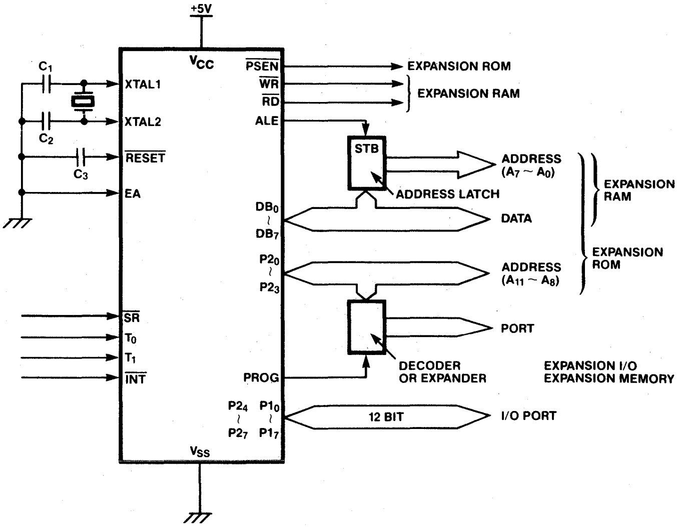
Typical Application

Figure 15. Stand Alone System



EXAMPLE:
XTAL:1 to 6MHz
$C_1 = C_2 = 20pF$
$C_3 = 1\mu F$

Figure 16. Expanded System



Absolute Maximum Ratings

Parameter	Symbol	Value Min.	Value Max.	Unit
Supply Voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 7.0	V
Input Voltage	V_{IN}	V_{SS} - 0.3	V_{CC} + 0.3	
Output Voltage	V_{OUT}	V_{SS} - 0.3	V_{CC} + 0.3	
Power Dissipation	P_D	—	600	mW
Operating Temperature	T_A*	-40	+85	°C
Storage Temperature	T_{STG}	-55	+150	

Note:
*T_A = 0°C to 70°C for H version.
**Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit	Note	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active Mode (Normal Operation)	
		3.5		6.0		Standby Mode	All internal states are retained
		2.0		6.0			Only internal RAM data are retained
	V_{SS}		0				
Operating Temperature	T_A	-40		+85	°C	MBL80C49N/C39N	
		0		+70		MBL80C49H/C39H	

DC Characteristics

Recommended operating conditions, unless otherwise noted.

(T_A = -40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V for MBL80C49N/MBL80C39N)
(T_A = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V for MBL80C49H/MBL80C39H)

	Applicable		Value			
Parameter	**Pin/Device**	**Symbol**	**Min.**	**Max.**	**Unit**	**Test Conditions**
Input Low Voltage	All except XTAL1, XTAL2, $\overline{\text{RESET}}$	V_{IL}	-0.3	0.8	V	
	XTAL1, XTAL2, $\overline{\text{RESET}}$	V_{IL1}	-0.3	0.6	V	
Input High Voltage	All except XTAL1, XTAL2, $\overline{\text{RESET}}$	V_{IH}	2.2	V_{CC}	V	
	XTAL1, XTAL2, $\overline{\text{RESET}}$	V_{IH1}	3.8	V_{CC}	V	
Output Low Voltage	BUS	V_{OL}		0.45	V	I_{OL} = 2.0mA
	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE	V_{OL1}		0.45	V	I_{OL} = 2.0mA
	PROG	V_{OL2}		0.45	V	I_{OL} = 1.0mA
	All Other Outputs	V_{OL3}		0.45	V	I_{OL} = 1.6mA
Output High Voltage	BUS	V_{OH}	2.4		V	I_{OH} = -400μA
	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE, PROG, T0	V_{OH1}	2.4		V	I_{OH} = -100μA
	P10-P17, P20-P27	V_{OH2}	2.4		V	I_{OH} = -40μA
Input Leakage Current	$\overline{\text{RESET}}$, $\overline{\text{SS}}$, $\overline{\text{SR}}$	I_{LI}		-100	μA	V_{SS} + 0.45≦V_{IN}≦V_{CC}
	T1, $\overline{\text{INT}}$, EA	I_{LI1}		±10	μA	V_{SS}≦V_{IN}≦V_{CC}
	P10-P17, P20-P27	I_{LI2}		-200	μA	V_{SS} + 0.45≦V_{IN}≦V_{CC}
Output Leakage Current	BUS, T0	I_{LO}		±10	μA	V_{SS} + 0.45≦V_{IN}≦V_{CC} High-Impedance Mode
Standby Supply Current	MBL80C49N/C39N	I_{CCH}		2	mA	V_{CC} = 3.5V, 6MHz, HALT Mode
	MBL80C49H/C49H	I_{CCH}		4	mA	V_{CC} = 3.5V, 11MHz, HALT Mode
	MBL80C49N/H, MBL80C39N/H	I_{CCS}		50	μA	V_{CC} = 2.0V, STOP Mode
Active Supply Current	MBL80C49N/C39N	I_{CC}		10	mA	All Outputs Open
	MBL80C49H/C39H	I_{CC}		18	mA	All Outputs Open

AC Characteristics

Recommended operating conditions, unless otherwise noted.

(T_A = -40°C to +85°C, V_{CC} = +5V ±10%, V_{SS} = 0V for MBL80C49N/MBL80C39N)
(T_A = 0°C to +70°C, V_{CC} = +5V ±10%, V_{SS} = 0V for MBL80C49H/MBL80C39H)

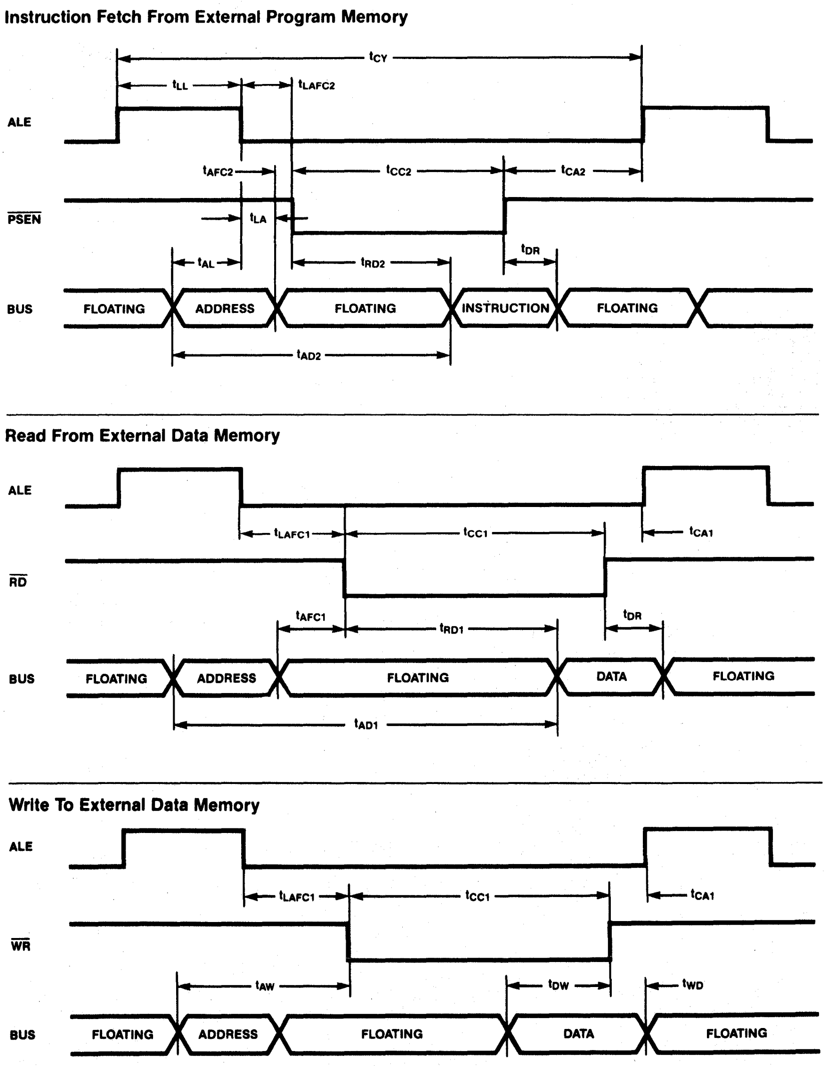
		MBL80C49H/C39H		MBL80C49N/C39N			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Test Conditions**
ALE Pulse Width	t_{LL}	150		410		ns	Note 1
Address Setup Time (to ALE↓)	t_{AL}	70		230		ns	
Address Hold Time (from ALE↓)	t_{LA}	50		120		ns	
$\overline{RD}$ & $\overline{WR}$ Pulse Width	t_{CC1}	480		1050		ns	
$\overline{PSEN}$ Pulse Width	t_{CC2}	350		800		ns	
Data Setup Time (to $\overline{WR}$↑)	t_{DW}	390		880		ns	
Data Hold Time (from $\overline{WR}$↑)	t_{WD}	40		120		ns	Note 2
Data Hold Time (from $\overline{RD}$↑, $\overline{PSEN}$↑)	t_{DR}	0	110	0	220	ns	Note 1
Data Delay Time (from $\overline{RD}$↓)	t_{RD1}		350		800	ns	
Data Delay Time (from $\overline{PSEN}$↓)	t_{RD2}		210		550	ns	
Address Setup Time (to $\overline{WR}$↓)	t_{AW}	310		680		ns	
Data Delay Time ($\overline{RD}$)	t_{AD1}		760		1590	ns	
Data Delay Time ($\overline{PSEN}$)	t_{AD2}		480		1090	ns	
Address Floating Time (to $\overline{RD}$↓, $\overline{WR}$↓)	t_{AFC1}	140		290		ns	
Address Floating Time (to $\overline{PSEN}$↓)	t_{AFC2}	10		40		ns	
$\overline{RD}$, $\overline{WR}$ Output Delay Time (from ALE↓)	t_{LAFC1}	200		420		ns	
$\overline{PSEN}$ Output Delay Time (from ALE↓)	t_{LAFC2}	60		170		ns	
ALE Delay Time (from $\overline{RD}$↑, $\overline{WR}$↑, PROG↑)	t_{CA1}	50		120		ns	
ALE Delay Time (from $\overline{PSEN}$↑)	t_{CA2}	320		620		ns	
Port Control Setup Time (to PROG↓)	t_{CP}	100		250		ns	
Port Control Hold Time (from PROG↓)	t_{PC}	160		460		ns	
Port 2 Input Data Delay Time (from PROG↓)	t_{PR}		700		1380	ns	
Port 2 Input Data Hold Time (from PROG↑)	t_{PF}	0	140	0	250	ns	
Output Data Setup Time (to PROG↑)	t_{DP}	400		850		ns	
Output Data Hold Time (from PROG↑)	t_{PD}	90		200		ns	
PROG Pulse Width	t_{PP}	700		1500		ns	
Port 2 I/O Data Setup Time (to ALE↑)	t_{PL}	160		460		ns	
Port 2 I/O Data Hold Time (from ALE↑)	t_{LP}	40		80		ns	
Port Data Output Time (from ALE↓)	t_{PV}		510		850	ns	
Cycle Time	t_{CY}	1.36		2.5		μs	
T0 Output Frequency	t_{OPRR}	270		500		ns	

Notes:
1. Load Conditions: BUS: C_L = 150pF, Other Outputs: C_L = 80pF, 1TTL
2. Load Conditions: BUS: C_L = 20pF, High impedance

↓: Falling edge
↑: Rising edge

Timing Diagram

Figure 11. Timing Diagram (1)



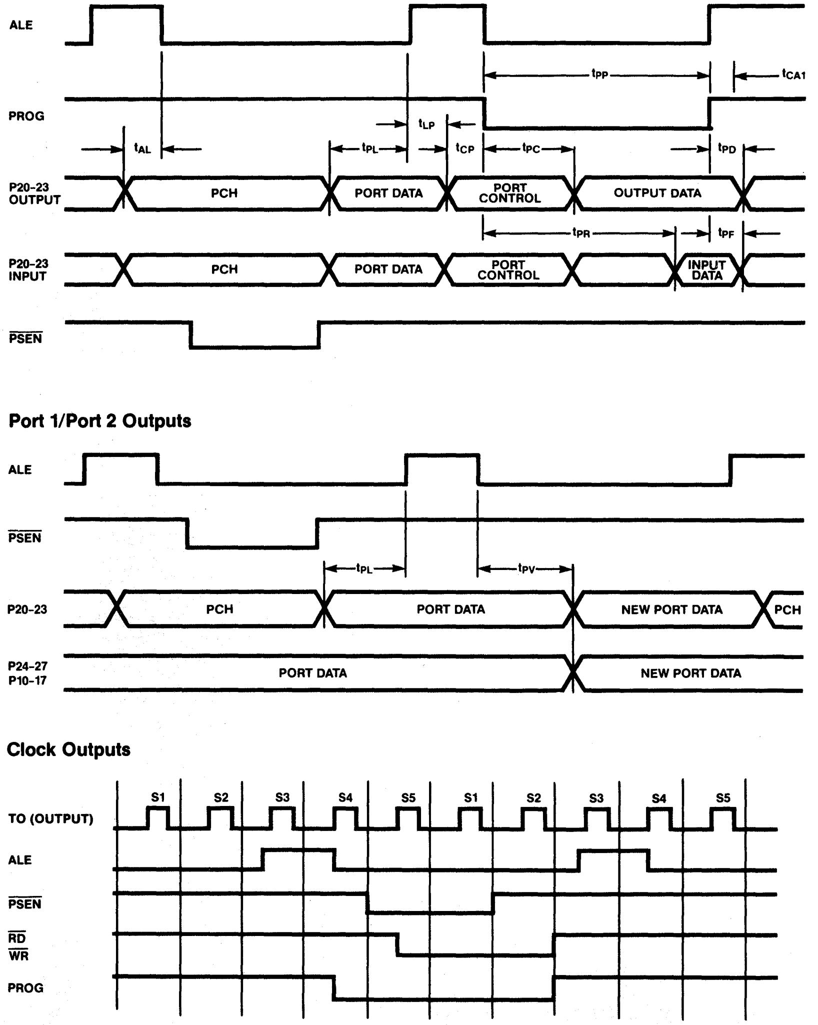
Instruction Fetch From External Program Memory

Read From External Data Memory

Write To External Data Memory

Timing Diagram
(Continued)

Figure 12. Timing Diagram (2)



P20-P23 Input/Output for Use of External Program Memory and Expander I/O Port

Port 1/Port 2 Outputs

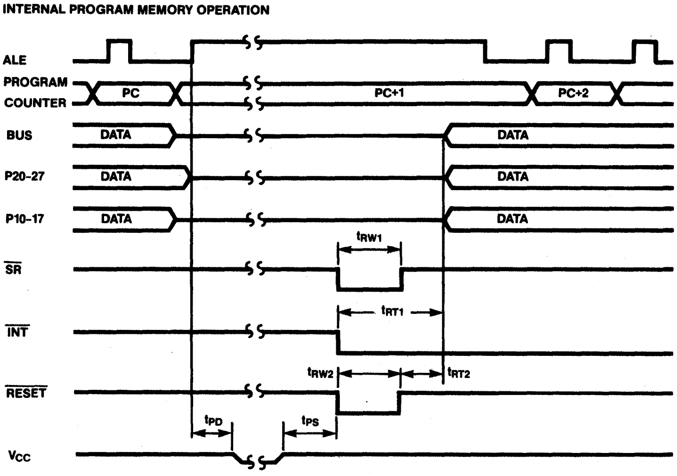
Clock Outputs

AC Characteristics for Standby Operation

Parameter		Symbol	Value		
			Min.	Typ.	Max.
Standby Release Pulse Width	$\overline{SR}$	t_{RW1}	2 · t_{CY}	—	—
	$\overline{RESET}$	t_{RW2}	12 · t_{CY}	—	—
Standby Release Time		t_{RT1}	4 · t_{CY}	5 · t_{CY}	6 · t_{CY}
	HALT Mode	t_{RT2}	4 · t_{CY}	5 · t_{CY}	6 · t_{CY}
	STOP Mode	t_{RT2}	—	8197 · t_{CY}	8200 · t_{CY}
V_{CC} Hold Time		t_{PD}	5 · t_{CY}	—	—
V_{CC} Setup Time		t_{PS}	5 · t_{CY}	—	—

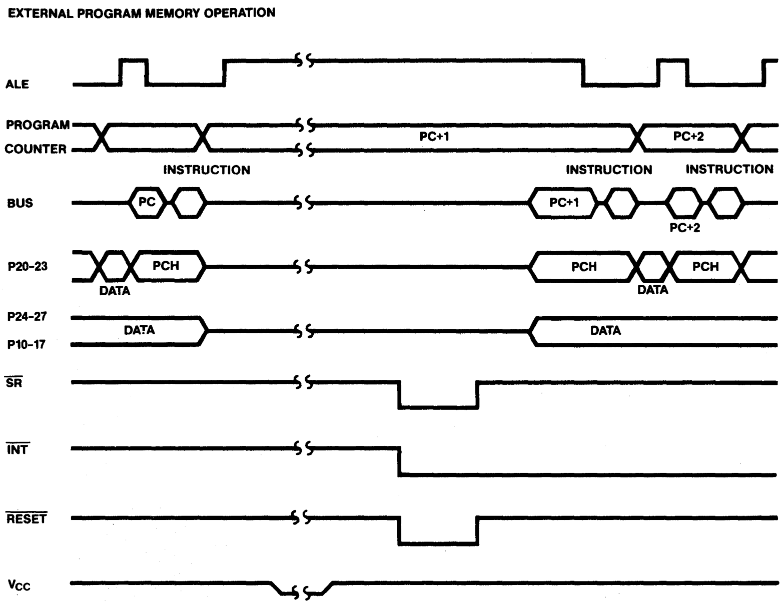
Timing Diagram

Figure 13. Standby Operation Timing (1)



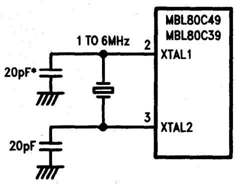
Timing Diagram
(Continued)

Figure 14. Standby Operation Timing (2)



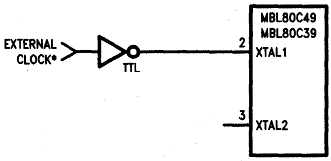
Oscillation Circuits

Crystal Oscillator



*Including stray capacitances

External Clock Drive

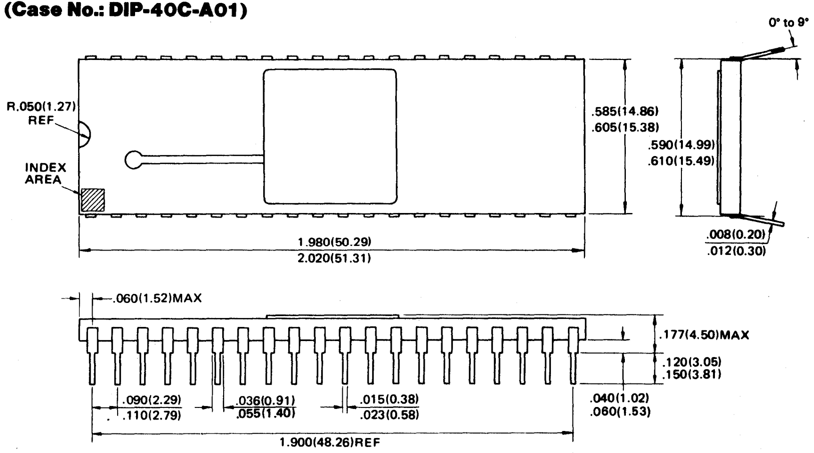


*Both high and low times should be more than 35% of the cycle time, and the rise and fall times should be less than 20ns.

Package Dimensions

Dimensions in inches (millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)



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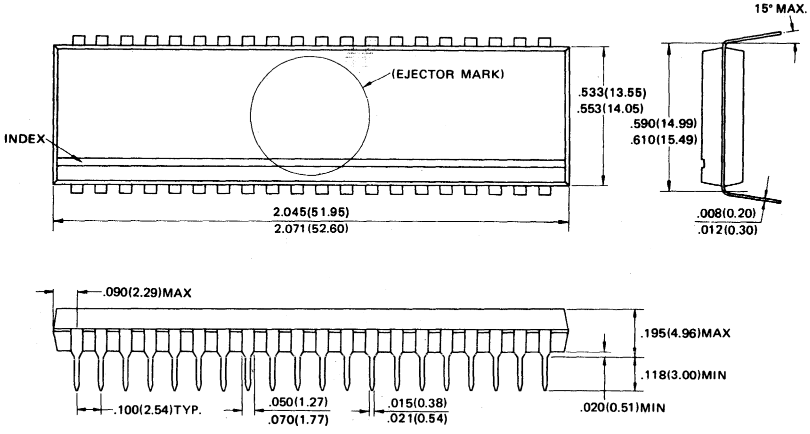
40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



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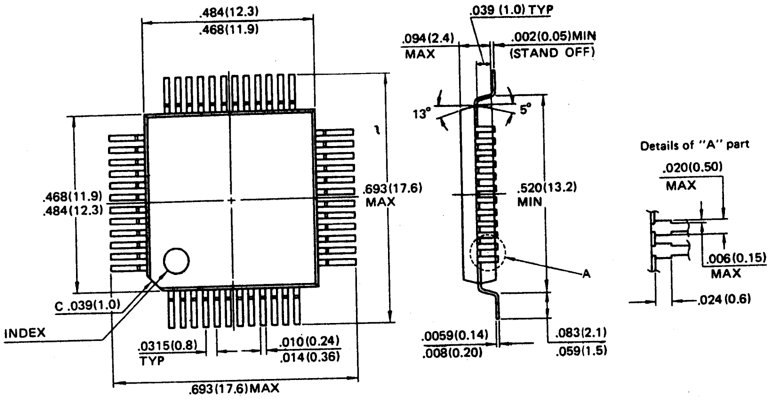
48-Lead Plastic Flat Package (CASE NO.:FPT-48P-M02)



Dimensions in inches (millimeters)

FUJITSU

NMOS INPUT/OUTPUT EXPANDER

MBL 8243

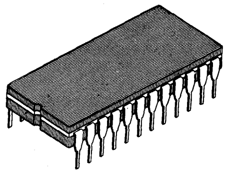
April 1986
Edition 2.1

NMOS INPUT/OUTPUT EXPANDER

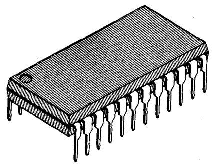
The Fujitsu MBL 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MBL 8048 series of single-chip microcomputers. Fabricated in 5 volts NMOS, the MBL 8243 combines low cost single supply voltage and high drive current capability. Also, the MBL 8243 is packaged in a 24-pin cerdip or plastic DIP package.

The MBL 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MBL 8048 series microcomputers. The 4-bit interface requires that only 4 I/O lines of the MBL 8048/8049/80C49/8749 be used for I/O expansion, and also allows multiple MBL 8243's to be added to the same bus.

The I/O ports of the MBL 8243 serve as a direct extension of the resident I/O facilities of the MBL 8048 series microcomputers and are accessed by their own MOVD, ANLD, and ORLD instructions.



CERAMIC DIP
DIP-24C-C01

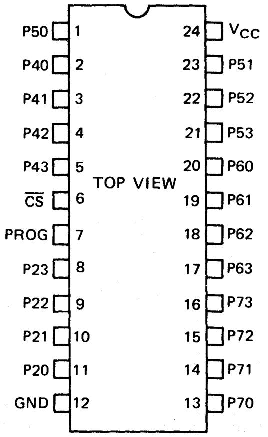


PLASTIC DIP
DIP-24P-M01

FEATURES

- Simple Interface to Fujitsu MBL 8048 Series and Intel MCS-48*
- Four 4-Bit I/O Ports.
- AND and OR Directly to Ports.
- High Current Drive: 5 mA at 0.45 V
  20 mA at 1.0 V
- On-Chip Power-On Reset Circuit.
- Single +5 V Power Supply.
- N-Channel Silicon-Gate E/D MOS Process.
- Two Package Options:
  —Standard 24-pin Cerdip (Suffix: Z)
  —Standard 24-pin Plastic DIP (Suffix: M)
- Pin-Compatible with Intel 8243 and Fujitsu MBL 82C43.

Fig. 1 – PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 2 – LOGIC SYMBOL

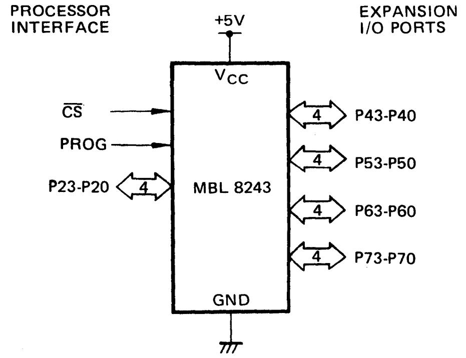
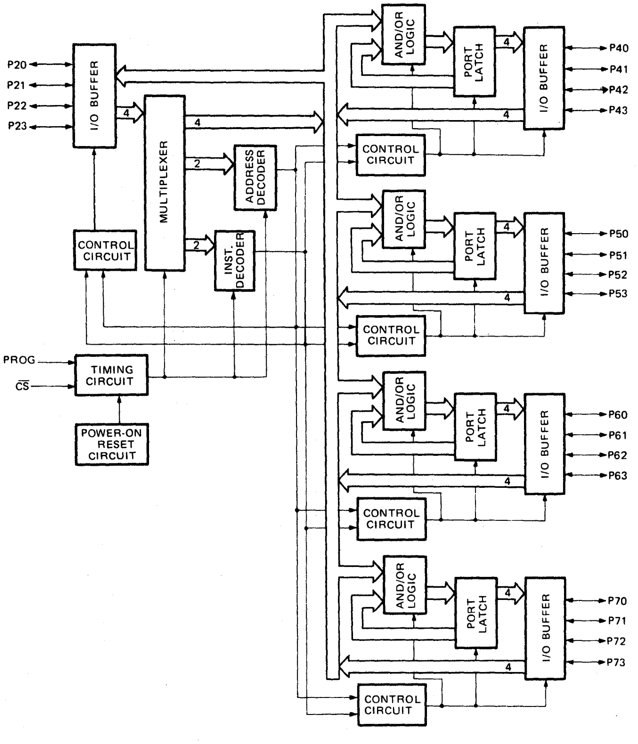


Fig. 3 – BLOCK DIAGRAM



PIN DESCRIPTION

The MBL 8243 has two interfaces: One is the processor interface; $\overline{CS}$, PROG, and Port 2, which are used for the processor to communicate with the MBL 8243 device. Another is the expansion I/O ports; Ports 4, 5, 6, and 7, which serve as an expansion of the processor's I/O.

Table 1—Pin Description

Symbol	Pin No.	Type	Function
V_{CC}	24	–	+5 V supply.
GND	12	–	0 V supply.
$\overline{CS}$	6	I	Chip Select input: A high on $\overline{CS}$ inhibits any change of output or internal status.
PROG	7	I	Clock input: A high-to-low transition on PROG signifies that address and control are available on P20–P23, and a low-to-high transition signifies that data is available on P20–P23.
P20 – P23	11 to 8	I/O	Port 2: Four (4) bit bi-directional port contains the address and control bits on a high-to-low transition of PROG. During a low-to-high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low-to-high transition if a read operation.
P40 – P43 P50 – P53 P60 – P63 P70 – P73	2 to 5 1, 23 to 21 20 to 17 13 to 16	I/O	Ports 4, 5, 6, and 7: Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20–P23 may be directly written, ANDed or ORed with previous data.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MBL 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the MBL 8048 series and the MBL 8243 occurs over Port 2 (P20–P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data. A high-to-low transition of the PROG line indicates that address is present while a low-to-high transition indicates the presence of data. Additional MBL 8243's may be added to the 4-bit bus and chip selected using additional output lines from the MBL 8048 series microcomputers.

POWER ON INITIALIZATION

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high-to-low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1 V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

WRITE MODES

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data, AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high-to-low transition of the PROG pin. On the low-to-high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

READ MODE

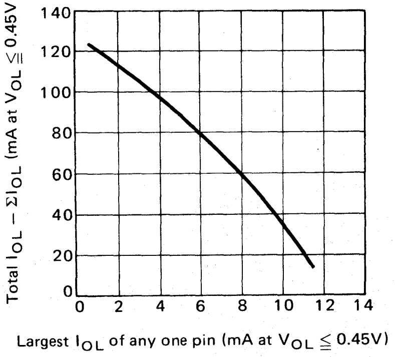
The device has one read mode. The operation code and port address are latched from the input port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low-to-high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the MBL 8243 output. A read of any port will leave that port in a high impedance state.

SINK CAPABILITY

The MBL 8243 can sink 5 mA at 0.45 V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

Fig. 4 – ΣI_{OL} vs I_{OL} (at $V_{OL} \leq 0.45V$)



For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA at 0.45 V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA
ΣI_{OL} = 60 mA from curve
# pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the MBL 8243.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An MBL 8243 will drive the following loads simultaneously.

2 loads – 20 mA at 1 V (port 7 only)
8 loads – 4 mA at 0.45 V
6 loads – 3.2 mA at 0.45 V
Is this within the specified limits?

ΣI_{OL} = (2 x 20) + (8 x 4) + (6 x 3.2) = 91.2 mA. From the curve: for I_{OL} = 4 mA. $\Sigma I_{OL} \approx$ 93 mA. since 91.2 mA $<$ 93 mA the loads are within specified limits.

Although the 20 mA at 1 V loads are used in calculating ΣI_{OL}, it is the largest current required at 0.45 V which determines the maximum allowable ΣI_{OL}.

TYPICAL APPLICATION

Fig. 5 – I/O EXPANDER INTERFACE

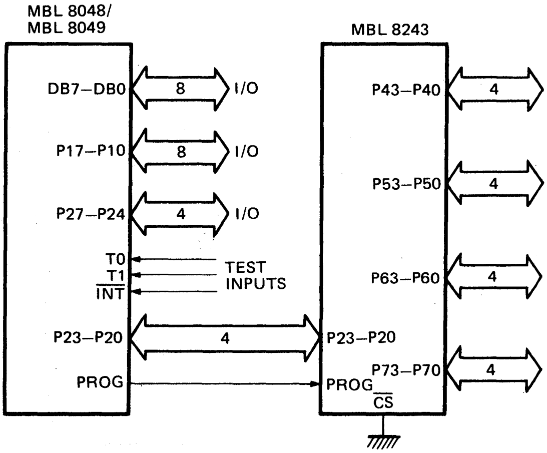
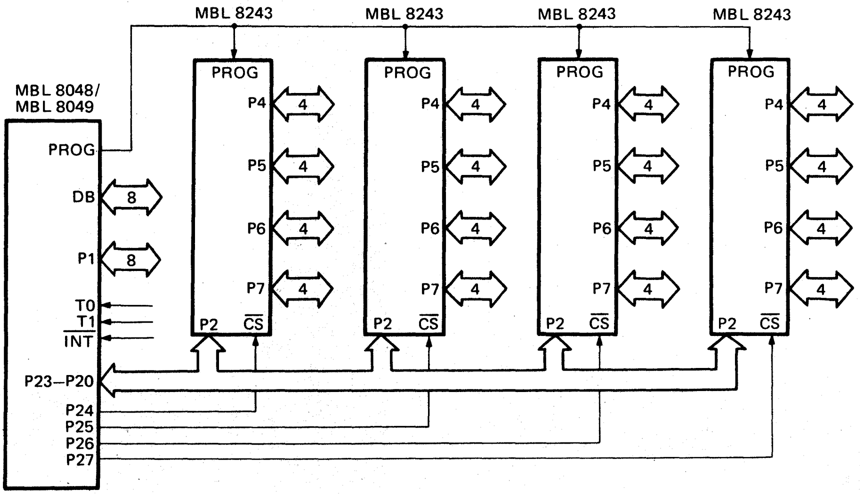


Fig. 6 – MULTIPLE I/O EXPANDER INTERFACE



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	GND − 0.3 to GND + 7.0	V
Input Voltage	V_{IN}	GND − 0.3 to GND + 7.0	
Ambient Temperature under Bias	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	
Power Dissipation	P_D	1	W

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+5 ± 10%	V
	GND	0	
Operating Temperature	T_A	0 to +70	°C

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, GND = 0V, T_A = 0°C to +70°C)

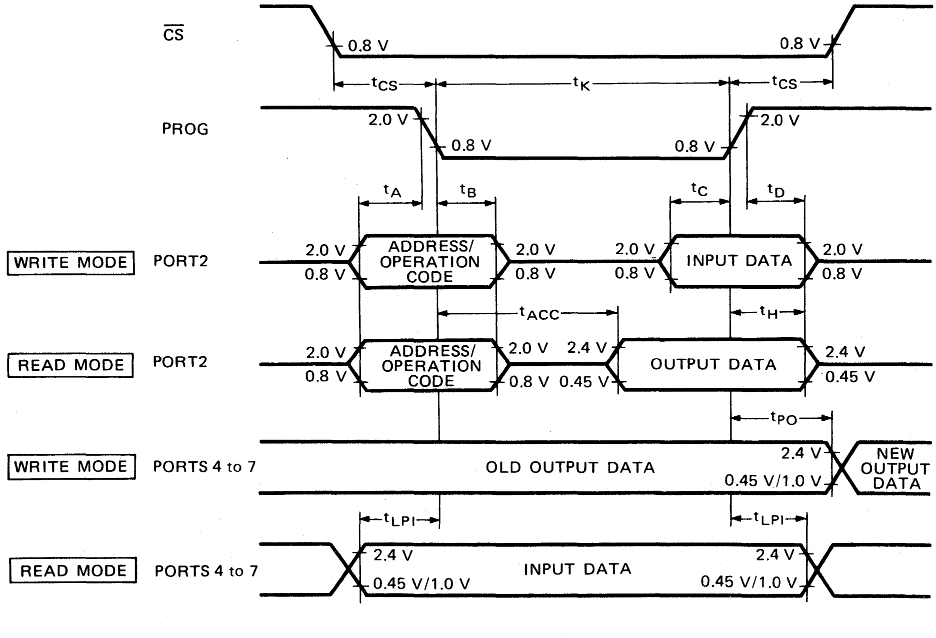
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input Low Voltage	V_{IL}		GND − 0.3		0.8	V
Input High Voltage	V_{IH}		2.0		V_{CC}+0.3	V
Output Low Voltage	V_{OL1}	Ports 4 to 7 I_{OL} = 5mA			0.45	V
	V_{OL2}	Ports 4 to 7 I_{OL} = 20mA			1.0	V
	V_{OL3}	Port 2 I_{OL} = 0.6mA			0.45	V
Output High Voltage	V_{OH1}	Ports 4 to 7 I_{OH} = −240μA	2.4			V
	V_{OH2}	Port 2 I_{OH} = −100μA	2.4			V
Input Leakage Current	I_{IL1}	Ports 4 to 7 GND ≦ V_{IN} ≦ V_{CC}	-10		20	μA
	I_{IL2}	Port 2, $\overline{CS}$, PROG GND ≦ V_{IN} ≦ V_{CC}	-10		10	μA
Total I_{OL} of 16 Output	ΣI_{OL}	I_{OUT}=5mA at each pin of Ports 4 to 7			80	mA
Supply Current	I_{CC}			10	20	mA

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, GND = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address/Operation Code Setup Time	t_A	C_L = 80pF	100			ns
Address/Operation Code Hold Time	t_B	C_L = 20pF	60			ns
Data Setup Time	t_C	C_L = 80pF	200			ns
Data Hold Time	t_D	C_L = 20pF	20			ns
Port 2 Floating Time	t_H	C_L = 20pF	0		150	ns
PROG Pulse Width	t_K		700			ns
$\overline{CS}$ Setup/Hold Times	t_{CS}		50			ns
Ports 4 to 7 Output Delay Time	t_{PO}	C_L = 100pF			700	ns
Ports 4 to 7 Setup/Hold Times	t_{LPI}		100			ns
Port 2 Output Delay Time	t_{ACC}	C_L = 80pF			650	ns

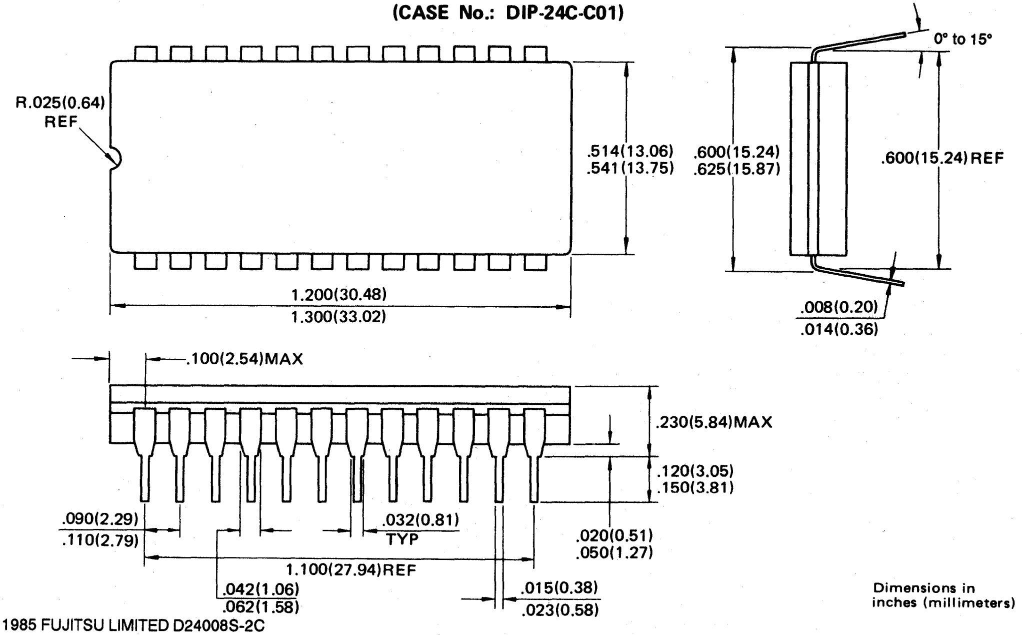
Fig. 7 — TIMING DIAGRAM



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: Z)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)

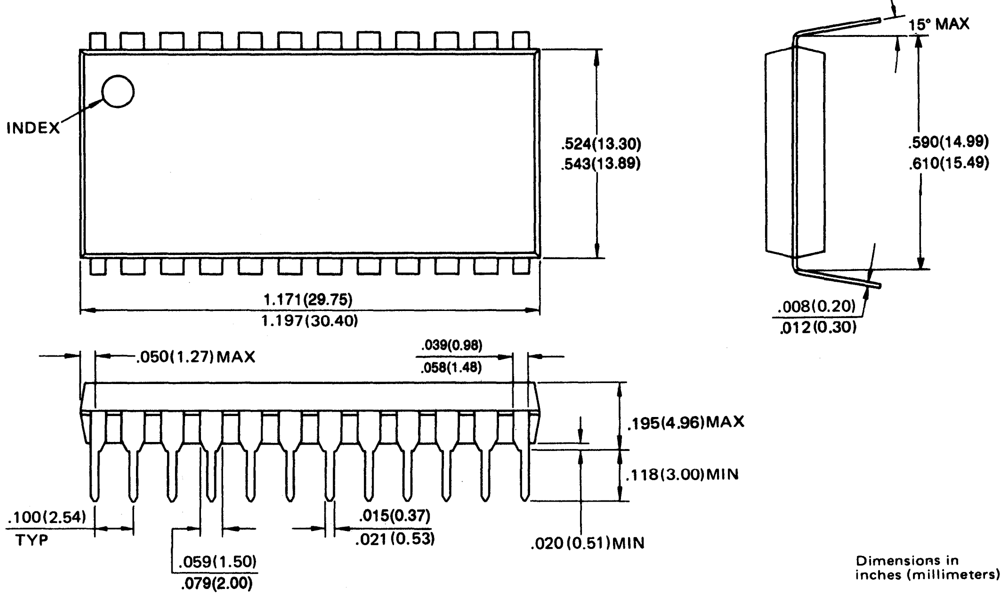


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: M)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE (CASE No.: DIP-24P-M01)



FUJITSU

CMOS INPUT/OUTPUT EXPANDER

MBL 82C43

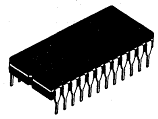
April 1986
Edition 2.1

CMOS INPUT/OUTPUT EXPANDER

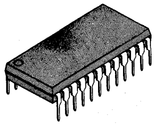
The Fujitsu MBL 82C43 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MBL 8048 series of single-chip microcomputers. Fabricated in 5 volts CMOS, the MBL 82C43 combines low cost single supply voltage and high drive current capability. Also, the MBL 82C43 is packaged in a 24-pin cerdip, plastic DIP, or plastic flat package (SOP).

The MBL 82C43 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MBL 8048 series microcomputers. The 4-bit interface requires that only 4 I/O lines of the MBL 8048/8049/80C49/8749 be used for I/O expansion, and also allows multiple MBL 82C43's to be added to the same bus.

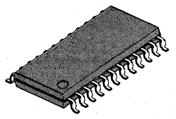
The I/O ports of the MBL 82C43 serve as a direct extension of the resident I/O facilities of the MBL 8048 series microcomputers and are accessed by their own MOVD, ANLD, and ORLD instructions.



CERAMIC DIP
DIP-24C-C01



PLASTIC DIP
DIP-24P-M01

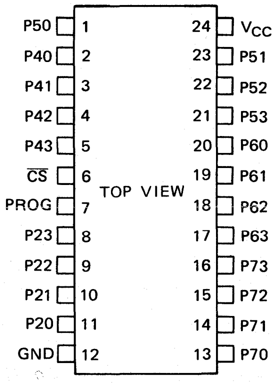


PLASTIC SOP
FPT-24P-M02

FEATURES

- CMOS Version of Fujitsu MBL 8243.
- Simple Interface to Fujitsu MBL 8048 Series and Intel MCS-48*
- Four 4-Bit I/O Ports.
- AND and OR Directly to Ports.
- High Current Drive: 5 mA at 0.45 V
  20 mA at 1.0 V
- On-Chip Power-On Reset Circuit
- Single +5 V Power Supply.
- Silicon-gate CMOS Process
- Three Package Options:
  —Standard 24-pin Cerdip (Suffix:-CZ)
  —Standard 24-pin Plastic DIP (Suffix:-P)
  —Standard 24-pin Plastic SOP (Suffix:-PF)
- Pin-Compatible with Fujitsu MBL 8243 and Intel 8243.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 — LOGIC SYMBOL

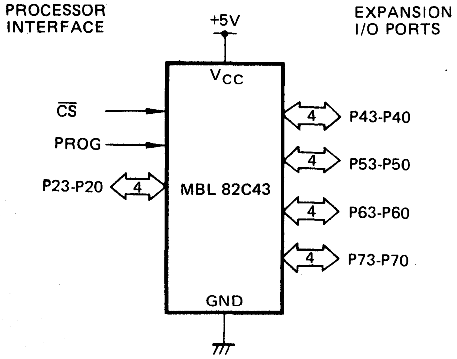
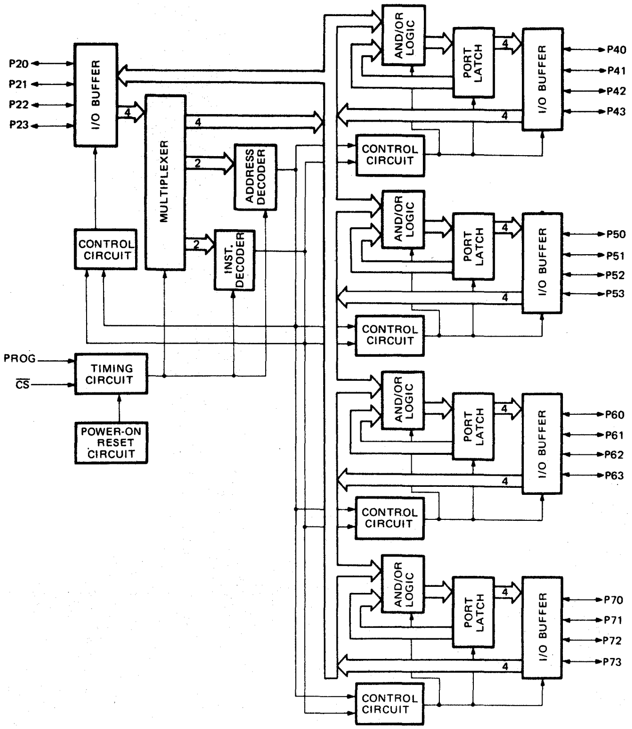


Fig. 2 — BLOCK DIAGRAM



PIN DESCRIPTION

The MBL 82C43 has two interfaces: One is the processor interface; $\overline{CS}$, PROG, and Port 2, which are used for the processor to communicate with the MBL 82C43 device. Another is the expansion I/O ports; Ports 4, 5, 6, and 7, which serve as an expansion of the processor's I/O.

Table 1-Pin Description

Symbol	Pin No.	Type	Function
V_{CC}	24	–	+5 V supply.
GND	12	–	0 V supply.
$\overline{CS}$	6	I	Chip Select input: A high on $\overline{CS}$ inhibits any change of output or internal status.
PROG	7	I	Clock input: A high-to-low transition on PROG signifies that address and control are available on P20-P23, and a low-to-high transition signifies that data is available on P20-P23.
P20 – P23	11 to 8	I/O	Port 2: Four (4) bit bi-directional port contains the address and control bits on a high-to-low transition of PROG. During a low-to-high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low-to-high transition if a read operation.
P40 – P43 P50 – P53 P60 – P63 P70 – P73	2 to 5 1, 23 to 21 20 to 17 13 to 16	I/O	Ports 4, 5, 6, and 7: Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20-P23 may be directly written, ANDed or ORed with previous data.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MBL 82C43 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the MBL 8048 series and the MBL 82C43 occurs over Port 2 (P20 – P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data. A high-to-low transition of the PROG line indicates that address is present while a low-to-high transition indicates the presence of data. Additional MBL 82C43's may be added to the 4-bit bus and chip selected using additional output lines from the MBL 8048 series microcomputers.

POWER ON INITIALIZATION

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high-to-low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1 V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

WRITE MODES

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data, AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high-to-low transition of the PROG pin. On the low-to-high transition of PROG data on port 2 is transferred to the logic block of the specified port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

READ MODE

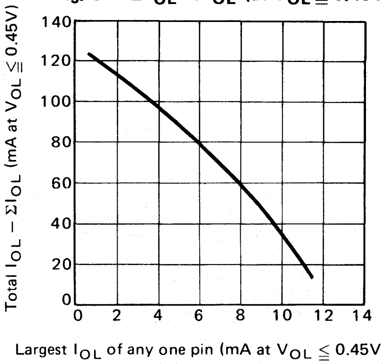
The device has one read mode. The operation code and port address are latched from the input port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low-to-high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the MBL 82C43 output. A read of any port will leave that port in a high impedance state.

SINK CAPABILITY

The MBL 82C43 can sink 5 mA at 0.45 V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

Fig. 3 – ΣI_{OL} vs I_{OL} (at $V_{OL} \leqq 0.45V$)



For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA at 0.45 V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA
ΣI_{OL} = 60 mA from curve
# pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the MBL 82C43.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An MBL 82C43 will drive the following loads simultaneously.

2 loads – 20 mA at 1 V (port 7 only)
8 loads – 4 mA at 0.45 V
6 loads – 3.2 mA at 0.45 V
Is this within the specified limits?

ΣI_{OL} = (2 x 20) + (8 x 4) + (6 x 3.2) = 91.2 mA.
From the curve: for I_{OL} = 4 mA. $\Sigma I_{OL} \approx$ 93 mA.
since 91.2 mA $<$ 93 mA the loads are within specified limits.

Although the 20 mA at 1 V loads are used in calculating ΣI_{OL}, it is the largest current required at 0.45 V which determines the maximum allowable ΣI_{OL}.

TYPICAL APPLICATION

Fig. 4 – I/O EXPANDER INTERFACE

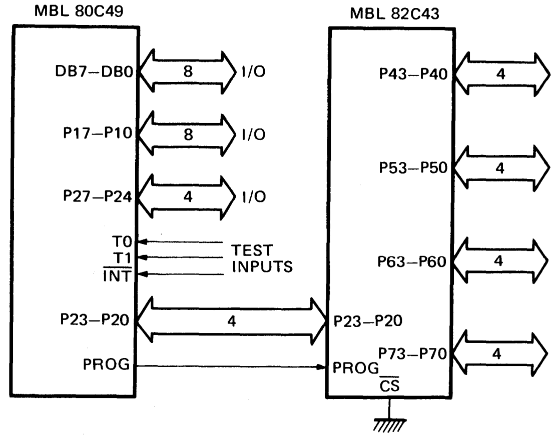
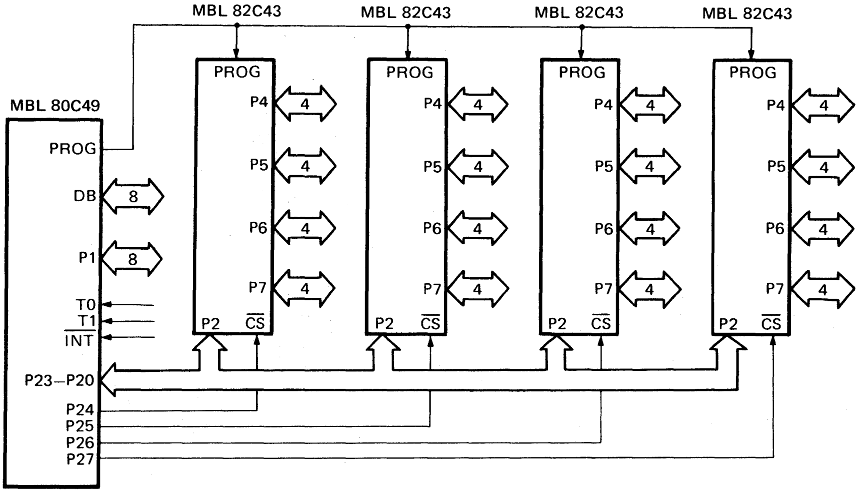


Fig. 5 – MULTIPLE I/O EXPANDER INTERFACE



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	GND –0.3 to +7.0	V
Input Voltage	V_{IN}	GND –0.3 to +7.0*	
Ambient Temperature under Bias	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	
Power Dissipation	P_D	1	W

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

* V_{IN} should not exceed V_{CC} + 0.3V.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	+5 ±10%	V	Normal Operation
		3.5 to 6.0		Standby Operation
	GND	0	V	
Operating Temperature	T_A	–40 to +85	°C	

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, GND = 0V, T_A = –40°C to +85°C)

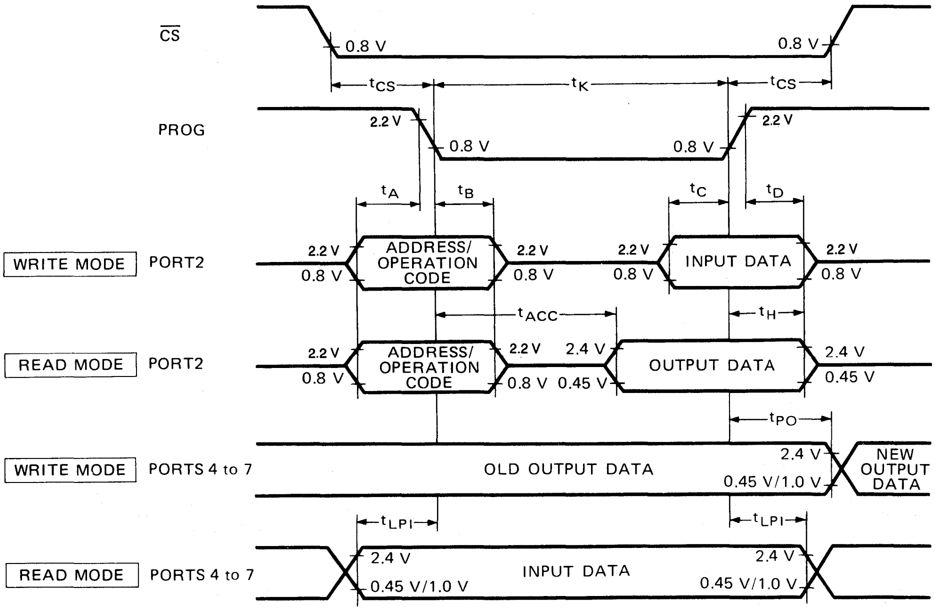
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Low Voltage	V_{IL}		GND –0.3		0.8	V
Input High Voltage	V_{IH}		2.2		V_{CC} +0.3	V
Output Low Voltage	V_{OL1}	Ports 4 to 7 I_{OL} = 5mA			0.45	V
	V_{OL2}	Ports 4 to 7 I_{OL} = 20mA			1.0	V
	V_{OL3}	Port 2 I_{OL} = 0.6mA			0.45	V
Output High Voltage	V_{OH1}	Ports 4 to 7 I_{OH} = -240μA	2.4			V
	V_{OH2}	Port 2 I_{OH} = –100μA	2.4			V
Input Leakage Current	I_{IL1}	Ports 4 to 7 GND ≦ V_{IN} ≦ V_{CC}	-10		20	μA
	I_{IL2}	Port 2, $\overline{CS}$, PROG GND ≦ V_{IN} ≦ V_{CC}	-10		10	μA
Total I_{OL} of 16 Outputs	ΣI_{OL}	I_{OUT} = 5mA at each pin of Ports 4 to 7			80	mA
Supply Current	I_{CC1}	All outputs open, Normal operation		200	600	μA
	I_{CC2}	All outputs open, Standby operation		1	10	μA

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, GND = 0V, T_A = −40°C to +85°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Address/Operation Code Setup Time	t_A	C_L = 80pF	100			ns
Address/Operation Code Hold Time	t_B	C_L = 20pF	60			ns
Data Setup Time	t_C	C_L = 80pF	200			ns
Data Hold Time	t_D	C_L = 20pF	20			ns
Port 2 Floating Time	t_H	C_L = 20pF	0		150	ns
PROG Pulse Width	t_K		700			ns
$\overline{CS}$ Setup/Hold Times	t_{CS}		50			ns
Ports 4 to 7 Output Delay Time	t_{PO}	C_L = 100pF			700	ns
Ports 4 to 7 Setup/Hold Times	t_{LPI}		100			ns
Port 2 Output Delay Time	t_{ACC}	C_L = 80pF			650	ns

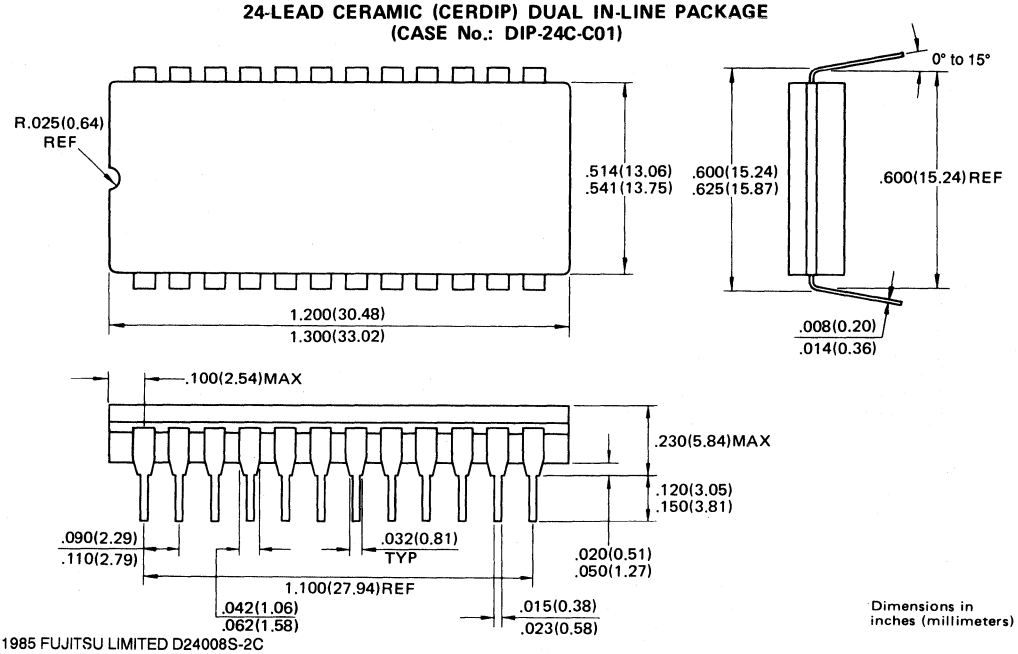
Fig. 6 — TIMING DIAGRAM



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix:-CZ)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)

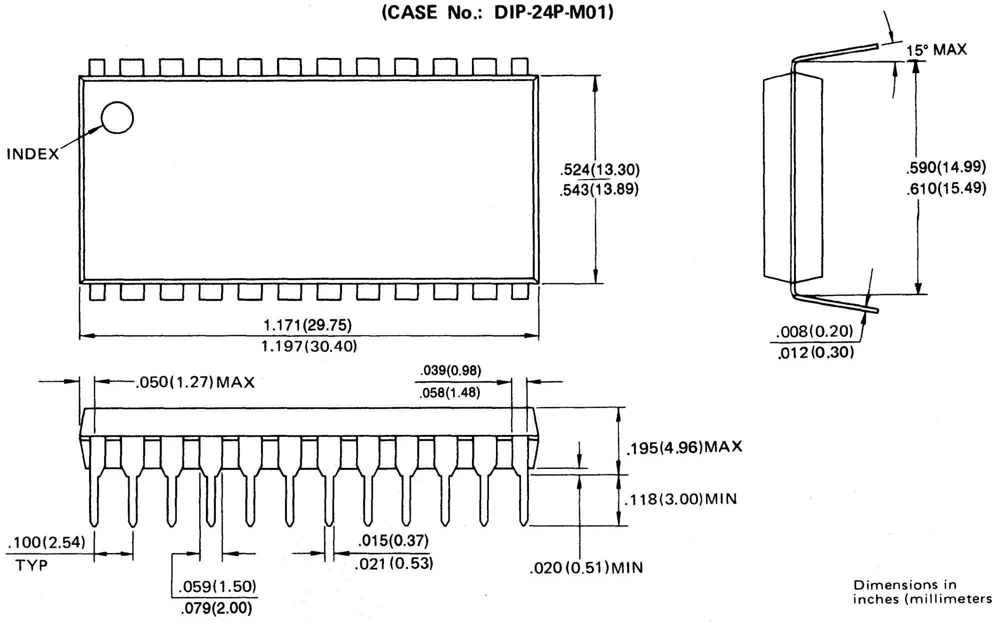


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix:-P)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M01)

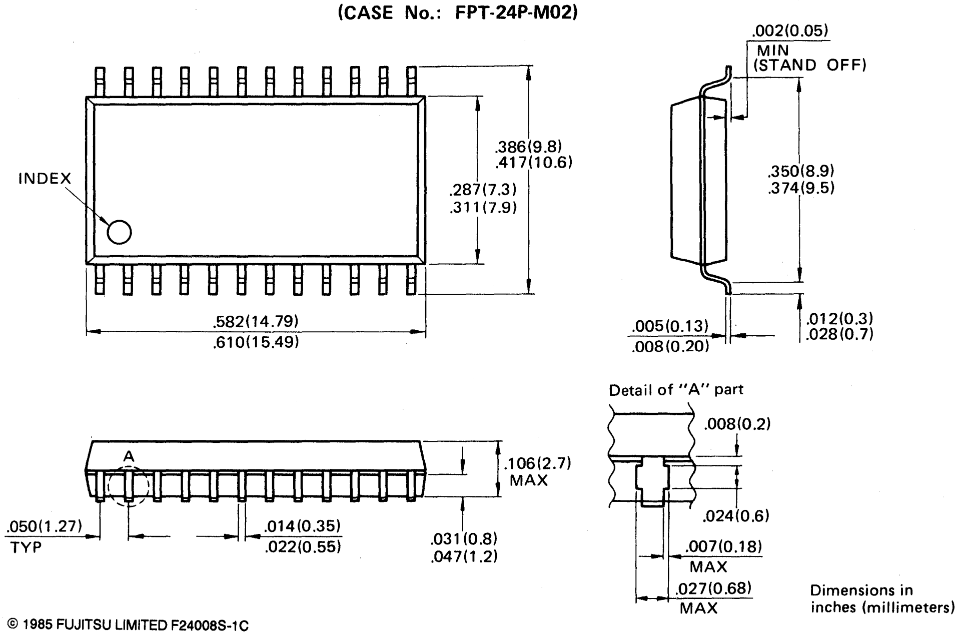


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC SOP (Suffix:-PF)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in inches (millimeters)

Selector Guide

4–Bit Microcomputers

April 1986
Edition 3.0

4-Bit Microcontrollers and Peripherals

Table 1: FUJITSU 4-BIT MCU FAMILY

Process/ Series	ROM Size [bits]	RAM Size [bits]	Device Number	Package[1]	Device Number	Package
NMOS MB 8840 Series	2K x 8	128 x 4	MB 8841HM/-PSH	DIP-42P-M01/M02	MB 8845HM	FPT-48P-M02
	2K x 8	128 x 4	MB 8842M/-PSH	DIP-28P-M02/M03	MB 8846M	FPT-48P-M02
	1K x 8	64 x 4	MB 8843M/-PSH	DIP-42P-M01/M02	MB 8847M	FPT-48P-M02
	1K x 8	64 x 4	MB 8844M/-PSH	DIP-28P-M02/M03	MB 8848M	FPT-48P-M02
CMOS MB 8850/H MB 8850B Series	2K x 8	128 x 4	MB 8851M/-PSH	DIP-42P-M01/M02	MB 8855M	FPT-48P-M02
	2K x 8	128 x 4	MB 8852M/-PSH	DIP-28P-M02/M03	MB 8856M	FPT-48P-M02
	1K x 8	64 x 4	MB 8854M/-PSH	DIP-28P-M02/M03	MB 8858M	FPT-48P-M02
	2K x 8	128 x 4	MB 8851AM/-PSH	DIP-42P-M01/M02	MB 8855AM	FPT-48P-M02
	2K x 8	128 x 4	MB 8852AM/-PSH	DIP-28P-M02/M03	MB 8856AM	FPT-48P-M02
	1K x 8	64 x 4	MB 8854AM/-PSH	DIP-28P-M02/M03	MB 8858AM	FPT-48P-M02
	2K x 8	128 x 4	MB 8851LM/-PSH	DIP-42P-M01/M02	MB 8855LM	FPT-48P-M02
	2K x 8	128 x 4	MB 8852LM/-PSH	DIP-28P-M02/M03	MB 8856LM	FPT-48P-M02
	1K x 8	64 x 4	MB 8854LM/-PSH	DIP-28P-M02/M03	MB 8858LM	FPT-48P-M02
	2K x 8	128 x 4	MB 8851HM/-PSH	DIP-42P-M01/M02	MB 8855HM	FPT-48P-M02
	2K x 8	128 x 4	MB 8851B-P[3]	DIP-42P-M01	MB 8855B-P[3]	FPT-48P-M02
CMOS MB 88200/H MB 88200B Series	512 x 8	16 x 4	MB 88201-P	DIP-16P-M02	MB 88201-PF	FPT-16P-M03
	1K x 8	32 x 4	MB 88202-P	DIP-16P-M02	MB 88202-PF	FPT-16P-M03
	512 x 8	16 x 4	MB 88201A-P	DIP-16P-M02	MB 88201A-PF	FPT-16P-M03
	1K x 8	32 x 4	MB 88202A-P	DIP-16P-M02	MB 88202A-PF	FPT-16P-M03
	512 x 8	16 x 4	MB 88201H-P	DIP-16P-M02	MB 88201H-PF	FPT-16P-M03
	1K x 8	32 x 4	MB 88202H-P	DIP-16P-M02	MB 88202H-PF	FPT-16P-M03
	1K x 8	32 x 4	*MB 88205B-P[3]	DIP-28P-M02	–	–
CMOS MB 88210 Series	1K x 8	32 x 4	MB 88211-P[4]	DIP-20P-M02	–	–
NMOS MB 88400/H Series	4K x 8	192 x 4	MB 88401-P/-PSH	DIP-42P-M01/M02	MB 88401-PF	FPT-48P-M02
	4K x 8	256 x 4	MB 88401H-P/-PSH	DIP-42P-M01/M02	MB 88401H-PF	FPT-48P-M02
	2K x 8	256 x 4	MB 88403H-P/-PSH	DIP-42P-M01/M02	MB 88403H-PF	FPT-48P-M02
NMOS MB 88410/H Series	4K x 8	192 x 4	MB 88411-P/-PSH[4]	DIP-42P-M01/M02	MB 88411-PF[4]	FPT-48P-M02
	2K x 8	192 x 4	MB 88413-P/-PSH[4]	DIP-42P-M01/M02	MB 88413-PF[4]	FPT-48P-M02
	4K x 8	256 x 4	MB 88411H-P/-PSH[4]	DIP-42P-M01/M02	MB 88411H-PF[4]	FPT-48P-M02
	2K x 8	256 x 4	MB 88413H-P/-PSH[4]	DIP-42P-M01/M02	MB 88413H-PF[4]	FPT-48P-M02
NMOS MB 88420/H Series	4K x 8	192 x 4	MB 88421-PSH[5]	DIP-64P-M01	–	–
	3K x 8	192 x 4	MB 88422-PSH[5]	DIP-64P-M01	–	–
	2K x 8	128 x 4	MB 88423-PSH[5]	DIP-64P-M01	–	–
	4K x 8	256 x 4	MB 88421H-PSH[5]	DIP-64P-M01	–	–

Maximum Input Only Ports	Maximum Output Only Ports	Maximum I/O Ports	Maximum Control Ports	Supply Voltage	Typical Power Dissipation [mW]	Number of Instructions	Minimum Instruction Cycle Time [μs]	Maximum Clock Frequency[2] [MHz]	Process/ Series
4	12	16	5	5.0 ± 10%	350	70	2.0	3.0	NMOS MB 8840 Series
4	8	11	2	5.0 ± 10%	300	69	3.0	2.0	
4	12	16	5	5.0 ± 10%	300	70	3.0	2.0	
4	8	11	2	5.0 ± 10%	300	69	3.0	2.0	
4	12	16	5	5.0 ± 10%	10 at 1MHz	70	3.0	2.0	CMOS MB 8850/H MB 8850B Series
4	8	11	2	5.0 ± 10%	10 at 1MHz	69	3.0	2.0	
4	8	11	2	5.0 ± 10%	10 at 1MHz	69	3.0	2.0	
4	12	16	5	3.5 to 6.0	10 at 1MHz	70	3.0	2.0	
4	8	11	2	3.5 to 6.0	10 at 1MHz	69	3.0	2.0	
4	8	11	2	3.5 to 6.0	10 at 1MHz	69	3.0	2.0	
4	12	16	5	2.5 to 4.0	1.8 at 0.5MHz	70	7.5	0.8	
4	8	11	2	2.5 to 4.0	1.8 at 0.5MHz	69	7.5	0.8	
4	8	11	2	2.5 to 4.0	1.8 at 0.5MHz	69	7.5	0.8	
4	12	16	5	5.0 ± 10%	15 at 2MHz	70	1.5	4.0	
4	12	16	5	5.0 ± 10%	10 at 1MHz	70	2.0	3.0	
0	0	12	0	5.0 ± 10%	5 at 1MHz	37	3.0	2.0	CMOS MB 88200/H MB 88200B Series
0	0	12	0	5.0 ± 10%	5 at 1MHz	38	3.0	2.0	
0	0	12	0	3.5 to 6.0	5 at 1MHz	37	3.0	2.0	
0	0	12	0	3.5 to 6.0	5 at 1MHz	38	3.0	2.0	
0	0	12	0	5.0 ± 10%	15 at 3MHz	37	1.5	4.0	
0	0	12	0	5.0 ± 10%	15 at 3MHz	38	1.5	4.0	
0	16	7	0	5.0 ± 10%	15 at 1MHz	39	3.0	2.0	
0	0	10	0	5.0 ± 10%	10 at 4MHz	39	3.0	4.0 with prescaler	CMOS MB 88210 Series
4	12	15	5	5.0 ± 10%	365	75	2.86	2.0	NMOS MB 88400/H Series
4	12	16	5	5.0 ± 10%	425	76	1.5	4.0	
4	12	16	5	5.0 ± 10%	425	76	1.5	4.0	
4	12	12	5	5.0 ± 10%	384	74	2.86	2.0	NMOS MB 88410/H Series
4	12	12	5	5.0 ± 10%	384	74	2.86	2.0	
4	12	12	5	5.0 ± 10%	440	75	1.5	4.0	
4	12	12	5	5.0 ± 10%	440	75	1.5	4.0	
4	8	40	5	5.0 ± 10%	415	79	2.86	2.0	NMOS MB 88420/H Series
4	8	40	5	5.0 ± 10%	415	79	2.86	2.0	
4	8	40	5	5.0 ± 10%	415	79	2.86	2.0	
4	8	40	5	5.0 ± 10%	415	80	1.5	4.0	

Table 1: (Continued)

Process/ Series	ROM Size [bits]	RAM Size [bits]	Device Number	Package[1]	Device Number	Package
CMOS MB 88500/H Series	4K x 8	192 x 4	MB 88501-P/-PSH	DIP-42P-M01/M02	MB 88501-PF	FPT-48P-M02
	4K x 8	256 x 4	MB 88505-P/-PSH	DIP-42P-M01/M02	MB 88505-PF	FPT-48P-M02
	2K x 8	256 x 4	MB 88507-P/-PSH	DIP-42P-M01/M02	MB 88507-PF	FPT-48P-M02
	4K x 8	192 x 4	MB 88501A-P/-PSH	DIP-42P-M01/M02	MB 88501A-PF	FPT-48P-M02
	4K x 8	256 x 4	MB 88505A-P/-PSH	DIP-42P-M01/M02	MB 88505A-PF	FPT-48P-M02
	4K x 8	256 x 4	MB 88501H-P/-PSH	DIP-42P-M01/M02	MB 88501H-PF	FPT-48P-M02
	2K x 8	256 x 4	MB 88503H-P/-PSH	DIP-42P-M01/M02	MB 88503H-PF	FPT-48P-M02
	4K x 8	256 x 4	MB 88505H-P/-PSH	DIP-42P-M01/M02	MB 88505H-PF	FPT-48P-M02
CMOS MB 88510 MB 88510B Series	4K x 8	256 x 4	*MB 88511-P/-PSH[4]	DIP-42P-M01/M02	*MB 88511-PF[4]	FPT-48P-M02
	2K x 8	192 x 4	*MB 88513-P/-PSH[4]	DIP-42P-M01/M02	*MB 88513-PF[4]	FPT-48P-M02
	6K x 8	256 x 4	MB 88514B-PSH[3,4,5]	DIP-64P-M01	–	–
	8K x 8	256 x 4	MB 88515B-PSH[3,4,5]	DIP-64P-M01	–	–
	4K x 8	256 x 4	MB 88516B-PSH[3,4]	DIP-64P-M01	–	–
	4K x 8	256 x 4	MB 88517B-P[3,4]	DIP-42P-M01	–	–
CMOS MB 88520 MB 88520B Series	4K x 8	256 x 4	MB 88521-PSH[5]	DIP-64P-M01	MB 88521-PF[5]	FPT-64P-M01
	4K x 8	256 x 4	*MB 88522-PSH[5]	DIP-64P-M01	–	–
	2K x 8	256 x 4	MB 88523-PSH[5]	DIP-64P-M01	MB 88523-PF[5]	FPT-64P-M01
	4K x 8	256 x 4	MB 88525-PSH[5]	DIP-64P-M01	–	–
	4K x 8	256 x 4	MB 88525B-PSH[3,5]	DIP-64P-M01	MB 88525B-PF[3,5]	FPT-64P-M01
CMOS MB 88530 Series	2K x 8	128 x 4	MB 88535-P/-PSH[6]	DIP-42P-M01/M02	MB 88535-PF[6]	FPT-48P-M02
	2K x 8	128 x 4	MB 88536-P/-PSH[6]	DIP-42P-M01/M02	MB 88536-PF[6]	FPT-48P-M02
CMOS MB 88540 Series	4K x 8	256 x 4	–	–	MB 88541-PF[7]	FPT-70P-M01
	4K x 8	256 x 4	–	–	*MB 88543-PF[7]	FPT-80P-M01
	4K x 8	256 x 4	–	–	*MB 88544-PF[7]	FPT-80P-M01
	4K x 8	256 x 4	–	–	*MB 88545-PF[7]	FPT-80P-M01
	4K x 8	256 x 4	–	–	*MB 88546-PF[7]	FPT-80P-M01
CMOS MB 88550/H Series	8K x 8	256 x 4	–	–	MB 88551-PF[4,5]	FPT-80P-M01
	6K x 8	256 x 4	–	–	MB 88552-PF[4,5]	FPT-80P-M01
	8K x 8	256 x 4	–	–	MB 88551H-PF[4,5]	FPT-80P-M01
	6K x 8	256 x 4	–	–	MB 88552H-PF[4,5]	FPT-80P-M01
CMOS MB 88560 Series	3K x 8	192 x 4	–	–	MB 88561-PF[4,7,8]	FPT-80P-M01
	4K x 8	256 x 4	–	–	*MB 88562-PF[3,4,8]	FPT-80P-M01

Notes:

1. 28- and 42-pin DIP packages may be specified with standard 100 mil pin spacing [M or -P suffix as shown], or small-outline 70 mil pin spacing [-PSH suffix]. The 64-pin DIP is available in small-outline 70 mil pin spacing only [-PSH suffix].
2. When the on-chip prescaler is connected, the maximum external clock frequency can be doubled. A 4.194 MHz crystal can be used for MB 884XX or MB 885XX devices. (except MB 88530 series)
3. On-chip VFD driver port
4. On-chip A/D converter
5. Multiple I/O ports
6. On-chip D/A converter
7. On-chip LCD driver
8. On-chip PLL

* Under development

Maximum Input Only Ports	Maximum Output Only Ports	Maximum I/O Ports	Maximum Control Ports	Supply Voltage	Typical Power Dissipation [mW]	Number of Instructions	Minimum Instruction Cycle Time [μs]	Maximum Clock Frequency[2] [MHz]	Process/ Series
4	12	15	5	5.0 ± 10%	10 at 1MHz	75	2.86	2.0	CMOS MB 88500/H Series
4	12	15	5	5.0 ± 10%	10 at 1MHz	75	2.0	3.0	
4	12	15	5	5.0 ± 10%	10 at 1MHz	75	2.0	3.0	
4	12	15	5	3.5 to 6.0	10 at 1MHz	75	2.86	2.0	
4	12	15	5	3.5 to 6.0	10 at 1MHz	75	2.86	2.0	
4	12	15	5	5.0 ± 10%	20 at 2MHz	76	1.5	4.0	
4	12	15	5	5.0 ± 10%	20 at 2MHz	76	1.5	4.0	
4	12	15	5	5.0 ± 10%	20 at 2MHz	76	1.5	4.0	
0	0	34	5	5.0 ± 10%	15 at 1MHz	79	2.0	3.0	CMOS MB 88510 MB 88510B Series
0	0	34	5	5.0 ± 10%	15 at 1MHz	79	2.0	3.0	
0	25	29	5	5.0 ± 10%	15 at 1MHz	81	2.0	3.0	
0	25	29	5	5.0 ± 10%	15 at 1MHz	81	2.0	3.0	
0	17	26	5	5.0 ± 10%	15 at 1MHz	81	2.0	3.0	
0	15	19	5	5.0 ± 10%	15 at 1MHz	81	2.0	3.0	
4	8	40	5	5.0 ± 10%	10 at 1MHz	80	2.0	3.0	CMOS MB 88520 MB 88520B Series
4	8	40	5	5.0 ± 10%	TBD	80	2.0	3.0	
4	8	40	5	5.0 ± 10%	10 at 1MHz	80	2.0	3.0	
4	8	40	5	5.0 ± 10%	10 at 1MHz	80	2.0	3.0	
4	32	16	5	5.0 ± 10%	10 at 1MHz	79	2.0	3.0	
4	8	17	5	5.0 ± 10%	10 at 1MHz	70	3.0	2.0	CMOS MB 88530 Series
4	8	15	5	5.0 ± 10%	10 at 1MHz	70	3.0	2.0	
4	4	16	5	5.0 ± 10%	10 at 1MHz	75	2.86	2.0	CMOS MB 88540 Series
4	4	16	5	5.0 ± 10%	10 at 1MHz	76	2.0	3.0	
4	4	24	5	5.0 ± 10%	10 at 1MHz	80	2.0	3.0	
4	4	16	5	5.0 ± 10%	10 at 1MHz	76	2.0	3.0	
4	4	24	5	5.0 ± 10%	10 at 1MHz	80	2.0	3.0	
0	0	68	5	5.0 ± 10%	15 at 1MHz	82	2.0	3.0	CMOS MB 88550/H Series
0	0	68	5	5.0 ± 10%	15 at 1MHz	82	2.0	3.0	
0	0	68	5	5.0 ± 10%	25 at 2MHz	82	1.5	4.0	
0	0	68	5	5.0 ± 10%	25 at 2MHz	82	1.5	4.0	
4	4	11	2	5.0 ± 10%	85 at 4.5MHz	70	6.67	4.5	CMOS MB 88560 Series
4	4	11	2	5.0 ± 10%	TBD	71	6.67	4.5	

Table 2: FEATURES OPTIONS AVAILABLE ON THE FUJITSU 4-BIT MCU FAMILY

Device Number	Process	ROM Size [bits]	RAM Size [bits]	Package	Ambient Temperature Range [°C]	Serial Port Output Latch	Serial Buffer	Nesting Levels
MB 8841HM/-PSH	NMOS	2K x 8	128 x 4	DIP	–30 to +70	option	4	4
MB 8842M/-PSH	NMOS	2K x 8	128 x 4	DIP	–30 to +70	no	4	4
MB 8843M/-PSH	NMOS	1K x 8	64 x 4	DIP	–30 to +70	option	4	4
MB 8844M/-PSH	NMOS	1K x 8	64 x 4	DIP	–30 to +70	no	4	4
MB 8845HM	NMOS	2K x 8	128 x 4	FPT	–30 to +70	option	4	4
MB 8846M	NMOS	2K x 8	128 x 4	FPT	–30 to +70	no	4	4
MB 8847M	NMOS	1K x 8	64 x 4	FPT	–30 to +70	option	4	4
MB 8848M	NMOS	1K x 8	64 x 4	FPT	–30 to +70	no	4	4
MB 8851M/-PSH	CMOS	2K x 8	128 x 4	DIP	–40 to +85	option	4	4
MB 8851AM/-PSH	CMOS	2K x 8	128 x 4	DIP	–30 to +70	option	4	4
MB 8851B-P	CMOS	2K x 8	128 x 4	DIP	–30 to +70	option	4	4
MB 8851HM/-PSH	CMOS	2K x 8	128 x 4	DIP	–40 to +85	option	4	4
MB 8851LM/-PSH	CMOS	2K x 8	128 x 4	DIP	–30 to +70	option	4	4
MB 8852M/-PSH	CMOS	2K x 8	128 x 4	DIP	–40 to +85	no	4	4
MB 8852AM/-PSH	CMOS	2K x 8	128 x 4	DIP	–30 to +70	no	4	4
MB 8852LM/-PSH	CMOS	2K x 8	128 x 4	DIP	–30 to +70	no	4	4
MB 8854M/-PSH	CMOS	1K x 8	64 x 4	DIP	–40 to +85	no	4	4
MB 8854AM/-PSH	CMOS	1K x 8	64 x 4	DIP	–30 to +70	no	4	4
MB 8854LM/-PSH	CMOS	1K x 8	64 x 4	DIP	–30 to +70	no	4	4
MB 8855M	CMOS	2K x 8	128 x 4	FPT	–40 to +85	option	4	4
MB 8855AM	CMOS	2K x 8	128 x 4	FPT	–30 to +70	option	4	4
MB 8855B-P	CMOS	2K x 8	128 x 4	FPT	–30 to +70	option	4	4
MB 8855HM	CMOS	2K x 8	128 x 4	FPT	–40 to +85	option	4	4
MB 8855LM	CMOS	2K x 8	128 x 4	FPT	–30 to +70	option	4	4
MB 8856M	CMOS	2K x 8	128 x 4	FPT	–40 to +85	no	4	4
MB 8856AM	CMOS	2K x 8	128 x 4	FPT	–30 to +70	no	4	4
MB 8856LM	CMOS	2K x 8	128 x 4	FPT	–30 to +70	no	4	4
MB 8858M	CMOS	1K x 8	64 x 4	FPT	–40 to +85	no	4	4
MB 8858AM	CMOS	1K x 8	64 x 4	FPT	–30 to +70	no	4	4
MB 8858LM	CMOS	1K x 8	64 x 4	FPT	–30 to +70	no	4	4

Output Port Options[1]	PLA Output Port[2] [bits]	Optional On-chip Prescaler	On-chip Clock Generator	Features	Device Number
5	4/8	yes	yes	High speed	MB 8841HM/-PSH
3	4/8	yes	yes	Standard	MB 8842M/-PSH
4	4/8	yes	yes	Standard	MB 8843M/-PSH
3	4/8	yes	yes	Standard	MB 8844M/-PSH
5	4/8	yes	yes	High speed	MB 8845HM
3	4/8	yes	yes	Standard	MB 8846M
4	4/8	yes	yes	Standard	MB 8847M
3	4/8	yes	yes	Standard	MB 8848M
2	4/8	yes	yes	Standard	MB 8851M/-PSH
2	4/8	yes	yes	Wide voltage range	MB 8851AM/-PSH
2	4/8	yes	yes	VFD driver port [8 seg. x 8 digits], high speed	MB 8851B-P
4	4/8	yes	yes	High speed	MB 8851HM/-PSH
2	4/8	yes	yes	Low voltage	MB 8851LM/-PSH
2	4/8	yes	yes	Standard	MB 8852M/-PSH
2	4/8	yes	yes	Wide voltage range	MB 8852AM/-PSH
2	4/8	yes	yes	Low voltage	MB 8852LM/-PSH
2	4/8	yes	yes	Standard	MB 8854M/-PSH
2	4/8	yes	yes	Wide voltage range	MB 8854AM/-PSH
2	4/8	yes	yes	Low voltage	MB 8854LM/-PSH
2	4/8	yes	yes	Standard	MB 8855M
2	4/8	yes	yes	Wide voltage range	MB 8855AM
2	4/8	yes	yes	VFD driver port [8 seg. x 8 digits], high speed	MB 8855B-P
4	4/8	yes	yes	High speed	MB 8855HM
2	4/8	yes	yes	Low voltage	MB 8855LM
2	4/8	yes	yes	Standard	MB 8856M
2	4/8	yes	yes	Standard	MB 8856AM
2	4/8	yes	yes	Standard	MB 8856LM
2	4/8	yes	yes	Standard	MB 8858M
2	4/8	yes	yes	Wide voltage range	MB 8858AM
2	4/8	yes	yes	Low voltage	MB 8858LM

Table 2: (Continued)

Device Number	Process	ROM Size [bits]	RAM Size [bits]	Package	Ambient Temperature Range [°C]	Serial Port Output Latch	Serial Buffer	Nesting Levels
MB 88201-P	CMOS	512 x 8	16 x 4	DIP	–40 to +85	–	–	2
MB 88201-PF	CMOS	512 x 8	16 x 4	FPT	–40 to +85	–	–	2
MB 88201A-P	CMOS	512 x 8	16 x 4	DIP	–30 to +70	–	–	2
MB 88201A-PF	CMOS	512 x 8	16 x 4	FPT	–30 to +70	–	–	2
MB 88201H-P	CMOS	512 x 8	16 x 4	DIP	–40 to +85	–	–	2
MB 88201H-PF	CMOS	512 x 8	16 x 4	FPT	–40 to +85	–	–	2
MB 88202-P	CMOS	1K x 8	32 x 4	DIP	–40 to +85	–	–	4
MB 88202-PF	CMOS	1K x 8	32 x 4	FPT	–40 to +85	–	–	4
MB 88202A-P	CMOS	1K x 8	32 x 4	DIP	–30 to +70	–	–	4
MB 88202A-PF	CMOS	1K x 8	32 x 4	FPT	–30 to +70	–	–	4
MB 88202H-P	CMOS	1K x 8	32 x 4	DIP	–40 to +85	–	–	4
MB 88202H-PF	CMOS	1K x 8	32 x 4	FPT	–40 to +85	–	–	4
*MB 88205B-P	CMOS	1K x 8	32 x 4	DIP	–40 to +85	–	–	4
MB 88211-P	CMOS	1K x 8	32 x 4	DIP	0 to +70	–	–	4
MB 88401-P/-PSH	NMOS	4K x 8	192 x 4	DIP	–30 to +70	yes	4	8
MB 88401-PF	NMOS	4K x 8	192 x 4	FPT	–30 to +70	yes	4	8
MB 88401H-P/-PSH	NMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88401H-PF	NMOS	4K x 8	256 x 4	FPT	–30 to +70	yes	4	8
MB 88403H-P/-PSH	NMOS	2K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88403H-PF	NMOS	2K x 8	256 x 4	FPT	–30 to +70	yes	4	8
MB 88411-P/-PSH	NMOS	4K x 8	192 x 4	DIP	–30 to +70	yes	4	8
MB 88411-PF	NMOS	4K x 8	192 x 4	FPT	–30 to +70	yes	4	8
MB 88411H-P/-PSH	NMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88411H-PF	NMOS	4K x 8	256 x 4	FPT	–30 to +70	yes	4	8
MB 88413-P/-PSH	NMOS	2K x 8	192 x 4	DIP	–30 to +70	yes	4	8
MB 88413-PF	NMOS	2K x 8	192 x 4	FPT	–30 to +70	yes	4	8
MB 88413H-P/-PSH	NMOS	2K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88413H-PF	NMOS	2K x 8	256 x 4	FPT	–30 to +70	yes	4	8
MB 88421-PSH	NMOS	4K x 8	192 x 4	DIP	–30 to +70	yes	4	8
MB 88421H-PSH	NMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88422-PSH	NMOS	3K x 8	192 x 4	DIP	–30 to +70	yes	4	8
MB 88423-PSH	NMOS	2K x 8	128 x 4	DIP	–30 to +70	yes	4	8

Output Port Options[1]	PLA Output Port[2] [bits]	Optional On-chip Prescaler	On-chip Clock Generator	Features	Device Number
4	–	yes	yes	Low cost	MB 88201-P
4	–	yes	yes	Low cost	MB 88201-PF
4	–	yes	yes	Wide voltage range	MB 88201A-P
4	–	yes	yes	Wide voltage range	MB 88201A-PF
4	–	yes	yes	High speed	MB 88201H-P
4	–	yes	yes	High speed	MB 88201H-PF
4	–	yes	yes	Low cost	MB 88202-P
4	–	yes	yes	Low cost	MB 88202-PF
4	–	yes	yes	Wide voltage range	MB 88202A-P
4	–	yes	yes	Wide voltage range	MB 88202A-PF
4	–	yes	yes	High speed	MB 88202H-P
4	–	yes	yes	High speed	MB 88202H-PF
3	–	yes	yes	Low cost, VFD driver port [8 seg. x 8 digits]	*MB 88205B-P
3	–	yes (fixed)	yes	Low cost, A/D converter [8 bits x 1 channel]	MB 88211-P
3	4/8	yes	yes	Standard	MB 88401-P/-PSH
2	4/8	yes	yes	Standard	MB 88401-PF
4	4/8	yes	yes	High speed	MB 88401H-P/-PSH
4	4/8	yes	yes	High speed	MB 88401H-PF
4	4/8	yes	yes	High speed, ROM 2K version	MB 88403H-P/-PSH
4	4/8	yes	yes	High speed, ROM 2K version	MB 88403H-PF
3	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels]	MB 88411-P/-PSH
2	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels]	MB 88411-PF
4	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels], high speed	MB 88411H-P/-PSH
4	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels], high speed	MB 88411H-PF
3	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels], ROM 2K version	MB 88413-P/-PSH
2	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels], ROM 2K version	MB 88413-PF
4	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels], high speed, ROM 2K version	MB 88413H-P/-PSH
4	4/8	yes	yes	On-chip A/D converter [8 bits x 7 channels], high speed, ROM 2K version	MB 88413H-PF
3	4	yes	yes	Multiple I/O ports [57 I/O ports]	MB 88421-PSH
5	4	yes	yes	Multiple I/O ports [57 I/O ports], high-speed	MB 88421H-PSH
3	4	yes	yes	Multiple I/O ports [57 I/O ports], ROM 3K version	MB 88422-PSH
3	4	yes	yes	Multiple I/O ports [57 I/O ports], ROM 2K version	MB 88423-PSH

Table 2: (Continued)

Device Number	Process	ROM Size [bits]	RAM Size [bits]	Package	Ambient Temperature Range [°C]	Serial Port Output Latch	Serial Buffer	Nesting Levels
MB 88501-P/-PSH	CMOS	4K x 8	192 x 4	DIP	–40 to +85	yes	4	8
MB 88501-PF	CMOS	4K x 8	192 x 4	FPT	–40 to +85	yes	4	8
MB 88501A-P/-PSH	CMOS	4K x 8	192 x 4	DIP	–30 to +70	yes	4	8
MB 88501A-PF	CMOS	4K x 8	192 x 4	FPT	–30 to +70	yes	4	8
MB 88501H-P/-PSH	CMOS	4K x 8	256 x 4	DIP	–40 to +85	yes	4	8
MB 88501H-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4	8
MB 88503H-P/-PSH	CMOS	2K x 8	256 x 4	DIP	–40 to +85	yes	4	8
MB 88503H-PF	CMOS	2K x 8	256 x 4	FPT	–40 to +85	yes	4	8
MB 88505-P/-PSH	CMOS	4K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88505-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
MB 88505A-P/-PSH	CMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4/8	8
MB 88505A-PF	CMOS	4K x 8	256 x 4	FPT	–30 to +70	yes	4/8	8
MB 88505H-P/-PSH	CMOS	4K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88505H-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
MB 88507-P/-PSH	CMOS	2K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88507-PF	CMOS	2K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
*MB 88511-P/-PSH	CMOS	4K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
*MB 88511-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
*MB 88513-P/-PSH	CMOS	2K x 8	192 x 4	DIP	–40 to +85	yes	4/8	8
*MB 88513-PF	CMOS	2K x 8	192 x 4	FPT	–40 to +85	yes	4/8	8
MB 88514B-PSH	CMOS	6K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88515B-PSH	CMOS	8K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88516B-PSH	CMOS	4K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88517B-P	CMOS	4K x 8	256 x 4	DIP	–40 to +85	yes	4/8	8
MB 88521-PSH	CMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88521-PF	CMOS	4K x 8	256 x 4	FPT	–30 to +70	yes	4	8

Output Port Options[1]	PLA Output Port[2] [bits]	Optional On-chip Prescaler	On-chip Clock Generator	Features	Device Number
2	4/8	yes	yes	Standard	MB 88501-P/-PSH
2	4/8	yes	yes	Standard	MB 88501-PF
2	4/8	yes	yes	Wide voltage range	MB 88501A-P/-PSH
2	4/8	yes	yes	Wide voltage range	MB 88501A-PF
4	4/8	yes	yes	High speed	MB 88501H-P/-PSH
4	4/8	yes	yes	High speed	MB 88501H-PF
4	4/8	yes	yes	High speed, ROM 2K version	MB 88503H-P/-PSH
4	4/8	yes	yes	High speed, ROM 2K version	MB 88503H-PF
2	4	yes	yes	Serial buffer 4/8 bits	MB 88505-P/-PSH
2	4	yes	yes	Serial buffer 4/8 bits	MB 88505-PF
2	4	yes	yes	Serial buffer 4/8 bits, wide voltage range	MB 88505A-P/-PSH
2	4	yes	yes	Serial buffer 4/8 bits, wide voltage range	MB 88505A-PF
2	4	yes	yes	High speed, serial buffer 4/8 bits	MB 88505H-P/-PSH
2	4	yes	yes	High speed, serial buffer 4/8 bits	MB 88505H-PF
2	4	yes	yes	High speed, ROM 2K version	MB 88507-P/-PSH
2	4	yes	yes	High speed, ROM 2K version	MB 88507-PF
4	–	yes	yes	On-chip A/D converter [8 bits x 4 channels]	*MB 88511-P/-PSH
4	–	yes	yes	On-chip A/D converter [8 bits x 4 channels]	*MB 88511-PF
4	–	yes	yes	On-chip A/D converter [8 bits x 4 channels], ROM 2K version	*MB 88513-P/-PSH
4	–	yes	yes	On-chip A/D converter [8 bits x 4 channels], ROM 2K version	*MB 88513-PF
4	–	yes	yes	On-chip A/D converter [8 bits x 8 channels], multiple I/O ports [54 I/O ports], VFD driver port [18 seg. x 7 digits], ROM 6K version	MB 88514B-PSH
4	–	yes	yes	On-chip A/D converter [8 bits x 8 channels], multiple I/O ports [54 I/O ports], VFD driver port [18 seg. x 7 digits], ROM 8K version	MB 88515B-PSH
4	–	yes	yes	On-chip A/D converter [8-bits x 8 channels], VFD driver port [10 seg. x 7 digits]	MB 88516B-PSH
4	–	yes	yes	On-chip A/D converter [8-bits x 4 channels], VFD driver port [8 seg. x 6 digits]	MB 88517B-P
3	–	yes	yes	Multiple I/O ports [57 I/O ports]	MB 88521-PSH
2	–	yes	yes	Multiple I/O ports [57 I/O ports]	MB 88521-PF

Table 2: (Contined)

Device Number	Process	ROM Size [bits]	RAM Size [bits]	Package	Ambient Temperature Range [°C]	Serial Port Output Latch	Serial Buffer	Nesting Levels
*MB 88522-PSH	CMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88523-PSH	CMOS	2K x 8	256 x 4	DIP	–30 to +70	yes	4	8
MB 88523-PF	CMOS	2K x 8	256 x 4	FPT	–30 to +70	yes	4	8
MB 88525-PSH	CMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4/8	8
MB 88525B-PSH	CMOS	4K x 8	256 x 4	DIP	–30 to +70	yes	4/8	8
MB 88525B-PF	CMOS	4K x 8	256 x 4	FPT	–30 to +70	yes	4/8	8
MB 88535-P/-PSH[3]	CMOS	2K x 8	128 x 4	DIP	–30 to +70	option	4	4
MB 88535-PF[3]	CMOS	2K x 8	128 x 4	FPT	–30 to +70	option	4	4
MB 88536-P/-PSH[3]	CMOS	2K x 8	128 x 4	DIP	–30 to +70	option	4	4
MB 88536-PF[3]	CMOS	2K x 8	128 x 4	FPT	–30 to +70	option	4	4
MB 88541-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4	8
*MB 88543-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
*MB 88544-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
*MB 88545-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8
*MB 88546-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	4/8	8

Output Port Options[1]	PLA Output Port[2] [bits]	Optional On-chip Prescaler	On-chip Clock Generator	Features	Device Number
TBD	–	yes	yes	Multiple I/O ports [57 I/O ports], square wave output	*MB 88522-PSH
3	–	yes	yes	Multiple I/O ports [57 I/O ports], ROM 2K version	MB 88523-PSH
3	–	yes	yes	Multiple I/O ports [57 I/O ports], ROM 2K version	MB 88523-PF
3	–	yes	yes	Multiple I/O ports [57 I/O ports], serial buffer 4/8 bits	MB 88525-PSH
2	–	yes	yes	Multiple I/O ports [57 I/O ports], VFD driver port [8 seg. x 16 digits]	MB 88525B-PSH
2	–	yes	yes	Multiple I/O ports [57 I/O ports], VFD driver port [8 seg. x 16 digits]	MB 88525B-PF
2	–	yes	yes	On-chip D/A converter [6 bits x 3 channels]	MB 88535-P/-PSH[3]
2	–	yes	yes	On-chip D/A converter [6 bits x 3 channels]	MB 88535-PF[3]
2	–	yes	yes	On-chip D/A converter [6 bits x 3 channels, 13 bits x 1 channel]	MB 88536-P/-PSH[3]
2	–	yes	yes	On-chip D/A converter [6 bits x 3 channels, 13 bits x 1 channel]	MB 88536-PF[3]
2	–	yes	yes	On-chip LCD driver [24 segment output and 4 common output, programmable duty: static, 1/2, 1/3, and 1/4]	MB 88541-PF
2	–	yes	yes	On-chip LCD driver [32 segment output and 4 common output, programmable duty: static, 1/2, 1/3, and 1/4], serial buffer 4/8 bit	*MB 88543-PF
2	–	yes	yes	On-chip LCD driver [24 segment output and 4 common output, programmable duty: static, 1/2, 1/3, and 1/4] serial buffer 4/8 bit	*MB 88544-PF
2	–	yes	yes	On-chip LCD driver [32 segment output and 4 common output, programmable duty: static, 1/2, 1/3, and 1/4], two clock, serial buffer 4/8 bit	*MB 88545-PF
2	–	yes	yes	On-chip LCD driver [24 segment output and 4 common output, programmable duty: static, 1/2, 1/3, and 1/4], two clock, serial buffer 4/8 bit	*MB 88546-PF

Table 2: (Continued)

Device Number	Process	ROM Size [bits]	RAM Size [bits]	Package	Ambient Temperature Range [°C]	Serial Port Output Latch	Serial Buffer	Nesting Levels
MB 88551-PF	CMOS	8K x 8	256 x 4	FPT	–30 to +70	yes	4/8	8
MB 88551H-PF	CMOS	8K x 8	256 x 4	FPT	–30 to +70	yes	4/8	8
MB 88552-PF	CMOS	6K x 8	256 x 4	FPT	–30 to +70	yes	4/8	8
MB 88552H-PF	CMOS	6K x 8	256 x 4	FPT	–30 to +70	yes	4/8	8
MB 88561-PF	CMOS	3K x 8	192 x 4	FPT	–40 to +85	yes	–	4
*MB 88562-PF	CMOS	4K x 8	256 x 4	FPT	–40 to +85	yes	–	4

Notes:

1. Standard pull-up, high-current pull-up, standard open-drain, high-current open-drain, middle-current open-drain, high-voltage open-drain, and 12V-interface open-drain output port configurations are available on certain devices.
2. "4" means dual 4-bit parallel output, "8" means 8-bit parallel output. Either option is available.
3. MB 8850 series device.

* Under development.

Output Port Options[1]	PLA Output Port[2] [bits]	Optional On-chip Prescaler	On-chip Clock Generator	Features	Device Number
3	–	yes	yes	On-chip A/D converter [5 bits x 4 channels], programmable pulse generator [9 bits x 1], multiple I/O ports [68 I/O ports]	MB 88551-PF
3	–	yes	yes	On-chip A/D converter [5 bits x 4 channels], programmable pulse generator [9 bits x 1], multiple I/O ports [68 I/O ports], high speed	MB 88551H-PF
3	–	yes	yes	On-chip A/D converter [5 bits x 4 channels], programmable pulse generator [9 bits x 1], multiple I/O ports [68 I/O ports]	MB 88552-PF
3	–	yes	yes	On-chip A/D converter [5 bits x 4 channels], programmable pulse generator [9 bits x 1], Multiple I/O ports [68 I/O ports], high speed	MB 88552H-PF
2	–	–	yes	On-chip LCD driver [26 segment output and 2 common output, 1/2 duty], PLL, A/D converter [6 bits x 3 channels]	MB 88561-PF
2	–	–	yes	On-chip VFD driver [39 segment output],PLL, A/D converter [6 bits x 3 channels]	*MB 88562-PF

Table 3: PERIPHERAL INTEGRATED CIRCUITS FOR THE FUJITSU 4-BIT MCU FAMILY

Process	Device Number	Function	Features
NMOS	MB 88301A-P	D/A Converter	Pulsewidth modulation type, 6-bit x 3 ch. 13-bit x 1 ch., 4-bit data input
	MB 88303-P	TV Display Controller [for TV/VCR]	20 character x 9 lines, 5 x 7 dot matrix, 64 character types, programmable character size/position/blink, parallel data input, character generator ROM
	MB 88304-P	I/O Expander [open-drain output]	4-bit x 4 ch. I/O ports, parallel/AND/OR I/O ports, power on reset
	MB 88305-P	I/O Expander [3 state output]	4-bit x 4 ch. I/O ports, parallel/AND/OR I/O ports, power on reset
CMOS	MB 88306-P/-PF	Output Expander	Rising-edge-triggered shift clock input, 8-bit CMOS data output, serial I/O
	MB 88307-P/-PF	Output Expander	Rising-edge-triggered shift clock input, 8-bit N-ch. open-drain data output, serial I/O
	MB 88308-P/-PF	Output Expander	Falling-edge-triggered shift clock input, 8-bit CMOS data output, serial I/O
	MB 88309-P/-PF	Output Expander	Falling-edge-triggered shift clock input, 8-bit N-ch. open-drain data output, serial I/O
	MB 88310-P	I/O Expander [open-drain output]	CMOS version of MB 88304
	MB 88311-P	I/O Expander [3 state output]	CMOS version of MB 88305
	MB 88313-P	TV Display Controller [for TV/VCR]	16(8) characters x 1(2), line(s), 5 x 7 dot matrix, 32 character types, programmable character size/position/blink, serial data input, character generator ROM
	*MB 88321-P	TV Display Controller [for TV, ROM version]	20 characters x 9 lines, 8 x 8 dot matrix, 64 character types, programmable character size/position/blink, serial data input, character generator ROM, RGB outputs
	*MB 88322-P	TV Display Controller [for TV, RAM version]	Character generator RAM version of MB 88321
	MB 88323-P	TV Display Controller [for VCR, ROM version]	20 characters x 9 lines, 8 x 8 dot matrix, 64 character types, programmable character size/position/blink, serial data input, character generator ROM, V & H sync generation
	MB 88324-P	TV Display Controller [for VCR, RAM version]	Character generator RAM version of MB 88323

* Under development

Package	Supply Voltage	Ambient Temperature Range [°C]	Typical Operating Clock Frequency [MHz]	Process
DIP-16P-M02	5.0 ± 10%	–30 to +70	4.0	NMOS
DIP-22P-M02/ FPT-24P-M02	5.0 ± 10%	–30 to +70	6.0	
DIP-24P-M01	5.0 ± 10%	–30 to +70	–	
DIP-24P-M01	5.0 ± 10%	–30 to +70	–	
DIP-16P-M02/ FPT-16P-M02	5.0 ± 10%	–40 to +85	2.0	CMOS
DIP-16P-M02/ FPT-16P-M02	5.0 ± 10%	–40 to +85	2.0	
DIP-16P-M02/ FPT-16P-M02	5.0 ± 10%	–40 to +85	2.0	
DIP-16P-M02/ FPT-16P-M02	5.0 ± 10%	–40 to +85	2.0	
DIP-24P-M01	5.0 ± 10%	–40 to +85	–	
DIP-24P-M01	5.0 ± 10%	–40 to +85	–	
DIP-16P-M02/ FPT-16P-M02	5.0 ± 10%	–30 to +70	6.0	
DIP-22P-M02	5.0 ± 10%	–30 to +70	TBD	
DIP-22P-M02	5.0 ± 10%	–30 to +70	TBD	
DIP-22P-M02	5.0 ± 10%	–30 to +70	7.16	
DIP-22P-M02	5.0 ± 10%	–30 to +70	7.16	

Table 4: PIGGYBACK EPROM TYPE EVALUATION DEVICES FOR THE FUJITSU 4-BIT FAMILY

Device Number[1]	Applicable Series/ Devices	Process	Piggyback EPROM	External ROM Size [bits]	Package	Supply Voltage	Ambient Temperature Range [°C]	RAM Size [bits]
MB 8850U1-C-401E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U1-C-402E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U1-C-403E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U1-C-411E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U1-C-412E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U1-C-413E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U2-C-401E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U2-C-402E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U2-C-403E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U2-C-411E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U2-C-412E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850U2-C-413E	MB 8840/50	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850H-C-001	MB 8840H/50H	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 8850H-C-002	MB 8840H/50H	CMOS	MBM 27C32A	4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	128 x 4
MB 88408U-C-001E	MB 88400	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	192 x 4
MB 88408U-C-002E	MB 88400	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	192 x 4
MB 88408U-C-003E	MB 88400	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	192 x 4
MB 88408H-C-101	MB 88400H	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	256 x 4
MB 88408H-C-111	MB 88400H	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	256 x 4
MB 88418-C-001E	MB 88410	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	192 x 4
MB 88418H-C-101	MB 88410H	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	256 x 4
MB 88418H-C-111	MB 88410H	NMOS	MBM 2732A	4K x 8	MDP-42C-P03	5.0 ± 10%	–30 to +70	256 x 4
MB 88428-C-101	MB 88420	NMOS	MBM 2764/ MBM 2732A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
*MB 88428-C-102	MB 88420	NMOS	MBM 2764/ MBM 2732A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4

Number of Instruc-tions	Output Port	PLA Output Mask Number	Serial Port Output Latch	On-chip Prescaler	Oscillation Type	Standby Function	Output Port Level During Standby	Serial Buffer	Output Port Level During Reset	Device Number
70	standard open-drain	#001[2]	yes	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U1-C-401E
70	standard open-drain	#002[3]	yes	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U1-C-402E
70	standard open-drain	#003[4]	yes	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U1-C-403E
70	standard pull-up	#001[2]	yes	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U1-C-411E
70	standard pull-up	#002[3]	yes	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U1-C-412E
70	standard pull-up	#003[4]	yes	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U1-C-413E
70	standard open-drain	#001[2]	no	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U2-C-401E
70	standard open-drain	#002[3]	no	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U2-C-402E
70	standard open-drain	#003[4]	no	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U2-C-403E
70	standard pull-up	#001[2]	no	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U2-C-411E
70	standard pull-up	#002[3]	no	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U2-C-412E
70	standard pull-up	#003[4]	no	yes/no[5]	crystal/ ceramic	yes/no[5]	high-Z	4	high	MB 8850U2-C-413E
70	standard[10] open-drain	#001[2]	no	yes/no[5]	crystal/ ceramic	yes/no[11] (soft)	hold	4	low	MB 8850H-C-001
70	standard[10] open-dran	#001[2]	yes	yes/no[5]	crystal/ ceramic	yes/no[12] (hard)	hold	4	high	MB 8850H-C-002
75	high-current open-drain	#001[2]	yes	yes/no[5]	crystal ceramic	no	–	4	high	MB 88408U-C-001E
75	high-current open-drain	#002[3]	yes	yes/no[5]	crystal/ ceramic	no	–	4	high	MB 88408U-C-002E
75	high-current open-drain	#003[4]	yes	yes/no[5]	crystal/ ceramic	no	–	4	high	MB 88408U-C-003E
76	high-current open-drain	#001[2]	yes	yes/no[5]	crystal/ ceramic	no	–	4	high	MB 88408H-C-101
76	high-current open-drain	#001[2]	yes	yes/no[5]	crystal/ ceramic	no	–	4	low	MB 88408H-C-111
74	high-current open-drain	#001[2]	yes	yes/no[5]	crystal/ ceramic	no	–	4	high	MB 88418-C-001E
75	high-current open-drain	#001[2]	yes	yes/no[5]	crystal/ ceramic	no	–	4	high	MB 88418H-C-101
75	high-current open-drain	#001[2]	yes	yes/no[5]	crystal/ ceramic	no	–	4	low	MB 88418H-C-111
81	standard pull-up	none	yes	yes	crystal/ ceramic	no	–	4	high	MB 88428-C-101
81	standard open-drain	none	yes	yes	crystal/ ceramic	no	–	4	high	*MB 88428-C-102

Table 4: (Continued)

Device Number[1]	Applicable Series/ Devices	Process	Piggyback EPROM	External ROM Size [bits]	Package	Supply Voltage	Ambient Temperature Range [°C]	RAM Size [bits]
MB 88428H-C-201	MB 88420H	NMOS	MBM 2764/ MBM 2732A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88428H-C-202	MB 88420H	NMOS	MBM 2764/ MBM 2732A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88428H-C-203	MB 88420H	NMOS	MBM 2764/ MBM 2732A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88508-C-101	MB 88501	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P03	5.0 ± 10%	–40 to +85	256 x 4
MB 88508-CF-101[6]	MB 88501	CMOS	MBM 27C64[7]	8K x 8	MQP-48C-P01	5.0 ± 10%	–40 to +85	256 x 4
MB 88508U-C-101	MB 88505/507	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P03	5.0 ± 10%	–40 to +85	256 x 4
MB 88508U-CF-101[6]	MB 88505/507	CMOS	MBM 27C64[7]	8K x 8	MQP-48C-P01	5.0 ± 10%	–40 to +85	256 x 4
MB 88508U-C-102	MB 88505/507	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P03	5.0 ± 10%	–40 to +85	256 x 4
MB 88508U-CF-102[6]	MB 88505/507	CMOS	MBM 27C64[7]	8K x 8	MQP-48C-P01	5.0 ± 10%	–40 to +85	256 x 4
MB 88508H-C-101	MB 88501H/ 503H	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	256 x 4
MB 88508H-CF-101[6]	MB 88501H/ 503H	CMOS	MBM 27C64[7]	8K x 8	MQP-48C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88508H-C-102	MB 88501H/ 503H	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	256 x 4
*MB 88508H-CF-102[6]	MB 88501H/ 503H	CMOS	MBM 27C64[7]	8K x 8	MQP-48C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG517B-C-201	MB 88517B	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	256 x 4
MB 88PG517B-C-202	MB 88517B	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-42C-P04	5.0 ± 10%	–40 to +85	256 x 4
MB 88518B-C-101	MB 88514B/ 515B/516B	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ±10%	–40 to +85	256 x 4
MB 88518B-C-102	MB 88514B/ 515B/516B	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–40 to +85	256 x 4
MB 88528-C-101	MB 88521/523	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88528-C-102	MB 88521/523	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88528-C-301	MB 88525	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88528-C-302	MB 88525	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88528B-C-101	MB 88520B	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88528B-C-102	MB 88520B	CMOS	MBM 27C64/ MBM 27C32A	8K x 8 4K x 8	MDP-64C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88538-C-201E[68]	MB 88535	CMOS	MBM 27C32A[7]	4K x 8	MDP-42C-P01	5.0 ± 10%	–30 to +70	128 x 4
MB 88538-C-202E[68]	MB 88536	CMOS	MBM 27C32A[7]	4K x 8	MDP-42C-P01	5.0 ± 10%	–30 to +70	128 x 4

Number of Instructions	Output Port	PLA Output Mask Number	Serial Port Output Latch	On-chip Prescaler	Oscillation Type	Standby Function	Output Port Level During Standby	Serial Buffer	Output Port Level During Reset	Device Number
82	standard pull-up	none	yes	yes	crystal/ ceramic	no	—	4	high	MB 88428H-C-201
82	high-current open-drain	none	yes	yes	crystal/ ceramic	no	—	4	high	MB 88428H-C-202
82	high-current open-drain	none	yes	yes	crystal/ ceramic	no	—	4	low	MB 88428H-C-203
77	standard pull-up	#001[2]	yes	yes	crystal/ ceramic	yes	high-Z	4	high	MB 88508-C-101
77	standard pull-up	#001[2]	yes	yes	crystal/ ceramic	yes	high-Z	4	high	MB 88508CF-101[6]
77	standard pull-up	#001[2]	yes	yes	crystal/ ceramic	yes	high-Z	4/8[9]	high	MB 88508U-C-101
77	standard pull-up	#001[2]	yes	yes	crystal/ ceramic	yes	high-Z	4/8[9]	high	MB 88508U-CF-101[6]
77	high-current open-drain	#001[2]	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	high	MB 88508U-C-102
77	high-current open-drain	#001[2]	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	high	MB 88508U-CF-102[6]
78	standard pull-up	#001[2]	yes	yes	crystal/ ceramic	yes	high-Z	4	high	MB 88508H-C-101
78	standard pull-up	#001[2]	yes	yes	crystal/ ceramic	yes	high-Z	4	high	MB 88508H-CF-101[6]
78	high-current open-drain	#001[2]	yes	yes	crystal/ ceramic	yes	hold	4	high	*MB 88508H-C-102
78	high-current open-drain	#001[2]	yes	yes	crystal/ ceramic	yes	hold	4	high	*MB 88508H-CF-102[6]
81	standard pull-up	none	yes	yes	crystal/ ceramic	no	—	4/8[9]	high	*MB 88PG517B-C-201
81	standard open-drain	none	yes	yes	crystal/ ceramic	no	—	4/8[9]	high	MB 88PG517B-C-202
81	high-current pull-up	none	yes	yes	crystal/ ceramic	yes	high-Z	4/8[9]	E0-E24: L other : H	MB 88518B-C-101
81	high-current open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	E0-E24: L other : H	MB 88518B-C-102
82	standard pull-up	none	yes	yes	crystal/ ceramic	yes	high-Z	4	high	MB 88528-C-101
82	standard[10] open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4	high	MB 88528-C-102
82	standard pull-up	none	yes	yes	crystal/ ceramic	yes	high-Z	4/8[9]	high	MB 88528-C-301
82	standard[10] open-drain	none	yes	yes	crystal ceramic	yes	hold	4/8[9]	high	MB 88528-C-302
81	standard pull-up	none	yes	yes	RC-network	yes	high-Z	4/8[9]	E0-E23: L other : H	MB 88528B-C-101
81	standard open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	E0-E23: L other : H	MB 88528B-C-102
70	standard pull-up	none	yes	yes	crystal/ ceramic	no	—	4	high	MB 88538-C-201E[68]
70	standard pull-up	none	yes	yes	crystal/ ceramic	no	—	4	high	MB 88538-C-202E[68]

2

Table 4: (Continued)

Device Number[1]	Applicable Series/ Devices	Process	Piggyback EPROM	External ROM Size [bits]	Package	Supply Voltage	Ambient Temperature Range [°C]	RAM Size [bits]
*MB 88PG543-CF-XXX	MB 88543	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG543-CF-XXX	MB 88543	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG544-CF-XXX	MB 88544	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG544-CF-XXX	MB 88544	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG545-CF-XXX	MB 88545	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG545-CF-XXX	MB 88545	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG546-CF-XXX	MB 88546	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
*MB 88PG546-CF-XXX	MB 88546	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–40 to +85	256 x 4
MB 88558-CF-101[6]	MB 88550	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	-30 to +70	256 x 4
MB 88558-CF-102[6]	MB 88550	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88558-CF-103[6]	MB 88550	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88558H-CF-101[6]	MB 88550H	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88558H-CF-102[6]	MB 88550H	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–30 to +70	256 x 4
MB 88558H-CF-103[6]	MB 88550H	CMOS	MBM 27C64[7]	8K x 8	MQP-80C-P01	5.0 ± 10%	–30 to +70	256 x 4

Notes:

1. -C designates a ceramic DIP package, and -CF, a ceramic FPT package. E indicates that the EPROM is attached to the package.
2. Dual 4-bit parallel output
3. 8-bit parallel output for 7-segment LED/dual 4-bit parallel output
4. 8-bit parallel output for 7-segment LED
5. Selectable using external control pin
6. For evaluation only
7. LCC package (MBM 27C32A-CV, MBM 27C64-CV except for MB 88508/U, MBM 27C64-MCV for MB 88508/U)
8. Multi-chip ceramic package configuration
9. Software selectable
10. P-Port is 12V-interface open-drain output port.
11. Soft: Software standby initiation
12. Hard: Hardware standby initiation

* Under development.

Number of Instruc-tions	Output Port	PLA Output Mask Number	Serial Port Output Latch	On-chip Prescaler	Oscillation Type	Standby Function	Output Port Level During Standby	Serial Buffer	Output Port Level During Reset	Device Number
78	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG543-CF-XXX
78	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG543-CF-XXX
82	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG544-CF-XXX
82	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG544-CF-XXX
78	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG545-CF-XXX
78	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG545-CF-XXX
82	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG546-CF-XXX
82	TBD	none	yes	yes	TBD	yes	TBD	4/8[9]	TBD	*MB 88PG546-CF-XXX
82	standard pull-up	none	yes	yes	crystal/ ceramic	yes	high-Z	4/8[9]	high	MB 88558-CF-101[6]
82	high-current open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	high	MB 88558-CF-102[6]
82	high-current open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	R0-R7: L other : H	MB 88558-CF-103[6]
82	standard pull-up	none	yes	yes	crystal/ ceramic	yes	high-Z	4/8[9]	high	MB 88558H-CF-101[6]
82	high-current open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	high	MB 88558H-CF-102[6]
82	high-current open-drain	none	yes	yes	crystal/ ceramic	yes	hold	4/8[9]	R0-R7: L other : H	MB 88558H-CF-103[6]

Table 5: EVALUATION BOARDS FOR THE FUJITSU 4-BIT MCU FAMILY

Device Number	Description	Applicable Series/Devices	Dimensions [mm]	Device Number
MB 2115-01	CRT unit	All	319 x 510 x 325	MB 2115-01
MB 2115-02	Monitor board with keyboard	All	283 x 328 x 66	MB 2115-02
MB 2115-04	EPROM writer board with RS-232C interface	All	140.5 x 152	MB 2115-04
MB 2115-13[1]	DUE[2] board	MB 88400	160 x 284	MB 2115-13[1]
MB 2115-13A[1] & MB 2115-89[3]	DUE board & DUE adapter	MB 88400H	160 x 284 160 x 284	MB 2115-13A[1] & MB 2115-89[3]
MB 2115-14[1]	DUE board	MB 88410	160 x 284	MB 2115-14[1]
MB2115-14A[1] & MB 2115-89[3]	DUE board & DUE adapter	MB 88410H	160 x 284 160 x 284	MB 2115-14A[1] & MB 2115-89[3]
MB 2115-31A[1] & MB 2115-89[3]	DUE board & DUE adapter	MB 88500/500H	160 x 284 160 x 284	MB 2115-31A[1] & MB 2115-89[3]
MB 2115-32[1]	DUE board	MB 88541	200 x 284	MB 2115-32[1]
MB 2115-33A[1]	DUE board	MB 8840/50H/ 200/200H	160 x 284	MB 2115-33A
MB 2115-33A[1] & MB 2115-94	DUE board & DUE adapter	MB 8850B	160 x 284 135 x 190	MB 2115-33A[1] & MB 2115-94
MB 2115-33A[1] & MB 2115-98	DUE board & DUE adapter	MB 88530	160 x 284 100 x 100	MB 2115-33A[1] & MB 2115-98
MB 2115-34[1] & MB 2115-96 & MB 2115-92[4]	DUE board & DUE adapter & SDIP 64-pin cable	MB 88510B (Except MB 88517B)	200 x 284 135 x 190	MB 2115-34[1] & MB 2115-96 & MB 2115-92[4]
MB 2115-35[1] & MB 2115-95 & MB 2115-92[4]	DUE board & DUE adapter & SDIP 64-pin cable	MB 88520B	200 x 284 135 x 190	MB 2115-35[1] & MB 2115-95 & MB 2115-92[4]
MB 2115-36A[1] & MB 2115-86[3]	DUE board & DUE adapter	MB 88550/550H	200 x 284 160 x 284	MB 2115-36A[1] & MB 2115-86[3]
MB 2115-37A[1] & MB 2115-88[3] & MB 2115-92[4]	DUE board & DUE adapter & SDIP 64-pin cable	MB 88520/420/420H	200 x 284 160 x 284	MB 2115-37A[1] & MB 2115-88[3] & MB 2115-92[4]
MB 2115-38[1]	DUE board	MB 88511/513/517B	200 x 284	MB 2115-38[1]
MB 2115-39[1]	DUE board	MB 88210	160 x 284	MB 2115-39[1]
MB 2115-40[1]	DUE board	MB 88561	200 x 430	MB 2115-40[1]
MB 2115-41[1]	DUE board	MB 88562	200 x 430	MB 2115-41[1]
*MB 2115-42[1]	DUE board	MB 88543/4/5/6	200 x 430	*MB 2115-42[1]
*MB 2115-43[1]	DUE board	MB 88200B	XXX x XXX	*MB 2115-43[1]

Notes:

1. Used in conjunction with the MB 2115-01 CRT unit and the MB 2115-02 monitor board with keyboard.
2. Device-Under-Evaluation.
3. This adapter applied to 12V-interface open-drain output port and select the port each bit.
4. MB 2115-92 is cable with SDIP 64-pin connector.

* Under development.

Table 6: SUPPORT SOFTWARE FOR THE FUJITSU 4-BIT MCU FAMILY

Order Number	Description	Media Supplied	Applicable Series	Support System
SM05212-A010	Cross-Assembler	8" standard floppy disk [single sided, single density or single sided, double density]	MB 8840/50/50H/ 0B/530	Intellec[1] Series II/III MDS
SM05220-A010			MB 88200/200H/200B/210	Intellec Series II/III MDS
SM05215-A010			MB 88400/400H/410/410H/420/ 420H/500/500H/510/510B/520/ 520B/540/550/550H/560	Intellec Series II/III MDS
SM07412-A012	Cross-Assembler	8" standard floppy disk [single sided, single density]	MB 8840/50/50H/50B/530	CP/M[2]-86
SM07420-A012			MB 88200/200H/200B/210	CP/M-86
SM07415-A012			MB 88400/400H/410/410H/420/ 420H/500/500H/510/510B/520/ 520B/540/550/550H/560	CP/M-86
*SMXXXXX-A010		5" mini floppy disk [double sided, double density]	MB 88400/400H/410/410H/420/ 420H/500/500H/510/510B/520/ 520B/540/550/550H/560	IBM PC-DOS
SM07412-G022[3]	Host-Emulator	8" standard floppy disk [single sided, single density]	MB 8840/50/50H/50B/530	CP/M-86
SM07420-G022[3]			MB 88200/200H/200B/210	CP/M-86
SM07415-G022[3]			MB 88400/400H/410/410H/420/ 420H/500/500H/510/510B/520/ 520B/540/550/550H/560	CP/M-86
*SMXXXXX-G020[3]		5" mini floppy disk [double sided, double density]	MB 88400/400H/410/410H/420/ 420H/500/500H/510/510B/520/ 520B/540/550/550H/560	IBM PC-DOS

Notes:

1. Intellec is a registered trademark of Intel Corporation.
2. CP/M is a registered trademark of Digital Research.
3. MB 2115-01, -02, -04 and an applicable DUE board are needed.

* Under development.

FUJITSU

NMOS 13-BIT×1-CHANNEL, 6-BIT×3-CHANNEL D/A CONVERTER

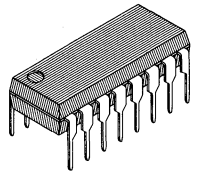
MB 88301A

April 1986
Edition 3.1

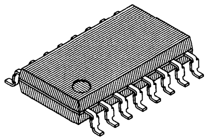
NMOS 13-BIT x 1-CHANNEL, 6-BIT x 3-CHANNEL D/A CONVERTER

The Fujitsu MB 88301A, a pulse width modulation (PWM) type digital-to-analog converter (DAC), is designed for interface with Fujitsu's MB 8840/8850 series and MB 88400/88500 series 4-bit single-ship microcomputers and also with a wide range of general 4-bit and 8-bit microprocessors.

The MB 88301A has four conversion outputs: one 13-bit resolution output and three 6-bit resolution outputs. All outputs generate positive pulse of varying pulse widths. The pulse widths vary in propotion to digital data programmed by the processor in the internal data register. With the connection of external filter circuits to the outputs, the MB 88301A provides an excellent, easy-to-configure DAC.



PLASTIC DIP
DIP-16P-M02

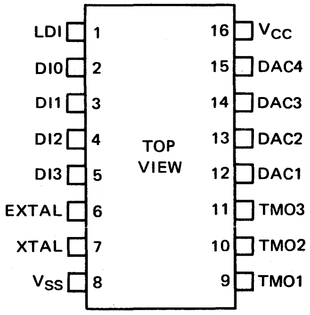


PLASTIC SOP
FPT-16P-M02

FEATURES

- Pulse width modulation D/A converter
- 4-bit parallel address/data loading
- Four on-chip pulse width modulators:
  - 13-bit resolution x 1 channel
  - 6-bit resolution x 3 channels
- On-chip 4 MHz clock generator with external crystal or ceramic resonator
- Clock cycle time / Clock frequency:
  - 0.25μs/4MHz for 13-bit resolution
  - 0.50μs/2MHz for 6-bit resolution
- Three synchronization clock outputs:
  - 2MHz clock output (4MHz divided by 2)
  - 15.625kHz clock output (4MHz divided by 2^8)
  - 488Hz clock output (4MHz divided by 2^{13})
- Single buffered conversion outputs.
- High-voltage open-drain conversion outputs
- Wide operating temperature range: -30°C to +70°C
- Single +5V power supply
- TTL compatible inputs/outputs
- N-channel silicon-gate E/D MOS process
- Two Package Options:
  - 16 pin plastic DIP (Suffix: -P)
  - 16 pin plastic SOP (Suffix: -PF)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — LOGIC SYMBOL

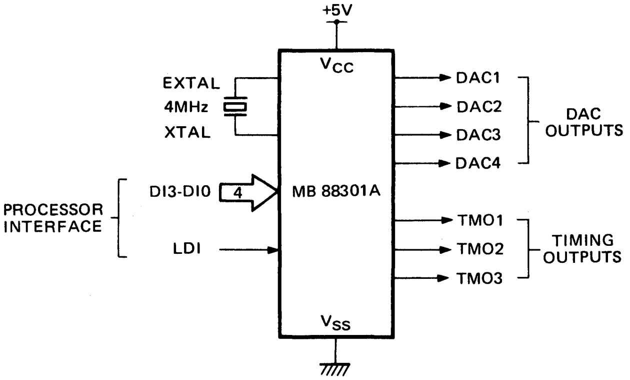
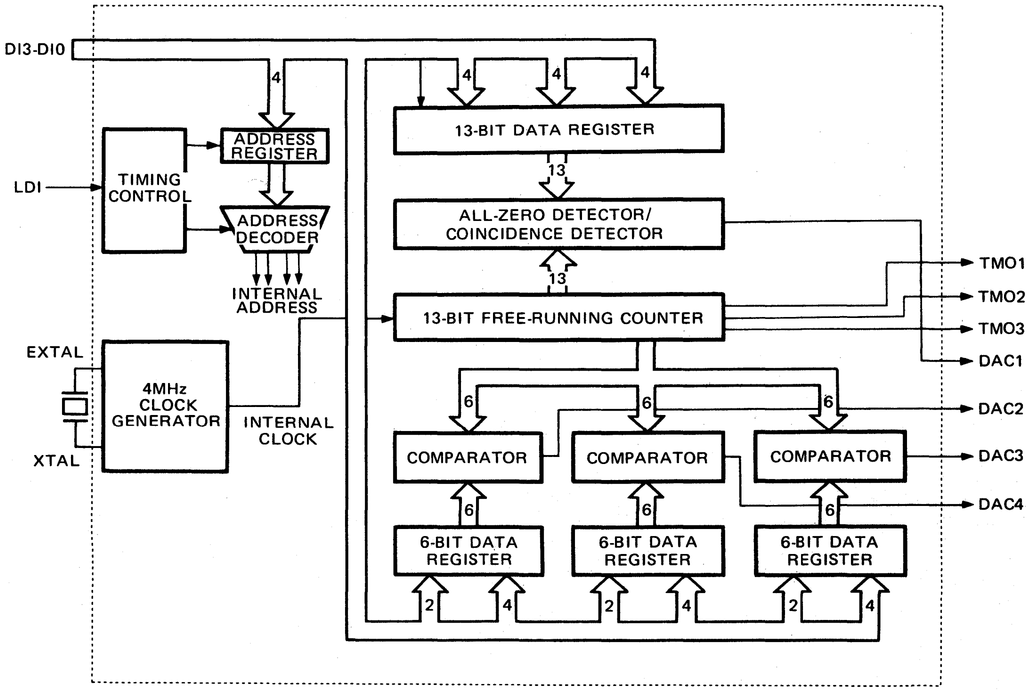


Fig. 2 — BLOCK DIAGRAM



PIN DESCRIPTION

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Function
V_{CC}	16	–	+5V power supply pin.
V_{SS}	8	–	Ground pin.
XTAL	7	–	External 4MHz crystal or ceramic resonator pins for the on-chip clock generator.
EXTAL	6	–	
DI3-DI0	5 to 2	I	4-bit parallel address/data input: The address/data format is that DI3 is the most significant bit (MSB) and that DI0 is the least significant bit (LSB). These inputs are TTL compatible. MSB LSB DI3 DI2 DI1 DI0
LDI	1	I	Write strobe input for a 4-bit address/data: At the leading edge of LDI, a 4-bit address on the ID3 to ID0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs are written into the internal data register designated by the address latched at the leading edge. This input is TTL compatible.
DAC1-DAC4	12 to 15	O	Pulse width modulator outputs (DAC outputs): DAC1: 13-bit resolution (one channel) DAC2-DAC4: 6-bit resolution (three channels) All four outputs are high-voltage open drain.
TMO1-TMO3	9 to 11	O	Synchronization clock outputs (Timing outputs): TMO1: 2MHz (4MHz divided by 2) TMO2: 15.625kHz (4MHz divided by 2^8) TMO3: 488Hz (4MHz divided by 2^{13}) All three clocks have a duty ratio of approximately 50%, and are TTL compatible.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MB 88301A is a pulse width modulation (PWM) type digital-to-analog converter (DAC). It converts digital data programmed by the processor in the internal data register (13-bit or 6-bit write-only register) into positive pulses. The width of these pulses is propotional to the value of the programmed data, and the cycle time of the pulses is defined by the resolution value (6 or 13 bits). The MB 88301A has four conversion outputs: channel 1 is a 13-bit resolution output DAC1, and channel 2 to 4 are 6-bit resolution outputs DAC2 to DAC4. The converted waveform appears at each DAC output. A user-designed external low-pass filter connected to the DAC output eliminates AC components from the output waveform and converts the waveform into a DC voltage propotional to the pulse width.

DIGITAL DATA INPUT

Fig. 4 shows the input timing of digital data to be converted: Digital data to define the width of the positive pulse is written into the 13-bit and 6-bit internal data registers through the DI3 to DI0 4-bit address/data inputs using the write strobe input LDI. At the leading edge of LDI, a 4-bit address on the DI3 to DI0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs is loaded into the internal data register designated by the address register.

Fig. 5 shows the address/data format: DI3 is the most significant bit (MSB) and DI0 is the least significant bit (LSB).

Fig. 3 – ADDRESS/DATA INPUT TIMING

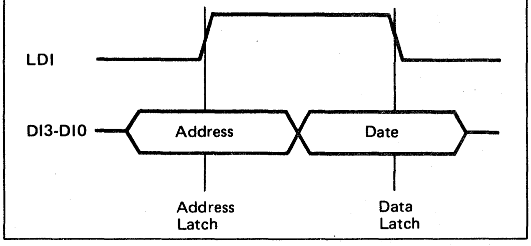


Fig. 4 – ADDRESS/DATA FORMAT

MSB			LSB
DI3	DI2	DI1	DI0

Fig. 6 shows the internal data register address map: The whole space size is 10 words. Addresses #0 to #3, addresses #4 and #5, addresses #6 and #7, and addresses #8 and #9 are assigned to DAC1, DAC2, DAC3 and DAC4, respectively. Fig. 7 shows the internal data register format: To the DAC1 data register, three 4-bit and one 1-bit digital data must be written. To the DAC2 to DAC4 data registers, one 4-bit and one 2-bit digital data must be written.

Fig. 5 – INTERNAL DATA REGISTER ADDRESS MAP

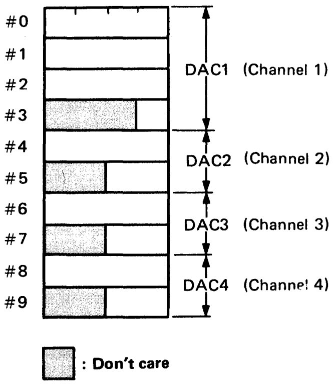
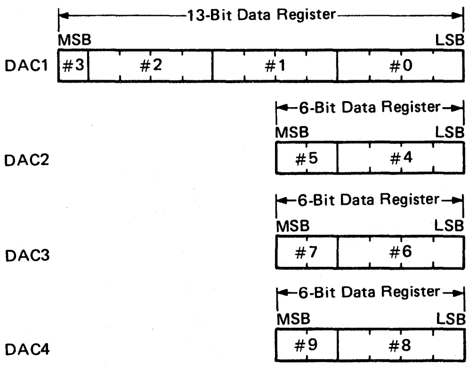


Fig. 6 – INTERNAL DATA REGISTER FORMAT



PULSE WIDTH MODULATION/DAC OUTPUT WAVEFORM

- **13-Bit Resolution D/A Converter: DAC1**

Fig. 8 shows the configuration of the 13-bit resolution pulse width modulator: The on-chip clock generater provides 4MHz clock for the 13-bit free-running counter. When all bits of the counter is zero, the all-zero detector sets the output R-R-S flip-flop. The coincidence detector compares the counter with the data register. When they match, the coincidence detector resets the output flip-flop. The waveform appearing at the DAC1 output depends on the data register value, shown in Fig. 9.

Fig. 7 — 13-BIT PULSE WIDTH MODULATOR CONFIGURATION

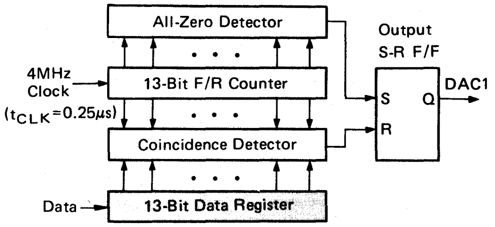
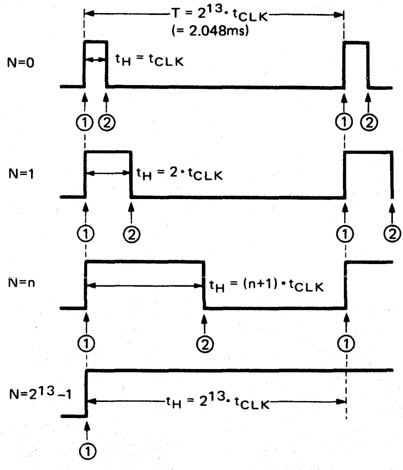


Fig. 8 — DAC1 OUTPUT WAVEFORM


$T = 2^{13} \cdot t_{CLK}$
(= 2.048ms)
N=0
$t_H = t_{CLK}$
① ②
N=1
$t_H = 2 \cdot t_{CLK}$
N=n
$t_H = (n+1) \cdot t_{CLK}$
$N=2^{13}-1$
$t_H = 2^{13} \cdot t_{CLK}$
①

NOTES: N : DATA REGISTER VALUE $(0 \leq N \leq 2^{13}-1)$
T : PULSE CYCLE TIME $(T = 2^{13} \cdot t_{CLK} = 2.048\text{ms})$
t_H : PULSE WIDTH $(t_H = (N+1) \cdot t_{CLK})$
t_{CLK} : COUNTER CLOCK CYCLE TIME $(t_{CLK} = 1/4\text{MHz} = 0.25\mu s)$
① : COUNTER IS ZERO.
② : COUNTER MATCHES DATA REGISTER.

- **6-Bit Resolution D/A Converters: DAC2 to DAC4**

Fig. 10 shows the configulation of the 6-bit resolution pulse width modulator: The 2MHz clock that is the output of Bit 1 of the 13-bit free-running counter drives the 6-bit free-running counter. This 6-bit counter is also part of the 13-bit counter (Bits 2 to 7). The comparator compares the counter with the data register every cycle. When the counter value is equal to or less than the data register value, the comparator outputs a high level at the DAC output. When the counter value exceeds the date register value, the comparator outputs a low level at the DAC output. This produces the waveforms at the DAC2, DAC3, and DAC4 outputs, shown in Fig. 11.

Fig. 9 — 6-BIT PULSE WIDTH MODULATOR CONFIGURATION

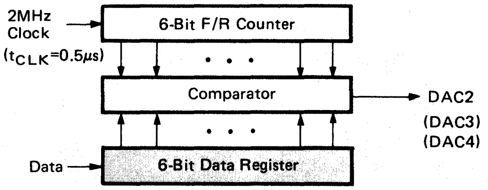
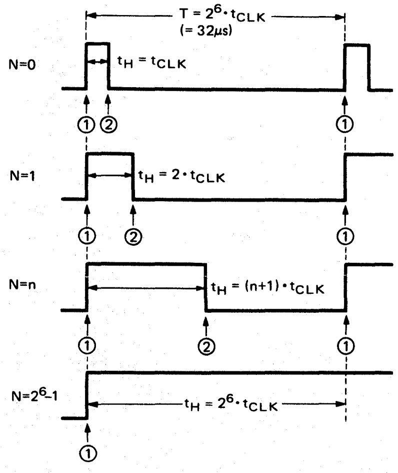


Fig. 10 — DAC2/DAC3/DAC4 OUTPUT WAVEFORM


$T = 2^{6} \cdot t_{CLK}$
(= 32μs)
N=0
$t_H = t_{CLK}$
① ②
N=1
$t_H = 2 \cdot t_{CLK}$
N=n
$t_H = (n+1) \cdot t_{CLK}$
$N=2^{6}-1$
$t_H = 2^{6} \cdot t_{CLK}$
①

NOTES: N : DATA REGISTER VALUE $(0 \leq N \leq 2^{6}-1)$
T : PULSE CYCLE TIME $(T = 2^{6} \cdot t_{CLK} = 32\mu s)$
t_H : PULSE WIDTH $(t_H = (N+1) \cdot t_{CLK})$
t_{CLK} : COUNTER CLOCK CYCLE TIME $(t_{CLK} = 1/2\text{MHz} = 0.5\mu s)$
① : COUNTER IS ZERO. (OVERFLOW)
② : COUNTER EXCEEDS DATA REGISTER.

EXTERNAL FILTER CONFIGURATION

The on-chip pulse width modulator generates positive pulse waveforms similar to the one shown in Fig. 13 at the DAC outputs (DAC1 to DAC4). The pulse width (t_H) is proportional to the digital data programmed into the data register. The cycle time (T) is determined by the resolution value (6 or 13 bits).

User-designed low-pass filters are required at the DAC outputs to eliminate AC components from the output waveform and to convert the waveform to a DC voltage. Fig. 12 shows an example of a simple output configuration in which an RC integrator is used as the low-pass filter. With this circuit, the DAC waveform shown in Fig. 13 is converted to the V_{OUT} output waveform shown in Fig. 14. Ripple and response time (t_R) depend on the time constant of the RC filter. A longer time constant reduces ripple but increases response time. A time constant that best meets the tradeoff between desired accuracy and response time should be chosen. Also, since the DAC outputs are high-voltage open drain, they can externally be pulled up to a power supply higher than 5V. This prevents the output voltage from attenuating through the external low-pass filters.

Note:
The low-pass filter shown in Fig. 12 is just an example. In actual practice, depending on the user's system design, additional amplifiers, multi-stage filters, and other circuits will be needed for the external low-pass filter.

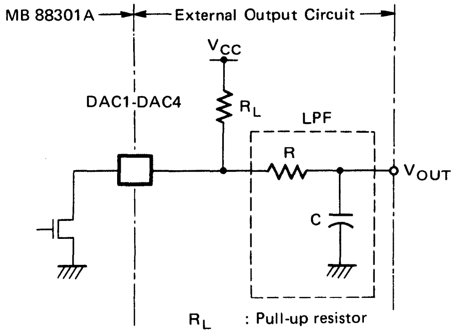
NOTICE

To change the DC output voltage of the external low-pass filter, the data register value must be updated to vary the positive pulse width (duty ratio) of the DAC output. However, all bits on the data register can not be changed at the same time. They are updated a nibble at a time by the 4-bit parallel data loading. In addition, the DAC output is single buffered. Because of this nibble-by-nibble update and single buffering, the data register value during update may become transient. During this pulse cycle, depending on the transient value, an undesirable duty ratio disturbance may occur at the DAC output, affecting the filter output. It is therefore necessary to design the output filter so that such disturbances in the DAC output waveform will not appear at the filter output. This notice applies to both the 13-bit and 6-bit resolution converters. With the 13-bit resolution converter, however, it is possible to avoid such disturbance by software. This is done by controlling the update timing of the data register value through monitoring of the DAC1 output and the TMO3 output waveforms.

Also, note the following thing when the DAC1 output is used: in the steady state where the DAC1 data register bits are all set (i.e., data is "1FFF") the DAC1 output remains high. But, when the data is updated, there is a possibility that the DAC1 output may become undefined during that output cycle time (less than one cycle time). To avoid this phenomenon, the following method is utilized:

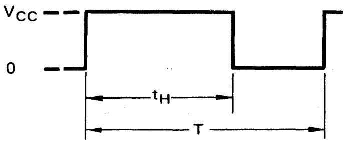
1. Not use data of "1FFF", or
2. Change the DAC1 data register value (i.e., "1FFF") just before the counter become full (i.e., all bits are set). Since in this case an undesired pulse due to the data change may appear at the DAC1 output, the pulse must be eliminated with the external filter.

Fig. 11 – OUTPUT CIRCUIT CONFIGURATION (EXAMPLE)



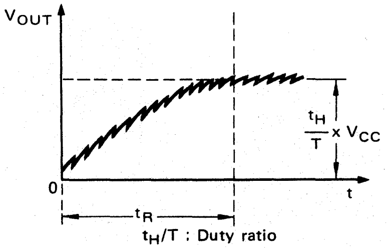
R_L : Pull-up resistor
LPF : Low-pass filter
V_{OUT} : LPF output voltage

Fig. 12 – DAC OUTPUT WAVEFORM



t_H : Pulse width
T : Cycle time

Fig. 13 – V_{OUT} OUTPUT WAVEFORM



t_H/T : Duty ratio
t_R : Response time
t : time

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Pins/Conditions	
Supply Voltage	V_{CC}	V_{SS} –0.3 to V_{SS} +8.0	V	V_{CC}	V_{SS} = 0 V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{SS} +8.0	V	DI0-DI3, LDI, EXTAL, XTAL	
Output Voltage	V_{OUT}	V_{SS} –0.3 to V_{SS} +15.0	V	DAC1-DAC4	
		V_{SS} –0.3 to V_{SS} +8.0		TMO1-TMO3	
Operating Temperature	T_A	–30 to +70	°C	Ambient temperature	
Storage Temperature	T_{stg}	–55 to +150	°C		

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}		0		
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}	- 0.3		0.8	V
Clock Frequency*	f_c	0.5		4.0	MHz
Operating Temperature	T_A	-30		70	°C

NOTE: * Crystal or ceramic resonator should be used. See Fig. 17.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Value			Unit
			Min.	Typ.	Max.	
Output High Voltage	V_{OH}	TMO1-TMO3 I_{OH} = –200μA	2.4			V
		DAC1-DAC4	Open Drain			
Output Low Voltage	V_{OL}	TMO1-TMO3 I_{OL} = 1.8mA			0.4	V
		DAC1-DAC4 I_{OL} = 2.0mA, 5kΩ External Pull Up Resistor			0.8	V
Output Leakage Current	I_{LOH}	DAC1-DAC4 V_{OH} = 13.2V, OFF State			50	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, All Outputs Open		15	25	mA

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Min.	Typ.	Max.	Unit
LDI Pulse Width	P_{WLDI}	LDI Fig. 14, Fig. 16	5			μs
LDI Rise/Fall times	t_{rLDI} t_{fLDI}	LDI Fig. 14, Fig. 16			1.5	μs
Address/Data Setup Time	t_S	DI3 - DI0 Fig. 14, Fig. 16	0.5			μs
Address/Data Hold Time	t_H	DI3 - DI0 Fig. 14, Fig. 16	2			μs
TMO Rise/Fall times	t_{rTMO} t_{fTMO}	TM01-TM03 Fig. 15, Fig. 16			0.2	μs

Fig. 14 — ADDRESS/DATA INPUT TIMING

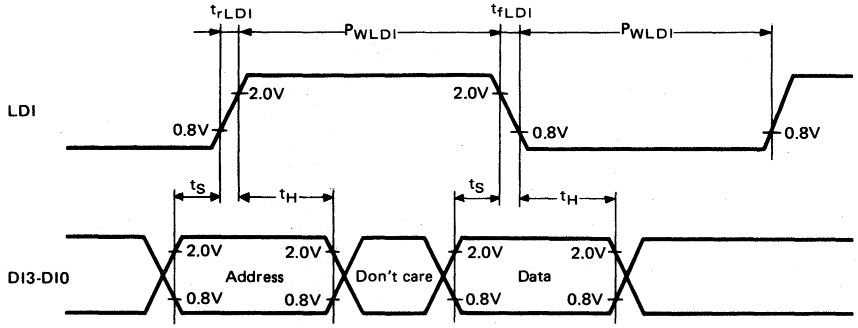


Fig. 15 — SYNCHRONIZATION CLOCK OUTPUT TIMING

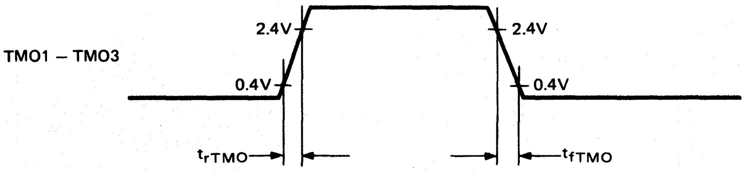
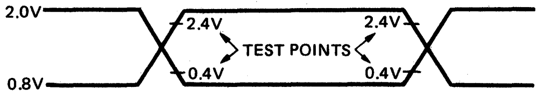


Fig. 16 – AC TEST CONDITIONS

INPUT CONDITIONS

- Input Levels:
  2.0V for a logic "1"
  0.8V for a logic "0"



OUTPUT CONDITIONS

- Timing Reference Levels:
  2.4V for a logic "1"
  0.4V for a logic "0"
- Output Load Circuit:
  C_L = 100pF (including scope and jig capacitances)
  R_L = 4kΩ

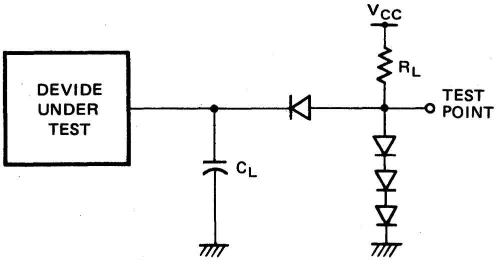
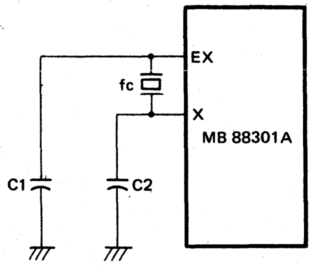


Fig. 17 – CRYSTAL/CERAMIC OSCILLATOR CIRCUIT

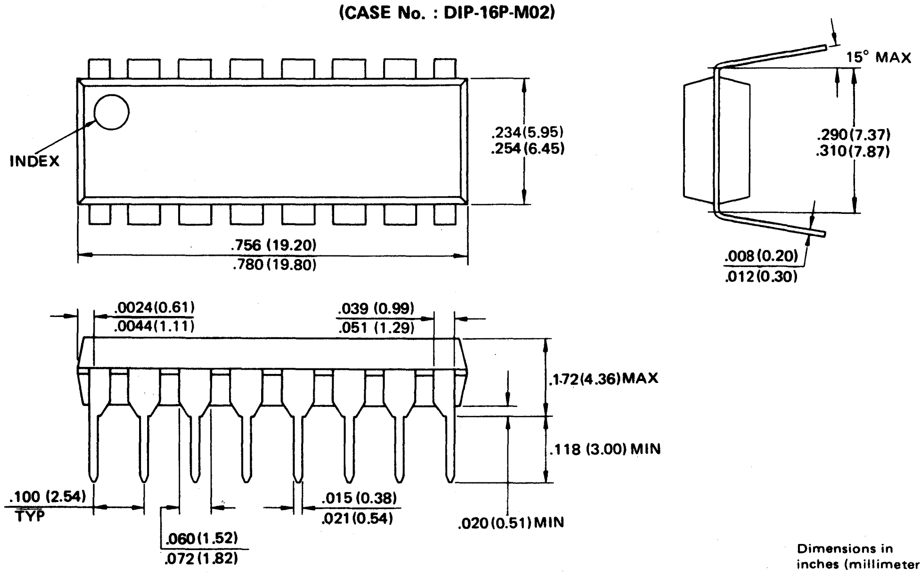


fc = 4MHz
C1 = C2 = 20pF – 60pF

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)

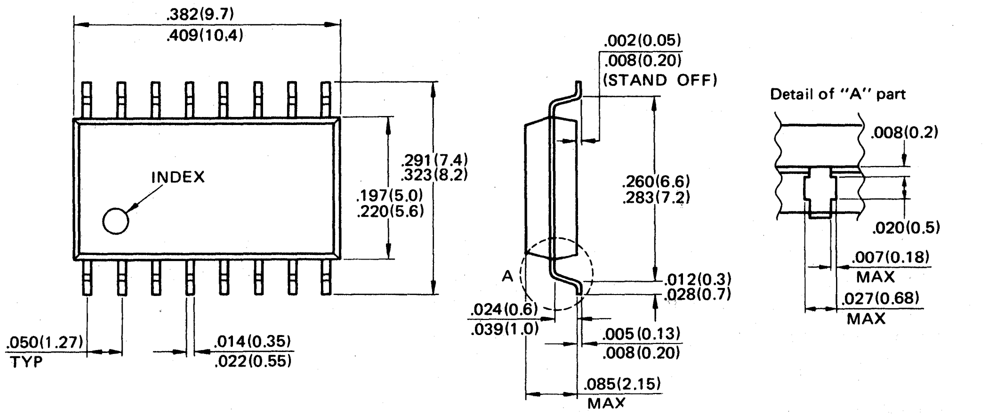


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC SOP(Suffix: -PF)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

FUJITSU

NMOS INPUT/OUTPUT EXPANDER

MB 88304
MB 88305

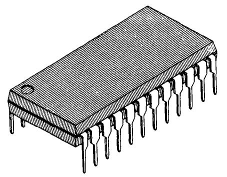
April 1986
Edition 1.1

NMOS INPUT/OUTPUT EXPANDER

The Fujitsu MB 88304/MB 88305 are peripheral integrated circuits that can be connected to a 4-bit or 8-bit single-chip microcomputer (MCU) to provide additional I/O ports. Besides furnishing simple I/O port expansion, the MB 88304 and MB 88305 can AND or OR port data with data from the MCU, on instruction from the MCU.

The MB 88304/MB 88305 are pseudo-bidirectional ports. They are accessed in 4-bit units, but each individual bit can be used for either input or output, and input and output can be intermixed. The interface to the MCU requires only the connection of a 4-bit interface port and a strobe signal. All output ports of the MB 88304 are open-drain; MB 88305 output ports all have pull-up resistors. The output ports on both chips are reset to the high-impedance state at power-up.

The MB 88304/MB 88305 are fabricated with N-channel silicon-gate E/D MOS process, and packaged in 24-pin plastic DIP. Also, they are powered with a single +5V power supply, and operate over the ambient temperature range of -30°C to +70°C.

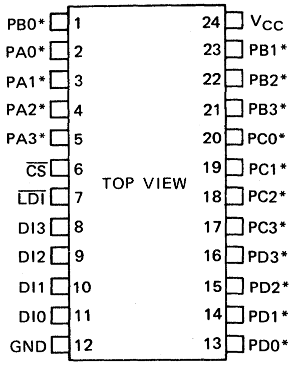


PLASTIC DIP
DIP-24P-M01

FEATURES

- Four 4-bit I/O ports (16 lines)
- Four Functions: parallel input, parallel output, AND output, and OR output
- AND and OR functions provide individual output capability
- Single-bit input/output: Input and output can be intermixed on each port
- High output drive
- Built-in power-on reset circuit
- $\overline{\text{CS}}$ pin for simplified input/output expansion
- Two output circuit types: Open-drain output (MB 88304)
  3-state output (MB 88305)
- Easily connectable to MCUs with 8243 interface
- Single +5V power supply
- -30°C to +70°C operating temperature range
- N-channel silicon-gate E/D MOS process
- 24-pin plastic DIP (Suffix: -P)

PIN ASSIGNMENT



* MB 88304: Open-drain output
  MB 88305: 3-state output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

LOGIC SYMBOL

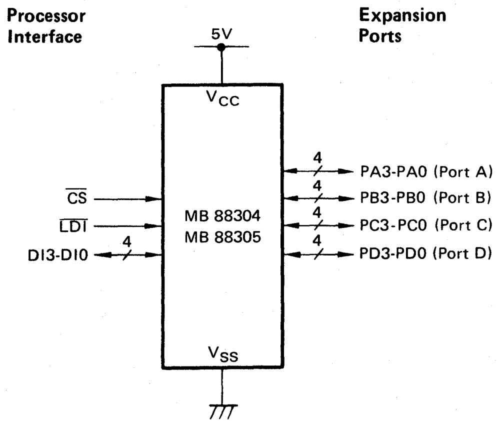
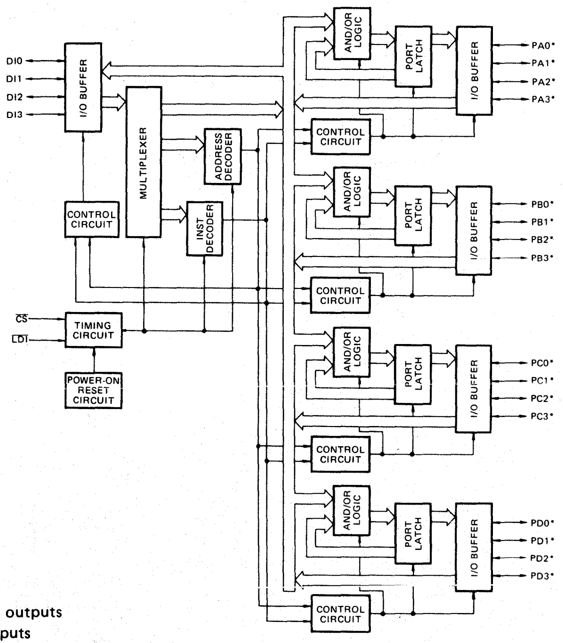


Fig. 1 — BLOCK DIAGRAM



* MB 88304: Open-drain outputs
MB 88305: 3-state outputs

PIN DESCRIPTION

The MB 88304/88305 have two interfaces: One is the processor interface; $\overline{\text{CS}}$, $\overline{\text{LDI}}$, and DI3—DI0, which are used for the processor to communicate with the MB 88304/5 devices. Another is the expansion I/O ports; Ports A, B, C, and D, which serve as an expansion of the processor's I/O.

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Name/Function
V_{CC}	24	–	**V_{CC}**: is the +5V power supply pin.
GND	12	–	**GND**: is the ground pin.
$\overline{\text{CS}}$	6	I	**Chip Select:** is a low-level-sense high-impedance input. A low level on this input selects the device. This input is TTL-compatible.
$\overline{\text{LDI}}$	7	I	**Load Data Input**: is an edge-triggered strobe input. The operation code and address code on DI0 to DI3 are latched at the $\overline{\text{LDI}}$ falling edge. The data transffered via DI0 to DI3 becomes valid on the rising edge of the $\overline{\text{LDI}}$ input.
DI3 to DI0	8 to 11	I/O	**Data Bus:** is a 4-bit bidirectional port used for interface to the MCU. The operation code and address code provided by the MCU on this port are latched at the falling edge of the $\overline{\text{LDI}}$ strobe input, and input/output data is transferred at the rising edge of the $\overline{\text{LDI}}$. The DI port remains in the high-impedance state except when the input operation is executed.
PA0 to PA3	2 to 5	I/O	**Ports A, B, C, and D** are 4-bit bidirectional ports used as expansion I/O ports. These four ports are addressed by address codes provided by the MCU. When an input operation code is given by the MCU, data on the addressed port is transferred to the DI0 to DI3 at the rising edge of the $\overline{\text{LDI}}$. When an output operation code is provided, data on the DI0 to DI3 is transferred and latched to the addressed port at the rising edge of the $\overline{\text{LDI}}$. Logical operations are also possible, in which data on the addressed port is ANDed or ORed with data on the DI0 to DI3 and the result is latched at the addressed port at the rising edge of the $\overline{\text{LDI}}$. After a power-on reset, Ports A to D are all set to the high-impedance state. An individual port is released from the high-impedance state when the OUT, AND, or OR function is applied to it. (Since the MB 88304 has open-drain outputs, a line returns to the high-impedance state when an "1" is written on it.)
PB0, PB1 to PB3	1, 21 to 23	I/O	
PC0 to PC3	20 to 17	I/O	
PD0 to PD3	16 to 13	I/O	

FUNCTIONAL DESCRIPTION

The four 4-bit I/O ports of the MB 88304 and MB 88305 are labelled port A, port B, port C, and port D (PA, PB, PC, and PD). They serve as expansion I/O ports for a one-chip microcomputer (MCU), and can be accessed via an MCU port. Their functions are as follows:

- Data transfer from the MCU to port A, B, C, or D
- Data transfer from port A, B, C, or D to the MCU
- ANDing of the port A, B, C, or D data with MCU data and latching of the result at port A, B, C, or D
- ORing of the port A, B, C, or D data with MCU data and latching of the result at port A, B, C, or D

For interface to the MCU, the MB 88304 and MB 88305 have a 4-bit interface port (DI0 to DI3), a strobe input ($\overline{\text{LDI}}$ pin), and a chip select input ($\overline{\text{CS}}$ pin). The interface data consists of two 4-bit units. The first 4 bits give the operation code (2-bits) and address code (2 bits). The second 4-bits are the input or output data. Both 4-bit units are transferred through the interface port (DI0 to DI3) on timings determined by the strobe ($\overline{\text{LDI}}$) signal. The MB 88304 or MB 88305 reads the operation code and address code from the MCU on the falling edge of the $\overline{\text{LDI}}$ signal, and sends or receives the I/O data on the rising edge of $\overline{\text{LDI}}$.

The $\overline{\text{CS}}$ pin is used to read a chip select signal from the MCU's I/O port when two or more MB 88304 or MB 88305 chips are connected to the MCU.

Ope. Code		Funciton	Addr. Code		Port Address
DI3	DI2		DI1	DI0	
0	0	IN (Input)	0	0	Port A (PA)
0	1	OUT (Output)	0	1	Port B (PB)
1	0	OR (Logical OR)	1	0	Port C (PC)
1	1	AND (Logical AND)	1	1	Port D (PD)

POWER-ON RESET

The MB 88304 and MB 88305 contain an internal power-on reset circuit that detects the rise of V_{CC} on the power supply line and holds the chip circuits in the reset state. In the reset state, the interface port (pins DI0 to DI3) is set to the input state, and ports A to D (PA to PD) are in the high-impedance state (except that latched output ports are not reset). The V_{CC} line must rise smoothly for the reset circuit to operate. Regardless of the input level (high of low) of the $\overline{\text{LDI}}$ pin at the moment power is applied, the reset state is released at the first falling edge of the $\overline{\text{LDI}}$ input. A power-on reset also occurs if the supply voltage (V_{CC}) drops to 1 V or less, then recovers to the rated voltage.

OUTPUT MODE (Write Mode)

Corresponding to three functions of the MCU, the MB 88304 and MB 88305 have three output modes: data transfer output (OUT), logical OR (OR), and logical AND (AND).

- OUT

The designated port latches and outputs the 4-bit data transferred from the MCU.

- AND

The 4-bit data transferred from the MCU is ANDed with the 4-bit data of the designated port, which then latches the result as output.

- OR

The 4-bit data transferred from the MCU is ORed with the 4-bit data of the designated port, which then latches the result as output.

The operation code and address code sent from the MCU to pins DI0 to DI3 of the MB 88304 or MB 88305 are latched on the falling edge of the strobe signal at the $\overline{\text{LDI}}$ pin. The MCU data is read on the rising edge of the strobe signal and sent to the logic circuit of the designated port, where it is processed. The MCU data is then latched as output data.

INPUT MODE (Read Mode)

The MB 88304 and MB 88305 have only one input mode (IN), corresponding to data input by the MCU.

- IN

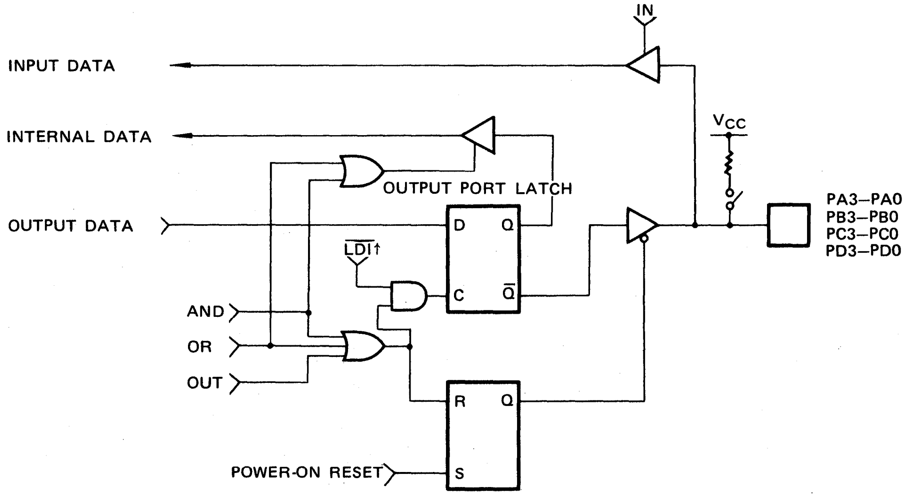
The input data at the port designated by the MCU is read and sent to the MCU via the interface port (DI0 to DI3).

The operation and address code sent from the MCU to pins DI0 to DI3 of the MB 88304 or MB 88305 are latched on the falling edge of the strobe signal at the $\overline{\text{LDI}}$ pin. If the operation code specifies input, the MB 88304 or MB 88305 sends data from the port designated by the address code to the MCU via DI0 to DI3.

A power-on reset places the chip in the input mode with ports A to D in the high-impedance state. If only the IN function is used thereafter, the ports remain in the high-impedance state. Release from the high-impedance state takes place when the OUT, AND, or OR function is used.

The MB 88304 and MB 88305 are designed for easy external driving. The MB 88304 has open-drain outputs, while the MB 88305 outputs have pull-up resistors. For both chips, the input level of a port to be used for input can be read by writing a 1 and performing the IN function. Input and output can therefore be intermixed within the four bits of each of the four ports (A to D).

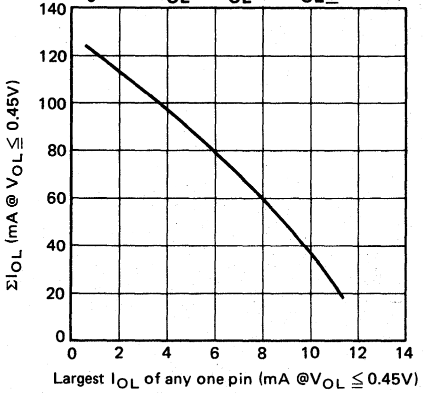
Fig. 2 – PORT CIRCUIT CONFIGURATION



SINK CURRENT FROM PORTS A TO D

When $V_{OL} \leqq 0.45V$, the MB 88304 and MB 88305 can sink 5mA (I_{OL}) on each of their 16 I/O lines simultaneously. When this current sinking capability is not required on all of the I/O lines, or not all of the lines have to sink 5mA, the driving capability (sink current) of the other I/O lines can be increased according to the characteristics shown in the curve below.

Fig. 3 – ΣI_{OL} vs I_{OL} (@ $V_{OL} \leqq 0.45V$)



For instance, if one of the I/O lines has to sink 9mA, the total I_{OL} (ΣI_{OL}) of all the lines can be up to 45mA.

Example-1: How many I/O lines with 5 TTL leads can be driven?

I_{OL} = 5 x 1.6mA = 8mA

$\Sigma I_{OL} \leqq$ 60mA (from the total I_{OL} characteristics curve)

60mA/8mA = 7 I/O lines

The chip can drive 7 lines with 5 TTL loads, making a total of 56mA on these lines. The remaining 4mA can be shared among the other 9 I/O lines.

Example-2: Suppose that two of the load lines have I_{OL} = 20mA (at $V_{OL} \leqq 1V$). Can the MB 88304 or MB 88305 drive the following loads?

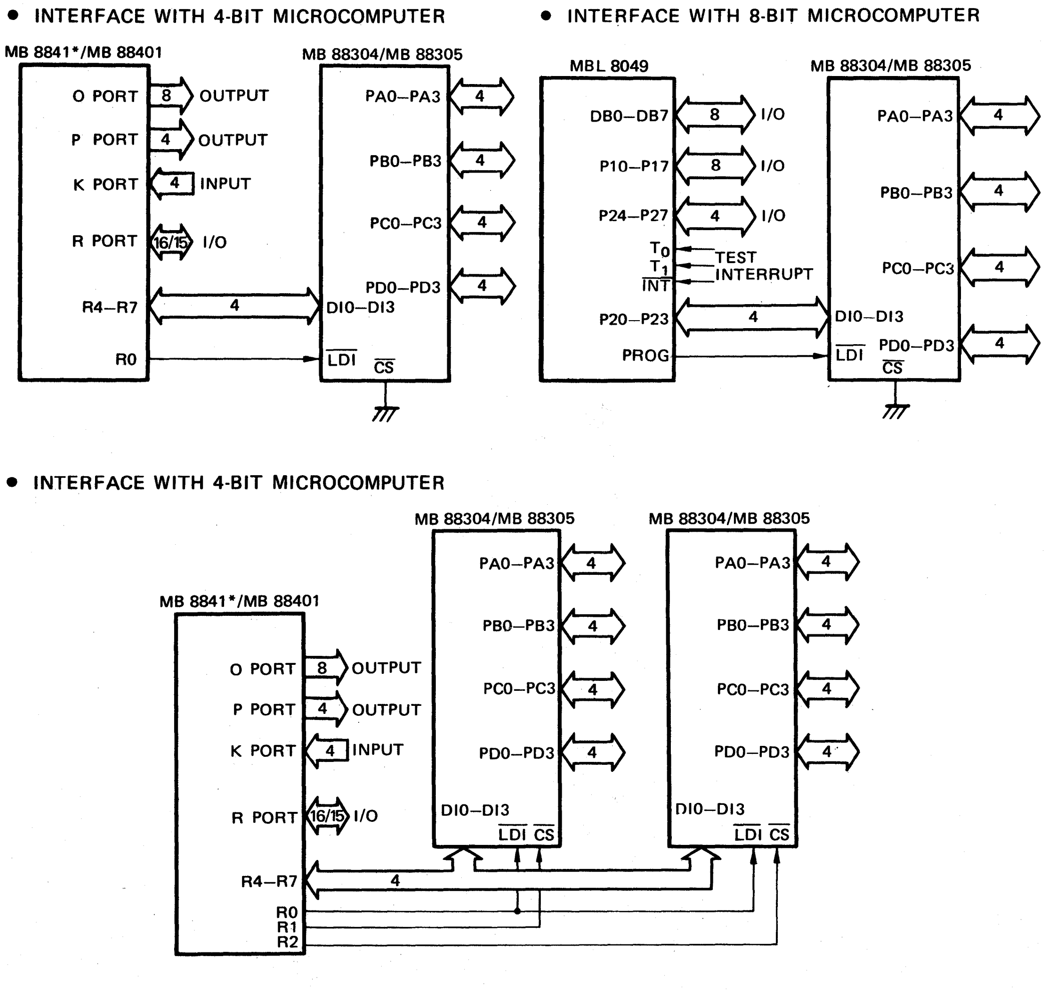
2 I/O lines: 20mA (at $V_{OL} \leqq 1V$)
8 I/O lines: 4mA (at $V_{OL} \leqq 0.45V$)
6 I/O lines: 3.2mA (at $V_{OL} \leqq 0.45V$)

Total I_{OL} = (2x20mA) + (8x4mA) + (6x3.2mA)
= 91.2mA

Reading the total I_{OL} characteristic for I_{OL} = 4mA, we see that $\Sigma I_{OL} \leqq$ 93mA. Since 91.2mA $\leqq$ 93mA, the chip can drive these loads.

Note: The allowable total I_{OL} (ΣI_{OL}) depends on the maximum sink current of the lines for which V_{OL} must be equal to or less than 0.45V.

Fig. 4 – TYPICAL APPLICATIONS


- INTERFACE WITH 4-BIT MICROCOMPUTER
- INTERFACE WITH 8-BIT MICROCOMPUTER
- INTERFACE WITH 4-BIT MICROCOMPUTER

NOTE: * Output port of MB 8841 should be open-drain type.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	V_{SS} -0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3 to +7.0	V
Operating Temperature	T_A	-30 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+5 ±10%	V
	V_{SS}	0	
Operating Temperature	T_A	-30 to +70	°C

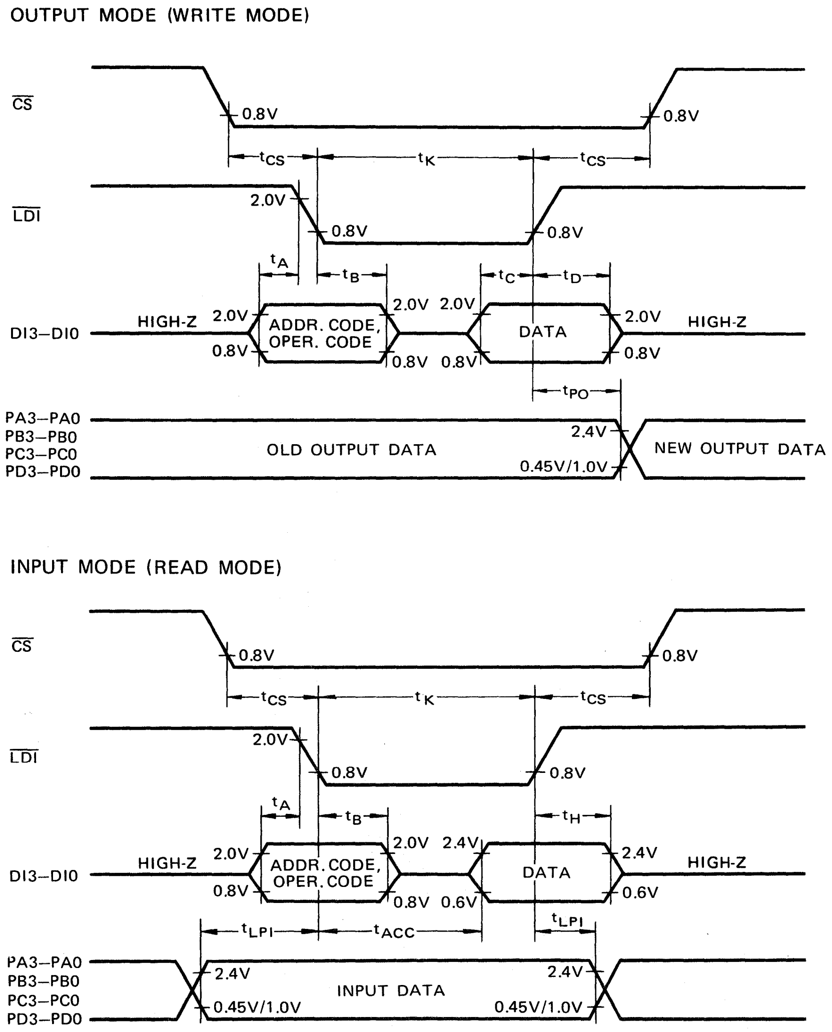
DC CHARACTERISTICS (T_A = -30°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Value			Unit	Conditions
			Min.	Typ.	Max.		
Input Low Voltage		V_{IL}	V_{SS}-0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC} + 0.3	V	
Output Low Voltage	Port A to D	V_{OL1}	–		0.45	V	I_{OL} = 5mA
		V_{OL2}	–		1.0	V	I_{OL} = 20mA
Output Low Voltage	DI0 to DI3	V_{OL3}	–		0.6	V	I_{OL} = 1.8mA
Output High Voltage	Ports A to D	V_{OH1}	2.4			V	I_{OH} = -50μA (MB 88305)
Output High Voltage	DI0 to DI3	V_{OH2}	2.4			V	I_{OH} = -100μA
Input Leakage Current	Ports A to D	I_{IL1}	-10		20	μA	$V_{SS} \leqq V_{IN} \leqq V_{CC}$
	DI0 to DI3, $\overline{CS}$, $\overline{LDI}$	I_{IL2}	-10		10	μA	$V_{SS} \leqq V_{IN} \leqq V_{CC}$
Input Current	Ports A to D	I_I		2.0		mA	V_{IN} = V_{SS} (MB 88305)
Total I_{OL} Output Current from 16 Output		ΣI_{OL}			80	mA	Each output current: 5mA
Supply Current	V_{CC}	I_{CC}		10	24	mA	

AC CHARACTERISTICS (T_A = −30°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Value			Unit	Condition
			Min.	Typ.	Max.		
Address/Op Codes Setup Time	DI3 to DI0	t_A	100			ns	C_L = 80pF
Address/Op Codes Hold Time	DI3 to DI0	t_B	60			ns	C_L = 20pF
Data Setup Time	DI3 to DI0 (Output Mode)	t_C	200			ns	C_L = 80pF
Data Hold Time	DI3 to DI0 (Output Mode)	t_D	20			ns	C_L = 20pF
Data Output Delay Time	Ports A to D (Output Mode)	t_{PO}			700	ns	C_L = 100pF
$\overline{LDI}$ Pulse Width	$\overline{LDI}$	t_K	700			ns	
$\overline{CS}$ Setup/Hold Time	$\overline{CS}$	t_{CS}	50			ns	
Input Data Setup/Hold Time	Ports A to D (Output Mode)	t_{LPI}	100			ns	
Data Output Delay Time	DI3 to DI0 (Input Mode)	t_{ACC}			650	ns	C_L = 80pF
Data Hold Time	DI3 to DI0 (Input Mode)	t_H	0		150	ns	C_L = 20pF

Fig. 5 — TIMING DIAGRAM



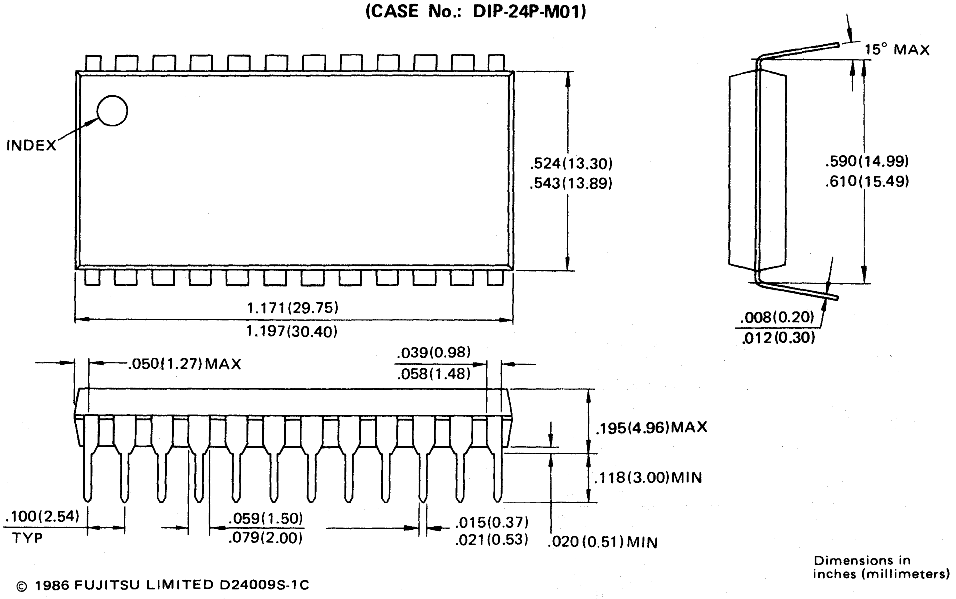
OUTPUT MODE (WRITE MODE)

INPUT MODE (READ MODE)

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M01)



FUJITSU

CMOS INPUT/OUTPUT EXPANDER

MB 88310 MB 88311

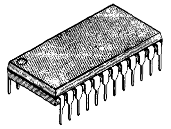
April 1986
Edition 1.0

CMOS INPUT/OUTPUT EXPANDER

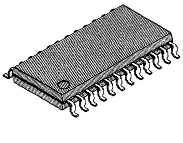
The Fujitsu MB 88310/MB 88311 are peripheral integrated circuits that can be connected to a 4-bit or 8-bit single-chip microcomputer (MCU) to provide additional I/O ports. Besides furnishing simple I/O port expansion, the MB 88310 and MB 88311 can AND or OR port data with data from the MCU, on instruction from the MCU.

The MB 88310/MB 88311 are pseudo-bidirectional ports. They are accessed in 4-bit units, but each individual bit can be used for either input or output, and input and output can be intermixed. The interface to the MCU requires only the connection of a 4-bit interface port and a strobe signal. All output ports of the MB 88310 are open-drain; MB 88311 output ports all have pull-up resistors. The output ports on both chips are reset to the high-impedance state at power-up.

The MB 88310/MB 88311 are fabricated with silicon-gate CMOS process, and package in a 24-pin plastic DIP or plastic fat package (SOP). Also, they are powered with a single +5V power supply, and operate over the ambient temperature range of –40°C to +85°C.



PLASTIC DIP
DIP-24P-M01

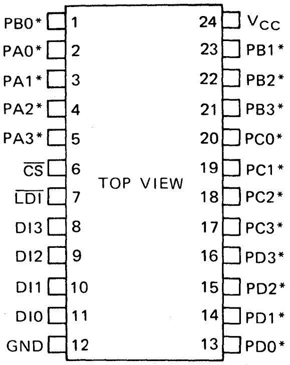


PLASTIC SOP
FPT-24P-M02

FEATURES

- CMOS Version of Fujitsu MB 88304/88305
- Four 4-bit I/O ports (16 lines)
- Four Functions: Parallel input, parallel output, AND output, and OR output
- AND and OR functions provide individual output capability
- Single-bit input/output: Input and output can be intermixed on each port
- High output drive
- Built-in power-on reset circuit
- $\overline{\text{CS}}$ pin for simplified input/output expansion
- Two output circuit types: Open-drain output (MB 88310)
  3-state output (MB 88311)
- Easily connectable to MCUs with 8243 interface
- Single +5V power supply
- -40°C to +85°C operating temperature range
- Silicon-gate CMOS process
- Two Package Options:
  – 24-pin plastic DIP (Suffix: -P)
  – 24-pin plastic SOP (Suffix: -PF)

PIN ASSIGNMENT



* { MB 88310: Open-drain output
MB 88311: 3-state output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

LOGIC SYMBOL

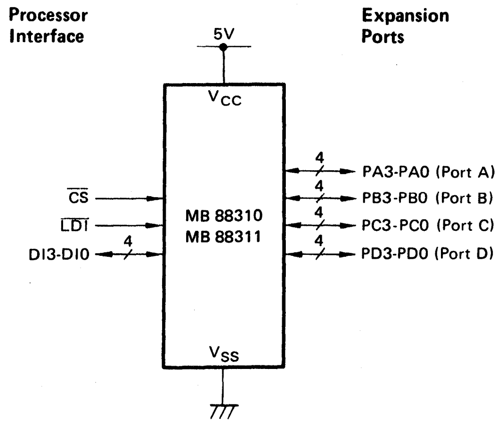
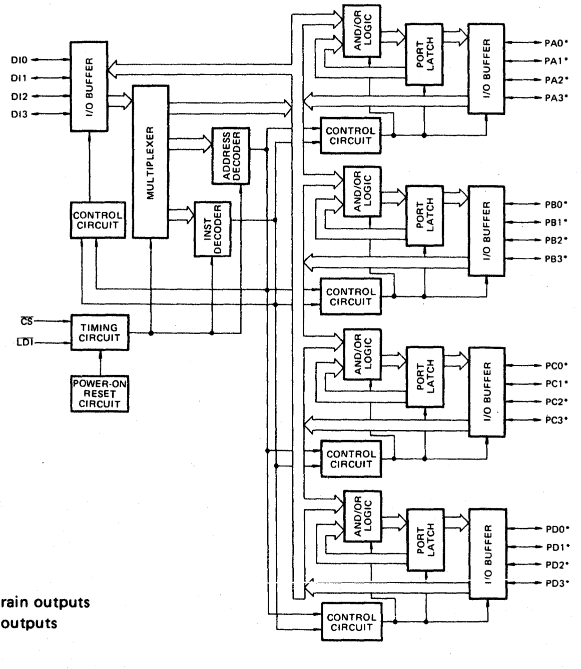


Fig. 1 – BLOCK DIAGRAM



*MB 88310: Open-drain outputs
MB 88311: 3-state outputs

PIN DESCRIPTION

The MB 88310/88311 have two interfaces: One is the processor interface; $\overline{\text{CS}}$, $\overline{\text{LDI}}$, and DI3–DI0, which are used for the processor to communicate with the MB 88310/88311 devices. Another is the expansion I/O ports; Ports A, B, C, and D, which serve as an expansion of the processor's I/O.

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Name/Function
V_{CC}	24	–	**V_{CC}**: is the +5V power supply pin.
GND	12	–	**GND**: is the ground pin.
$\overline{\text{CS}}$	6	I	**Chip Select**: is a low-level-sense high-impedance input. A low level on this input selects the device. This input is TTL-compatible.
$\overline{\text{LDI}}$	7	I	**Load Data Input**: is an edge-triggered strobe input. The operation code and address code on DI0 to DI3 are latched at the $\overline{\text{LDI}}$ falling edge. The data transffered via DI0 to DI3 becomes valid on the rising edge of the $\overline{\text{LDI}}$ input.
DI3 to DI0	8 to 11	I/O	**Data Bus**: is a 4-bit bidirectional port used for interface to the MCU. The operation code and address code provided by the MCU on this port are latched at the falling edge of the $\overline{\text{LDI}}$ strobe input, and input/output data is transferred at the rising edge of the $\overline{\text{LDI}}$. The DI port remains in the high-impedance state except when the input operation is executed.
PA0 to PA3	2 to 5	I/O	**Ports A, B, C, and D** are 4-bit bidirectional ports used as expansion I/O ports. These four ports are addressed by address codes provided by the MCU. When an input operation code is given by the MCU, data on the addressed port is transferred to the DI0 to DI3 at the rising edge of the $\overline{\text{LDI}}$. When an output operation code is provided, data on the DI0 to DI3 is transferred and latched to the addressed port at the rising edge of the $\overline{\text{LDI}}$. Logical operations are also possible, in which data on the addressed port is ANDed or ORed with data on the DI0 to DI3 and the result is latched at the addressed port at the rising edge of the $\overline{\text{LDI}}$. After a power-on reset, Ports A to D are all set to the high-impedance state. An individual port is released from the high-impedance state when the OUT, AND, or OR function is applied to it. (Since the MB 88310 has open-drain outputs, a line returns to the high-impedance state when an "1" is written on it.)
PB0, PB1 to PB3	1, 21 to 23	I/O	
PC0 to PC3	20 to 17	I/O	
PD0 to PD3	16 to 13	I/O	

FUNCTIONAL DESCRIPTION

The four 4-bit I/O ports of the MB 88310 and MB 88311 are labelled port A, port B, port C, and port D (PA, PB, PC, and PD). They serve as expansion I/O ports for a one-chip microcomputer (MCU), and can be accessed via an MCU port. Their functions are as follows:

- Data transfer from the MCU to port A, B, C, or D
- Data transfer from port A, B, C, or D to the MCU
- ANDing of the port A, B, C, or D data with MCU data and latching of the result at port A, B, C, or D
- ORing of the port A, B, C, or D data with MCU data and latching of the result at port A, B, C, or D

For interface to the MCU, the MB 88310 and MB 88311 have a 4-bit interface port (DI0 to DI3), a strobe input ($\overline{\text{LDI}}$ pin), and a chip select input ($\overline{\text{CS}}$ pin). The interface data consists of two 4-bit units. The first 4 bits give the operation code (2-bits) and address code (2 bits). The second 4-bits are the input or output data. Both 4-bit units are transferred through the interface port (DI0 to DI3) on timings determined by the strobe ($\overline{\text{LDI}}$) signal. The MB 88310 or MB 88311 reads the operation code and address code from the MCU on the falling edge of the $\overline{\text{LDI}}$ signal, and sends or receives the I/O data on the rising edge of $\overline{\text{LDI}}$.

The $\overline{\text{CS}}$ pin is used to read a chip select signal from the MCU's I/O port when two or more MB 88310 or MB 88311 chips are connected to the MCU.

Ope. Code		Function Funct	Addr. Code		Port Address
DI3	DI2		DI1	DI0	
0	0	IN (Input)	0	0	Port A (PA)
0	1	OUT (Output)	0	1	Port B (PB)
1	0	OR (Logical OR)	1	0	Port C (PC)
1	1	AND (Logical AND)	1	1	Port D (PD)

POWER-ON RESET

The MB 88310 and MB 88311 contain an internal power-on reset circuit that detects the rise of V_{CC} on the power supply line and holds the chip circuits in the reset state. In the reset state, the interface port (pins DI0 to DI3) is set to the input state, and ports A to D (PA to PD) are in the high-impedance state (except that latched output ports are not reset). The V_{CC} line must rise smoothly for the reset circuit to operate. Regardless of the input level (high of low) of the $\overline{\text{LDI}}$ pin at the moment power is applied, the reset state is released at the first falling edge of the $\overline{\text{LDI}}$ input. A power-on reset also occurs if the supply voltage (V_{CC}) drops to 1 V or less, then recovers to the rated voltage.

OUTPUT MODE (Write Mode)

Corresponding to three functions of the MCU, the MB 88310 and MB 88311 have three output modes: data transfer output (OUT), logical OR (OR), and logical AND (AND).

- OUT

The designated port latches and outputs the 4-bit data transferred from the MCU.

- AND

The 4-bit data transferred from the MCU is ANDed with the 4-bit data of the designated port, which then latches the result as output.

- OR

The 4-bit data transferred from the MCU is ORed with the 4-bit data of the designated port, which then latches the result as output.

The operation code and address code sent from the MCU to pins DI0 to DI3 of the MB 88310 or MB 88311 are latched on the falling edge of the strobe signal at the $\overline{\text{LDI}}$ pin. The MCU data is read on the rising edge of the strobe signal and sent to the logic circuit of the designated port, where it is processed. The MCU data is then latched as output data.

INPUT MODE (Read Mode)

The MB 88310 and MB 88311 have only one input mode (IN), corresponding to data input by the MCU.

- IN

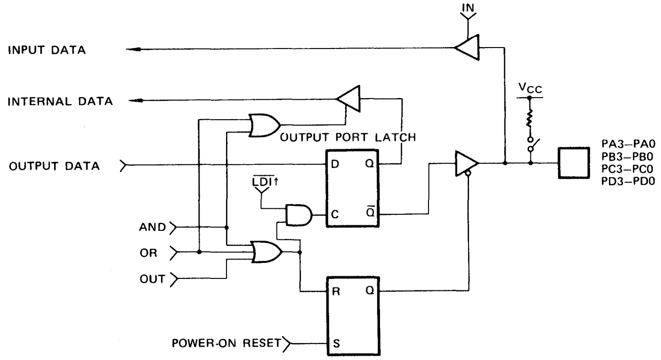
The input data at the port designated by the MCU is read and sent to the MCU via the interface port (DI0 to DI3).

The operation and address code sent from the MCU to pins DI0 to DI3 of the MB 88310 or MB 88311 are latched on the falling edge of the strobe signal at the $\overline{\text{LDI}}$ pin. If the operation code specifies input, the MB 88310 or MB 88311 sends data from the port designated by the address code to the MCU via DI0 to DI3.

A power-on reset places the chip in the input mode with ports A to D in the high-impedance state. If only the IN function is used thereafter, the ports remain in the high-impedance state. Release from the high-impedance state takes place when the OUT, AND, or OR function is used.

The MB 88310 and MB 88311 are designed for easy external driving. The MB 88310 has open-drain outputs, while the MB 88311 outputs have pull-up resistors. For both chips, the input level of a port to be used for input can be read by writing a 1 and performing the IN function. Input and output can therefore be intermixed within the four bits of each of the four ports (A to D).

Fig. 2 – PORT CIRCUIT CONFIGURATION



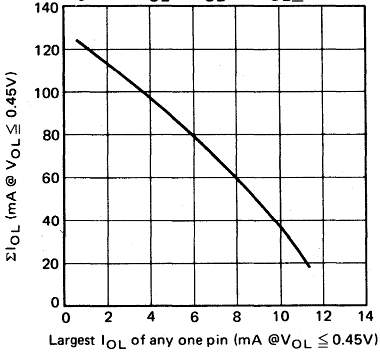
SINK CURRENT FROM PORTS A TO D

When $V_{OL} \leqq 0.45V$, the MB 88310 and MB 88311 can sink 5mA (I_{OL}) on each of their 16 I/O lines simultaneously. When this current sinking capability is not required on all of the I/O lines, or not all of the lines have to sink 5mA, the driving capability (sink current) of the other I/O lines can be increased according to the characteristics shown in the curve below.

For instance, if one of the I/O lines has to sink 9mA, the total I_{OL} (ΣI_{OL}) of all the lines can be up to 45mA.

Example-1: How many I/O lines with 5 TTL leads can be driven?
$I_{OL} = 5 \times 1.6mA = 8mA$
$\Sigma I_{OL} \leqq 60mA$ (from the total I_{OL} characteristics curve)
60mA/8mA = 7 I/O lines
The chip can drive 7 lines with 5 TTL loads, making a total of 56mA on these lines. The remaining 4mA can be shared among the other 9 I/O lines.

Fig. 3 – ΣI_{OL} vs I_{OL} (@ $V_{OL} \leqq 0.45V$)

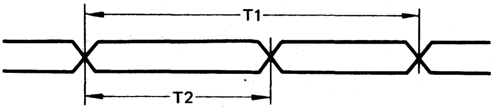


Example-2: Suppose that two of the load lines have I_{OL} = 20mA (at $V_{OL} \leqq 1V$). Can the MB 88310 or MB 88311 drive the following loads?
2 I/O lines: 20mA (at $V_{OL} \leqq 1V$)
8 I/O lines: 4mA (at $V_{OL} \leqq 0.45V$)
6 I/O lines: 3.2mA (at $V_{OL} \leqq 0.45V$)
Total I_{OL} $(2 \times 20mA) + (8 \times 4mA) + (6 \times 3.2mA)$
$= 91.2mA$
Reading the total I_{OL} characteristic for I_{OL} = 4mA, we see that $\Sigma I_{OL} \leqq 93mA$. Since 91.2mA $\leqq$ 93mA, the chip can drive these loads.
Note: The allowable total I_{OL} (ΣI_{OL}) depends on the maximum sink current of the lines for which V_{OL} must be equal to or less than 0.4V.

NOTICE ON USING INPUT MODE

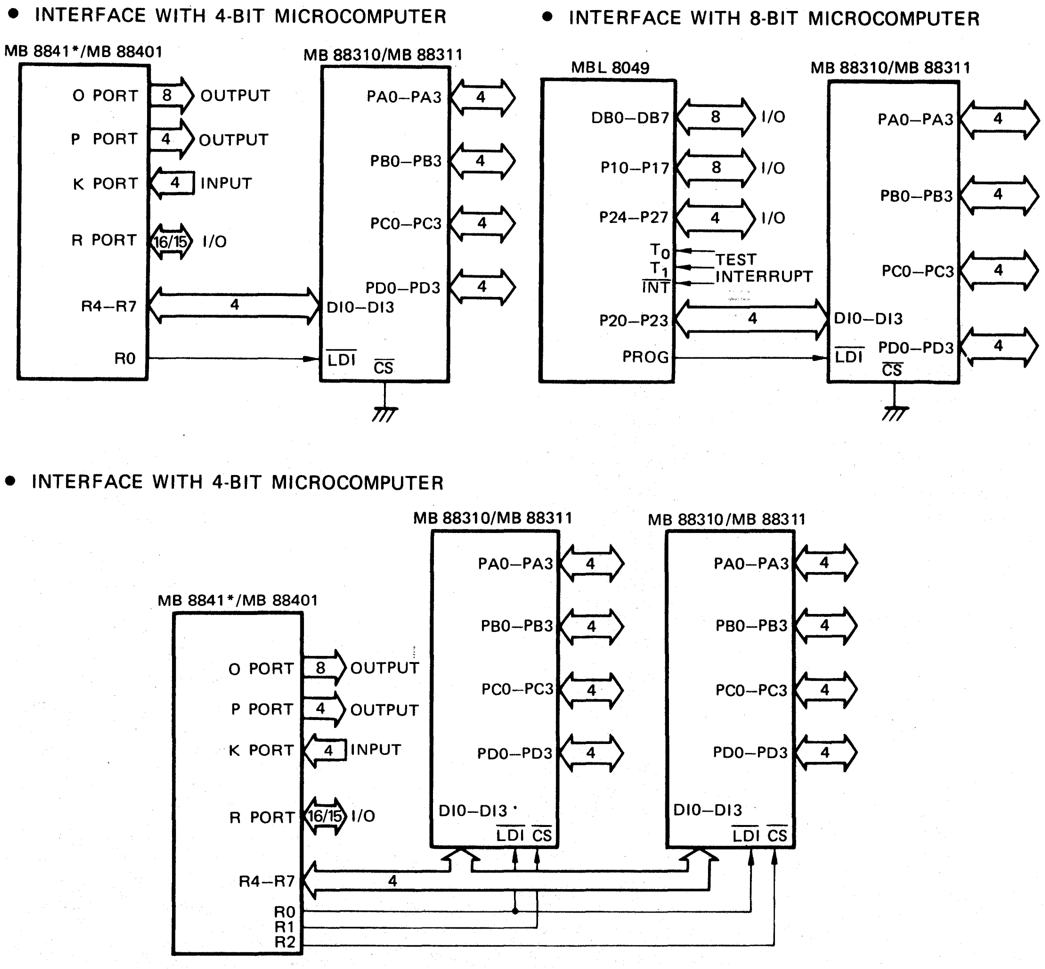
When the MB 88310/88311 devices work in input mode with a processor which has no 8243 interface, data collision may occur between the device's DI3–DI0 port and processor's data bus. In such case, the following limits should be noticed.

1. DC collision: Maximum short circuit current for DI3 – DI0 = 2.5mA.
2. AC collision: Maximum short circuit current for DI3 – DI0 = 30mA at T2/T1 (= duty) < 0.1 and T2 < 1ms. (See figure below.)



Note: T1 = Period, T2 = Collision Time

Fig. 4 – TYPICAL APPLICATIONS



- INTERFACE WITH 4-BIT MICROCOMPUTER
- INTERFACE WITH 8-BIT MICROCOMPUTER
- INTERFACE WITH 4-BIT MICROCOMPUTER

NOTE: * Output port of MB 8841 should be open-drain type.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	V_{SS}-0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3 to +7.0*	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

*V_{IN} should not exceed V_{CC} + 0.3V.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+5 ± 10%	V
	V_{SS}	0	
Operating Temperature	T_A	-40 to +85	°C

ELECTRICAL CHARACTERISTICS

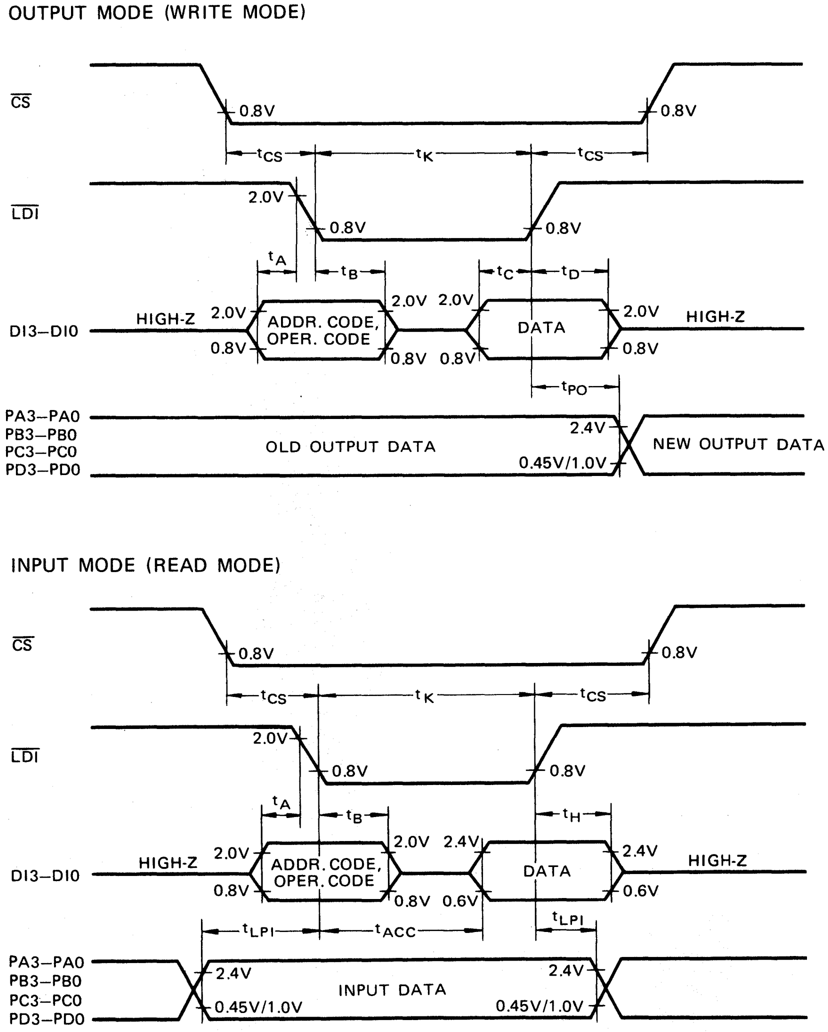
DC CHARACTERISTICS (T_A = –40°C to +85°C, V_{CC} = +5V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Value			Unit	Conditions
			Min.	Typ.	Max.		
Input Low Voltage		V_{IL}	V_{SS}-0.3		0.8	V	
Input High Voltage		V_{IH}	2.2		V_{CC}+0.3	V	
Output Low Voltage	Port A to D	V_{OL1}	–		0.45	V	I_{OL} = 5mA
		V_{OL2}	–		1.0	V	I_{OL} = 20mA
Output Low Voltage	DI0 to DI3	V_{OL3}	–		0.6	V	I_{OL} = 1.8mA
Output High Voltage	Ports A to D	V_{OH1}	2.4			V	I_{OH} = –240μA (MB 88311)
Output High Voltage	DI0 to DI3	V_{OH2}	2.4			V	I_{OH} = –100μA
Input Leakage Current	Ports A to D	I_{IL1}	-10		20	μA	$V_{SS} \leqq V_{IN} \leqq V_{CC}$
	DI0 to DI3, CS, $\overline{LDI}$	I_{IL2}	-10		10	μA	$V_{SS} \leqq V_{IN} \leqq V_{CC}$
Input Current	Ports A to D	I_I		1.0		mA	V_{IN} = V_{SS} (MB 88311)
Total I_{OL} Output Current from 16 Output		ΣI_{OL}			80	mA	Each output current: 5mA
Supply Current	V_{CC}	I_{CC1}		200	600	μA	All outputs open, Normal operation
		I_{CC2}		1.0	10	μA	All outputs open, Standby operation, $\overline{LDI}$ cycle = 5μs

AC CHARACTERISTICS (T_A = –40°C to +85°C, V_{CC} = +5V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Value			Unit	Conditions
			Min.	Typ.	Max.		
Address/Op Codes Setup Time	DI3 to DI0	t_A	100			ns	C_L = 80pF
Address/Op Codes Hold Time	DI3 to DI0	t_B	60			ns	C_L = 20pF
Data Setup Time	DI3 to DI0 (Output Mode)	t_C	200			ns	C_L = 80pF
Data Hold Time	DI3 to DI0 (Output Mode)	t_D	20			ns	C_L = 20pF
Data Output Delay Time	Ports A to D (Output Mode)	t_{PO}			700	ns	C_L = 100pF
$\overline{\text{LDI}}$ Pulse Width	$\overline{\text{LDI}}$	t_K	700			ns	
$\overline{\text{CS}}$ Setup/Hold Time	$\overline{\text{CS}}$	t_{CS}	50			ns	
Input Data Setup/Hold Time	Ports A to D (Output Mode)	t_{LPI}	100			ns	
Data Output Delay Time	DI3 to DI0 (Input Mode)	t_{ACC}			650	ns	C_L = 80pF
Data Hold Time	DI3 to DI0 (Input Mode)	t_H	0		150	ns	C_L = 20pF

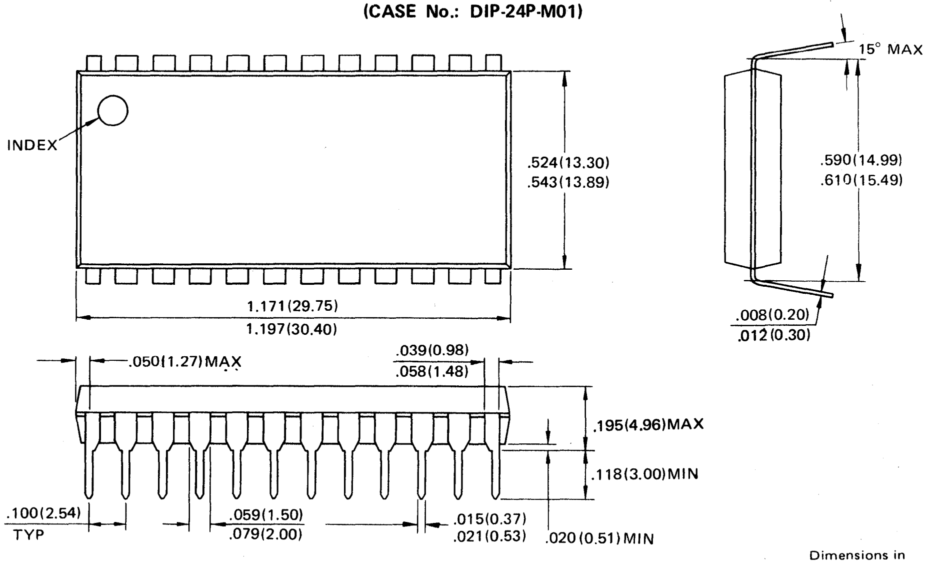
Fig. 5 – TIMING DIAGRAM



PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M01)

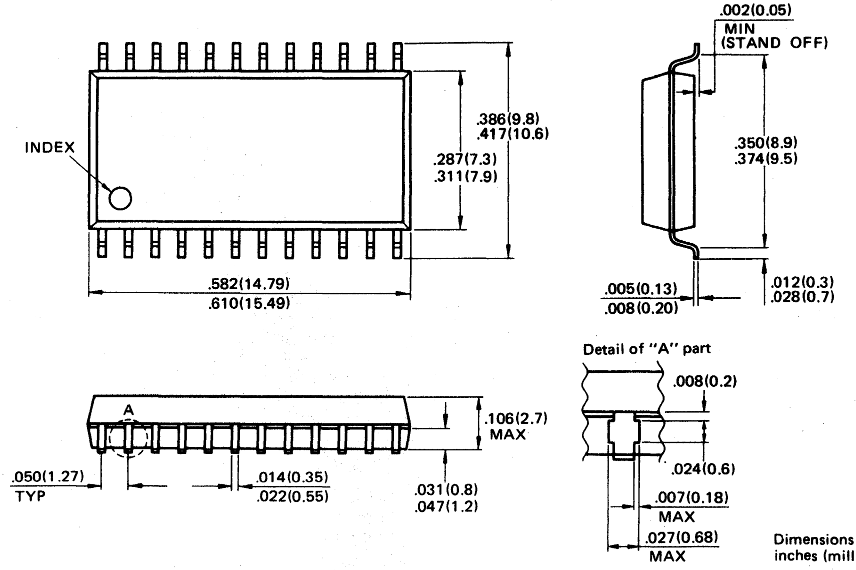


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC SOP (Suffix: -PF)

24-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-24P-M02)



Dimensions in inches (millimeters)

[redacted]

FUJITSU

MB88306 MB88307 MB88308 MB88309

October 1986

CMOS Output Expander

DESCRIPTION

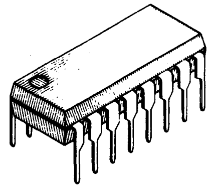
Each of the four expanders provides a serial I/O port and an 8-bit parallel output port. Data is serially loaded via the input port, converted to an 8-bit parallel format, and latched. The latched data is then transferred to the parallel output port for distribution. The 8-bit output port can directly drive a Light Emitting Diode (LED) display; the LED display can be expanded in byte-size increments to make any desired configuration. In terms of output drive and shift clock triggers, each expander is unique—see description that follows.

Expander	Output	Shift Clock Trigger
MB88306	CMOS 3-State	Rising Edge
MB88307	NMOS Open Drain	Rising Edge
MB88308	CMOS 3-State	Falling Edge
MB88309	NMOS Open Drain	Falling Edge

MB88306/7/8/9 are fabricated by a silicon-gate CMOS process and are packaged in a standard 16-pin plastic DIP or SOP. All four expanders operate with a single +5V power source and a 2 MHz shift clock over an ambient temperature range of −40°C to +85°C.

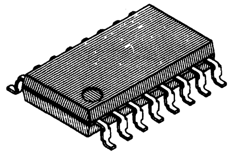
FEATURES

- 8-bit parallel output
- Serial input/output
- Expandable in 8-bit increments
- LED direct drive capability: 15 mA max at 1.2V
- Two output port types:
  —CMOS 3-state output (MB88306/8)
  —NMOS open-drain output (MB88307/9)
- Two shift clock polarities:
  —Rising-edge-triggering (MB88306/7)
  —Falling-edge-triggering (MB88308/9)
- Simple interface to Fujitsu 4-bit microcomputers
- TTL compatible outputs
- Single +5V power supply
- Silicon-gate CMOS process
- Two package options:
  —16-pin plastic DIP (Suffix -P)
  —16-pin plastic SOP (Suffix -PF)



8306–1

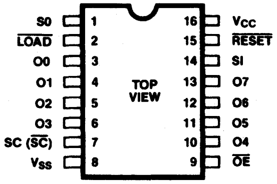
Plastic DIP (Suffix -P)
DIP-16P-M02



8306–2

Plastic SOP (Suffix -PF)
FPT-16P-M02

Pin Assignments



8306–3

Note:
SC is applicable to MB88306 and MB88307
$\overline{SC}$ is applicable to MB88308 and MB88309

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

B38306

Figure 1. Block Diagram

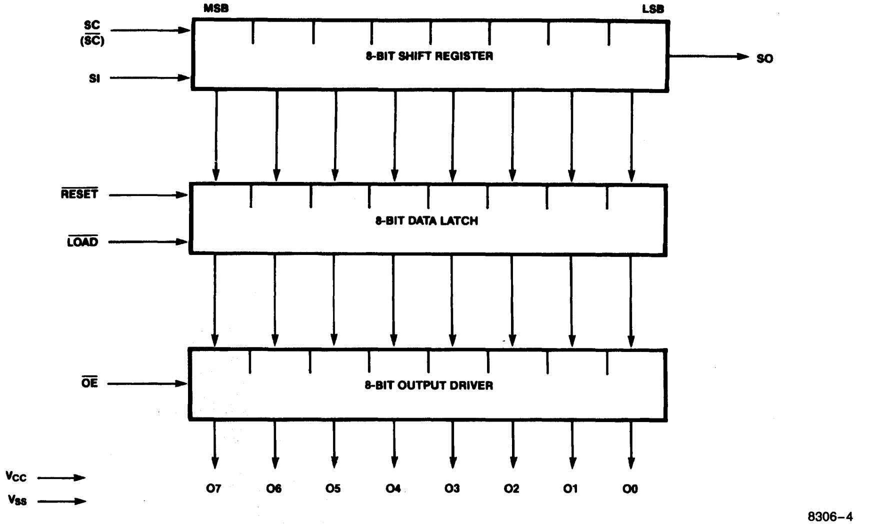
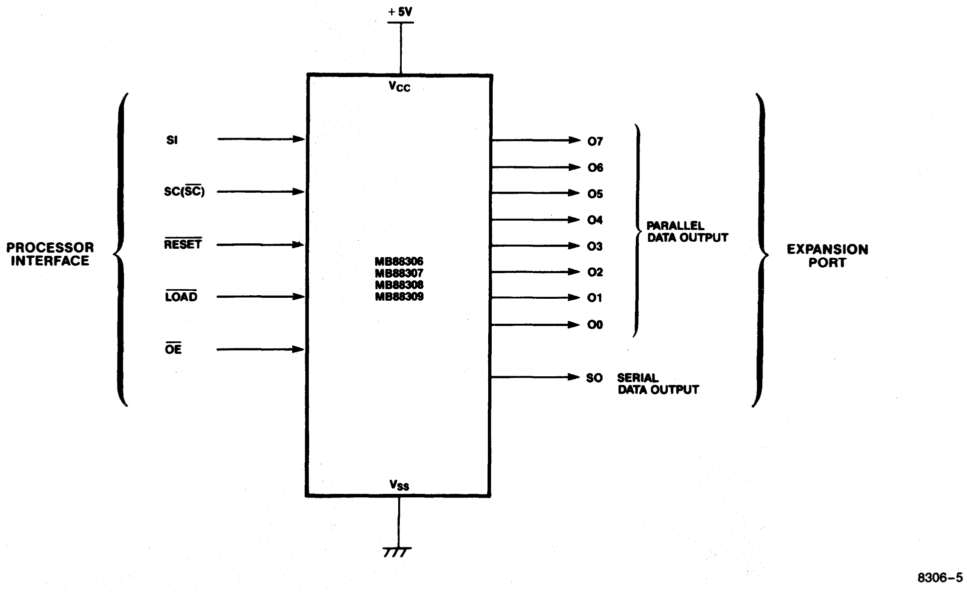


Figure 2. System Interface



Note:
SC for MB88306/7; $\overline{SC}$ for MB88308/9

PIN DESCRIPTION

Figures 1 and 2 show the pin assignment and logic symbol of the MB88306/7/8/9. Table 1 shows the pin description. The MB88306/7/8/9 have two interfaces: one is the processor interface; SI, SC ($\overline{\text{SC}}$), $\overline{\text{RESET}}$, $\overline{\text{LOAD}}$, and $\overline{\text{OE}}$ inputs; the other is the expansion output port; O7-O0, and SO outputs.

Table 1: Pin Description

Symbol	Number	Type	Name & Function
• Power Supply			
V_{CC}	16	—	+ 5V dc power supply pin.
V_{SS}	8	—	Power supply ground pin.
• Processor Interface			
SI	14	I	Serial data input to the internal shift register: A data bit on the SI pin is shifted into the MSB of the shift register at the rising edge (MB88306/7) of the shift clock SC or the falling edge (MB88308/9) of the shift clock for $\overline{\text{SC}}$. The data bits are transferred from the processor or from the SO pin of the cascaded devices.
SC ($\overline{\text{SC}}$)	4	I	Shift clock input for the internal shift register: The rising edge of SC (MB88306/7) or falling edge of $\overline{\text{SC}}$ (MB88308/9) shifts a data bit on the SI pin into the MSB of the shift register, each bit of the shift register is shifted right, and the LSB of the shift register appears directly on the SO pin. A high level and low level and the falling edge (MB88306/7) or the rising edge (MB88308/9) keep contents of the shift register. *This is a hysteresis input.*
$\overline{\text{RESET}}$	15	I	Preset input for the internal data latch: A low level on the $\overline{\text{RESET}}$ pin initializes the data latch in high state, and also inhibits the $\overline{\text{LOAD}}$ input. *This is a hysteresis input.* The $\overline{\text{RESET}}$ input does not affect the shift register and the output drain.
$\overline{\text{LOAD}}$	2	I	Load enable input for the internal data latch: A low level on the $\overline{\text{LOAD}}$ pin transfers 8-bit parallel data of the shift register into the data latch. A high level inhibits data transmission from the shift register to the data latch, to hold contents of the data latch. This input is automatically inhibited when the $\overline{\text{RESET}}$ input is activated (low). *This is a hysteresis input.*
$\overline{\text{OE}}$	9	I	Output enable input of the output driver: A low level on the $\overline{\text{OE}}$ pin outputs 8-bit data of the data latch on the data output pins O7–O0. A high level places the O7–O0 pins in high impedance state. The $\overline{\text{OE}}$ pin does not control the SO output.
• Expansion Port			
O7–O0	13–10, 6–3	O	Parallel data output: This is an 8-bit 3-state data output port. This port outputs 8-bit data in the data latch when the $\overline{\text{OE}}$ pin is activated (low), and is placed in high impedance state when the $\overline{\text{OE}}$ pin is inactive (high). This port is CMOS 3-state output (MB88306/8) or NMOS open-drain output (MB88307/9). Both output drivers can directly drive LEDs. The MSB and LSB of the shift register are output onto the O7 and O0 pins, respectively. These pins are TTL compatible.
SO	1	O	Serial data output of the internal shift register: The LSB of the shift register appears directly onto the SO pin with some delay time because the SO output has no output latch. This pin is used to cascade devices to expand the data output port in 8-bit units. This pin is TTL compatible but is not 3-state output controlled by the $\overline{\text{OE}}$ pin.

FUNCTIONAL DESCRIPTION

BLOCK FUNCTIONS

The MB88306/7/8/9 consist of a shift register, a data latch, and an output driver. Figure 1.

Shift Register

This is an 8-bit serial-in/parallel-out static shift register, that converts serial data loaded by the processor into 8-bit parallel data. The rising edge (MB88306/7) or falling edge (MB88308/9) of the shift clock (SC or $\overline{\text{SC}}$) shifts a data bit on the SI pin into the MSB of the shift register. Each bit of the shift register is shifted right (MSB → LSB), and the LSB of the shift register is shifted out onto the SO pin. Eight parallel output lines of the shift register are internally connected to the data latch inputs. The Shift register has no clear input and, after power-up, the register contents are undefined. The $\overline{\text{RESET}}$ input does not affect the shift register.

Data Latch

This is an 8-bit D-type transparent latch that holds 8-bit parallel data transferred from the shift register. The latch has two control inputs, $\overline{\text{LOAD}}$ and $\overline{\text{RESET}}$: The $\overline{\text{LOAD}}$ pin is a data enable input and a low level on this pin transfers contents of the shift register into the data latch. The $\overline{\text{RESET}}$ pin is a preset input and a low level on this pin initializes the data latch in the high state. When the $\overline{\text{RESET}}$ input is active, the $\overline{\text{LOAD}}$ input is automatically inhibited.

Output Driver

This is an 8-bit 3-state output driver that is driven by 8 bits of data from the data latch. The MB88306/8 have a CMOS 3-state output driver and the MB88307/9 have an NMOS open-drain output driver. Both drivers are controlled by the $\overline{\text{OE}}$ input and can directly drive LEDs (V_{OL} = 1.2V max at I_{OL} = 20 mA). A low level on the $\overline{\text{OE}}$ pin enables 8-bit data in the data latch onto output pins O7–O0. A high level forces the output pins to a high impedance state. The $\overline{\text{RESET}}$ input does not affect the output driver.

SYSTEM INTERFACE

The processor and expansion-port interface for the four expanders is shown in Figure 2. As previously indicated, internal operations of the MB88306 and MB88307 are initiated on the rising edge of Shift Clock (SC) whereas, the same operations in the MB88308 and MB88309 occur on the falling edge of $\overline{\text{SC}}$. The Serial Output (SO) pin can be used to cascade two or more expanders; an example is shown later in this data sheet.

Table 2. Expander Functions

	Control Inputs				Internal State		Data Outputs
Mode	SC ($\overline{\text{SC}}$)	$\overline{\text{LOAD}}$	$\overline{\text{RESET}}$	$\overline{\text{OE}}$	Shift Register	Data Latch	O7–O0
Shift	↑ (↓)	H	X	X	X	X	X
Hold	H/L, ↓ (↑)	X	X	H	X	X	Z
				L			X
Load	X (X)	L	H	H	X	X	Z
				L	H/L	H/L	H/L
Reset	X (X)	X	L	H	X	H	Z
				L			X

Legend:

H = High level	Z = High impedance	↑ = Rising edge
L = Low level	X = Don't care	↓ = Falling edge

FUNCTIONAL DESCRIPTION (Continued)

OPERATING MODES

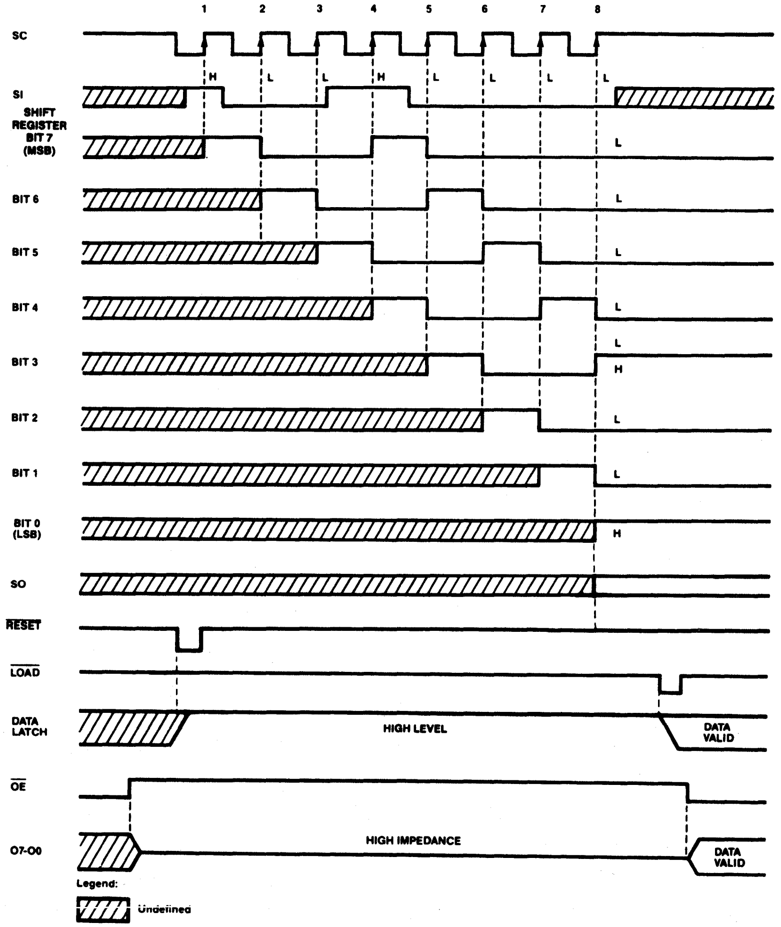
Initialization (Reset Mode)

After power on, contents of the shift register and data latch are undefined. The shift register can not be initialized by hardware because it has no preset input. The data latch can be preset to a high state by a low level on the $\overline{\text{RESET}}$ pin.

Data Input (Shift & Hold Modes)

Data serially loaded by the processor through the SI pin synchronously with the shift clock, SC (MB88306/7) or $\overline{\text{SC}}$ (MB88308/9). At the rising edge of SC or the falling edge of $\overline{\text{SC}}$, serial data on the SI pin is shifted into the MSB of the shift register. Each bit of the shift register is shifted right, and the LSB of the shift register underflows onto the SO pin. During high and low levels of SC ($\overline{\text{SC}}$), contents of the shift register are held.

Figure 3. Input/Output Timing Based on the Rising Edge of SC (I/O timing for $\overline{\text{SC}}$ is identical, except for pulse-width offset.)



8306-6

FUNCTIONAL DESCRIPTION (Continued)

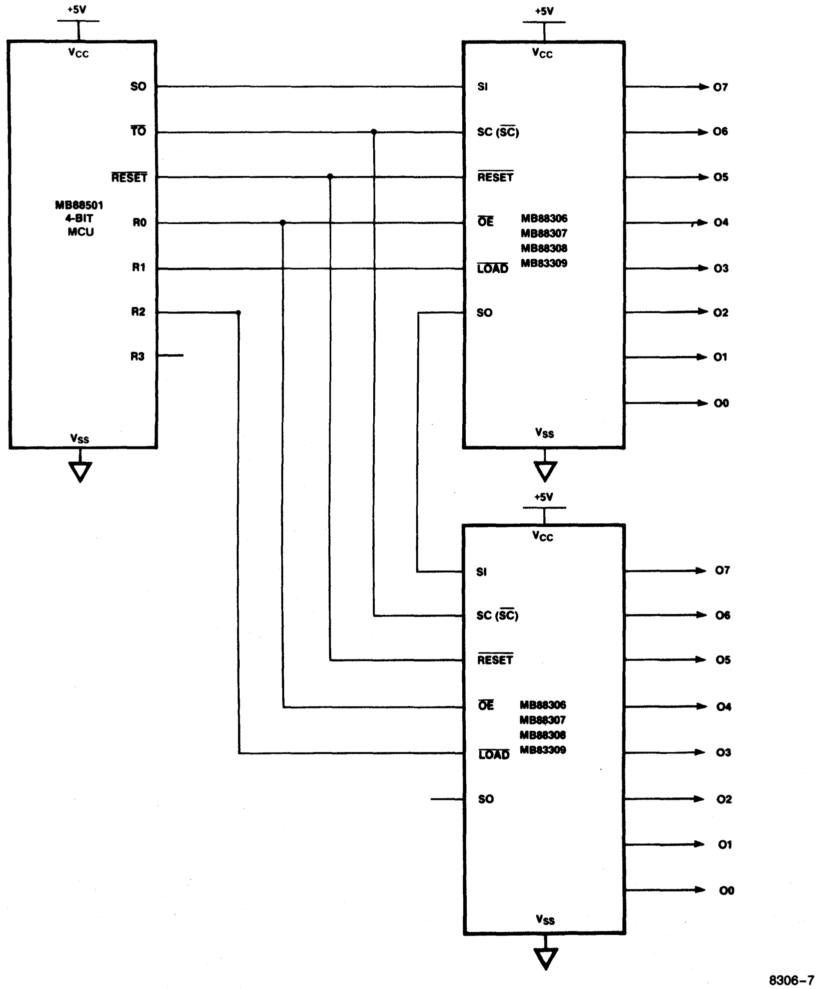
Data Output (Load Mode)

A low level on the $\overline{\text{LOAD}}$ pin transfers 8 bits of data from the shift register in parallel into the data latch. A low level on the $\overline{\text{OE}}$ pin enables the 8-bit data in the data latch onto the output port pins O7–O0. When the $\overline{\text{LOAD}}$ pin is high, the shift register and the data latch are isolated to hold contents of the data latch. (When the $\overline{\text{RESET}}$ pin is activated, the load input is automatically inhibited.) Also, when the $\overline{\text{OE}}$ pin is inactive, the O7–O0 pins are forced to a high impedance state. (The data output pins of the MB88307/9 float when 1s are output because they have NMOS open-drain drivers.)

APPLICATION

Figure 4 shows an example of an expanded output port configuration.

Figure 4. Expanded Output Port Configuration



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply Voltage	V_{CC}	$V_{SS}-0.3$	$V_{SS}+7.0$	V	
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Voltage	V_{OUT}	$V_{SS}-0.3$	$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Low Current	I_{OL}		20	mA	
Total Output Low Current	ΣI_{OL}		60	mA	
Power Dissipation	P_D		200	mW	
Operating Ambient Temperature	T_A	−40	+85	°C	
Storage Temperature	T_{STG}	−55	+150	°C	

Note:

Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply Voltage	V_{CC}	4.5	5.5	V	Guaranteed range
	V_{SS}	0	0	V	
Input High Voltage	V_{IH}	$0.7V_{CC}$	$V_{CC}+0.3$	V	Non-hysteresis inputs: SI, $\overline{\text{OE}}$
	V_{IHS}	$0.8V_{CC}$	$V_{CC}+0.3$	V	Hysteresis inputs: $\overline{\text{RESET}}$, $\overline{\text{LOAD}}$, SC ($\overline{\text{SC}}$)
Input Low Voltage	V_{IL}	$V_{SS}-0.3$	$0.3V_{CC}$	V	Non-hysteresis inputs: SI, $\overline{\text{OE}}$
	V_{ILS}	$V_{SS}-0.3$	$0.2V_{CC}$	V	Hysteresis inputs: $\overline{\text{RESET}}$, $\overline{\text{LOAD}}$, SC ($\overline{\text{SC}}$)
Operating Ambient Temperature	T_A	−40	+85	°C	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Output High Voltage	V_{OH}	O7–O0[1], SO	V_{CC} = 4.5V, I_{OH} = −200 μA	2.4			V
			V_{CC} = 4.5V, I_{OH} = −10 μA	4.0			V
Output Low Voltage	V_{OL}	O7–O0, SO	V_{CC} = 4.5V, I_{OL} = 1.8 mA			0.4	V
			V_{CC} = 4.5V, I_{OL} = 5.0 mA			0.6	V
			V_{CC} = 4.5V, I_{OL} = 15 mA			1.2	V
Input Leakage Current	I_{IL}	SI, SC, ($\overline{SC}$) $\overline{RESET}$, $\overline{LOAD}$, $\overline{OE}$	V_{CC} = 5.5V, V_{IN} = 0.4V			−10	μA
High-Impedance Output Leakage Current	I_{OZ}	O7–O0[1]	V_{CC} = 5.5V, V_{IN} = 0V to 5.5V, Off State			±10	μA
Open-Drain Output Leakage Current	I_{leak}	O7–O0[2], SO	V_{CC} = 5.5V, V_{IN} = 5.5V, Off State			10	μA
Supply Current	I_{CC}	V_{CC}	V_{CC} = 5.0V (Typ), 5.5V (Max), f_C = 2 MHz, All Outputs Open and All Inputs Pulled Up/Down to V_{CC}/V_{SS}		100	200	μA

Notes:

1. This parameter is specified for MB88307/MB88309 (CMOS 3-state output).
2. This parameter is specified for MB88306/MB88308 (NMOS open-drain output).

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

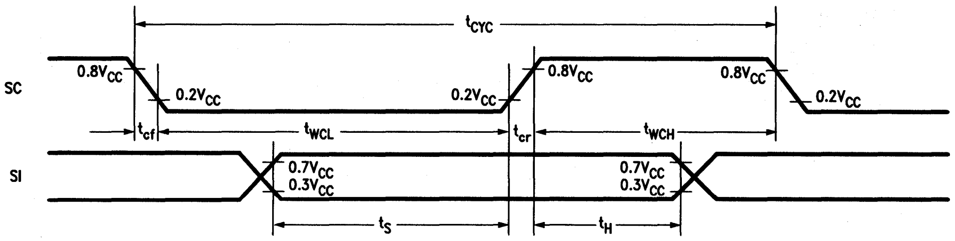
Input Timing Requirements

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Shift Clock Frequency	f_C	SC ($\overline{SC}$)				2	MHz
Shift Clock Cycle Time	t_{CYC}	SC ($\overline{SC}$)	Fig. 5 (Fig. 6)	0.5			μs
Shift Clock Pulse Width	t_{WCH} t_{WCL}	SC ($\overline{SC}$)	Fig. 5 (Fig. 6)	200			ns
Shift Clock Rise/Fall Times	t_{cr} t_{cf}	SC ($\overline{SC}$)	Fig. 5 (Fig. 6)	10		100	ns
Input Data Setup Time	t_S	SI	Fig. 5 (Fig. 6)	100			ns
Input Data Hold Time	t_H	SI	Fig. 5 (Fig. 6)	50			ns
Reset Pulse Width	t_{W1}	$\overline{RESET}$	Fig. 7	100			ns
Load Pulse Width	t_{W2}	$\overline{LOAD}$	Fig. 7	200			ns

AC CHARACTERISTICS

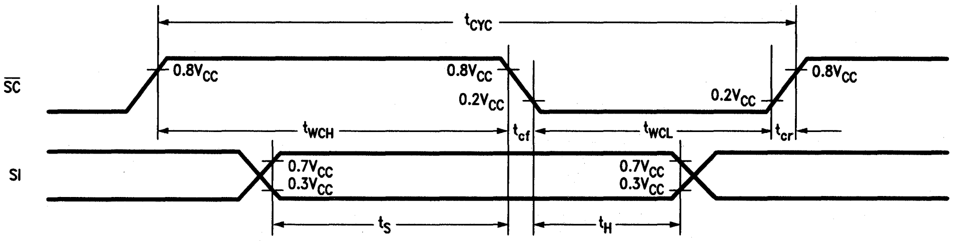
(Recommended operating conditions unless otherwise noted) (Continued)

Figure 5. Input Timing for MB88306 and MB88307



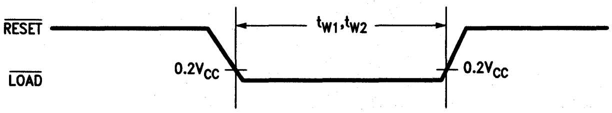
8306-8

Figure 6. Input Timing for MB88308 and MB88309



8306-9

Figure 7. Input Timing for All Expanders



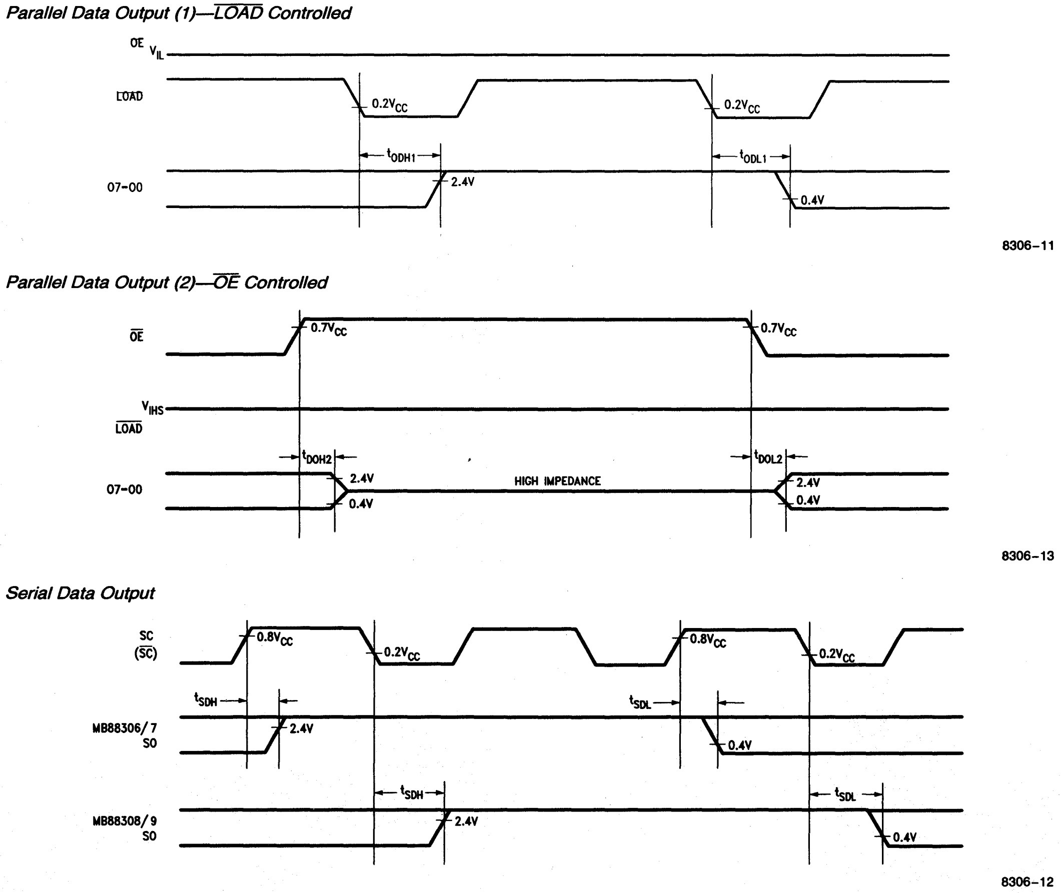
8306-10

AC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted) (Continued)

Output Timing Responses

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Parallel Data Output Delay Time	t_{ODH1}	O7–O0	Output Load: 50 pF + 1.2 kΩ See Fig. 8			500	ns
	t_{ODL1}					200	ns
	t_{DOH2}					500	ns
	t_{DOL2}					200	ns
Serial Data Output Delay Time	t_{SDH}	SO				500	ns
	t_{SDL}					200	ns

Figure 8. Output Timing for All Expanders



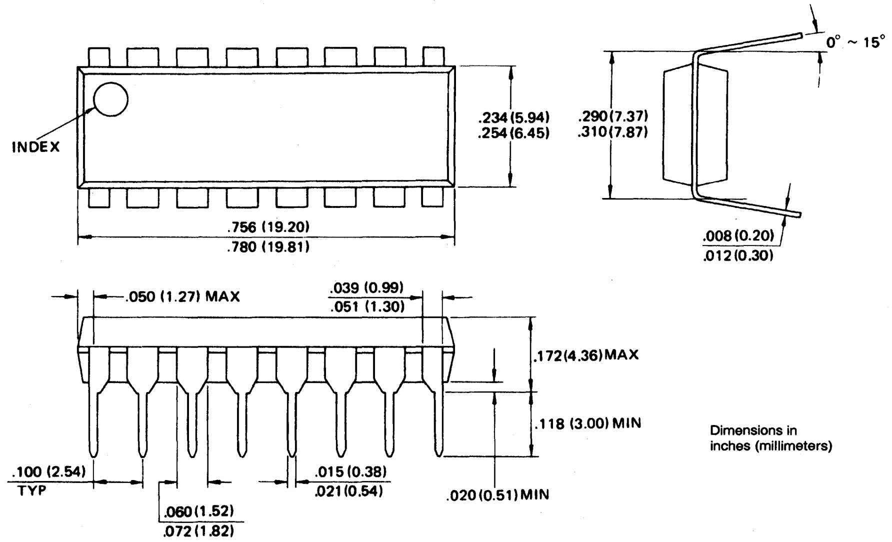
Parallel Data Output (1)—LOAD Controlled

Parallel Data Output (2)—OE Controlled

Serial Data Output

PACKAGE DIMENSIONS

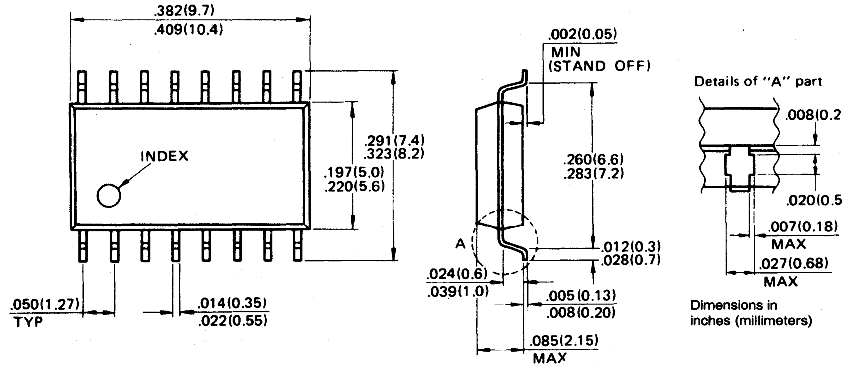
16-LEAD PLASTIC DUAL IN-LINE PACKAGE (DIP-16P-M02)



Dimensions in inches (millimeters)

8306–14

16-LEAD PLASTIC FLAT PACKAGE (FPT-16P-M02)



Dimensions in inches (millimeters)

8306–15

Section 3

Memory Controllers

3

FUJITSU

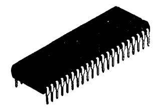
DYNAMIC RAM CONTROLLER LSI

MB 1422A

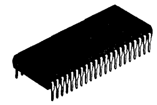
June 1986
Edition 1.0

DYNAMIC RAM CONTROLLER

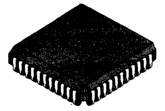
The Fujitsu MB 1422A is a high performance DRAM controller LSI.
The MB 1422A controls address multiplexing, refresh timing and their arbitration, and realizes one chip DRAM peripheral controller.
The MB 1422A is designed to easily interface 64K and 256K DRAM to the system based on the 8086 or 68000.
The MB 1422A is fabricated in an advanced low-power Schottky TTL process. The device is housed in a plastic 42-pin Dual In-line-Package, 42 pin shrink DIP, and 44-pin PLCC.



PLASTIC PACKAGE
DIP-42P-M01



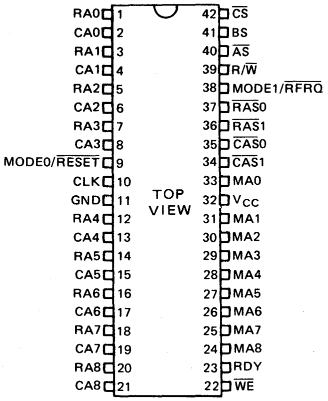
PLASTIC PACKAGE
DIP-42P-M02



PLASTIC PACKAGE
LCC-44P-M01

- 256k and 64k Dynamic-RAM control capability
- Directly addresses and drives up to 44 DRAMs without external drivers
- Internal/external refresh capability
- Supports 8086 (5MHz or 8MHz) or 68000 (8MHz or 12.5MHz) type microprocessor
- +5V only schottky TTL technology for high performance
- Low power dissipation: 440mW Typ.
- TTL compatible I/O
- Standard 42 pin Plastic DIP (Suffix: -P)
- Standard 42 pin Plastic Shrink DIP (Suffix: -P)
- Standard 44 pin Plastic LCC (Suffix: -PD)

PIN ASSIGNMENT



PLCC PIN ASSIGNMENT: See Page 21

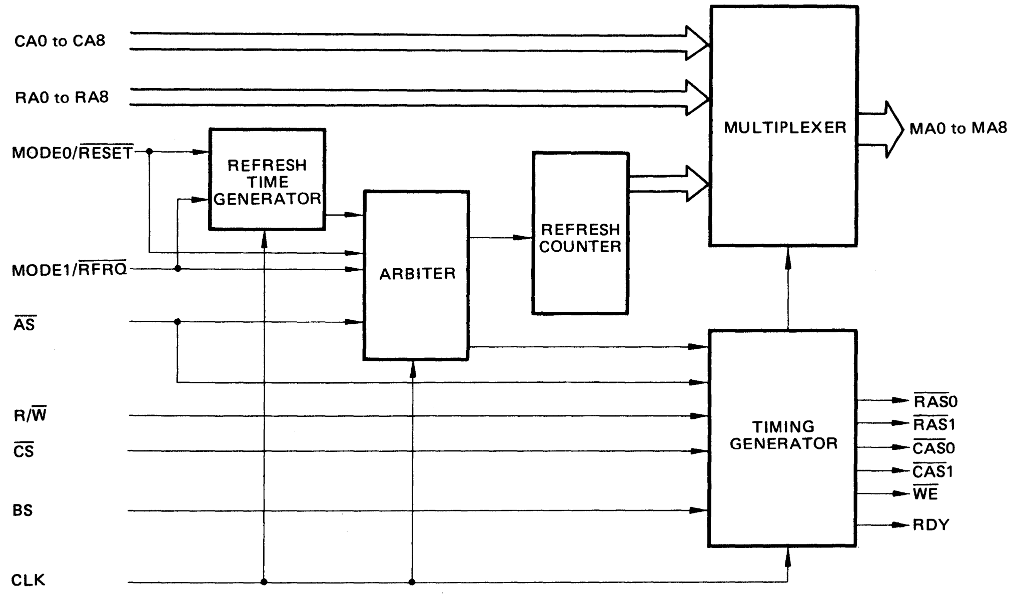
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Powery Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	-0.5 to +5.5	V
Output Voltage	V_O	-0.5 to +5.5	V
Operating Temperature	T_{OP}	-25 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 1422A BLOCK DIAGRAM



BLOCK FUNCTIONS

Multiplexer: Multiplexes the CPU addresses (CA and RA) and refresh address to nine row and nine column address.
Timing Generator: Generates $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ signals by address strobe (AS) and R/$\overline{\text{W}}$ signals from CPU and refresh request signal from the arbiter. Sends select signals for row, column or refresh address to multiplexer.
Refresh Counter: Generates the refresh address and counts up at each cycle.
Refresh Time Generator: Generates an internal refresh request signal.
Arbiter: Resolves the conflict of read/write and refresh cycle.

Table 1 – PIN DESCRIPTION

Symbol	Pin		Type	Pin Name and Function
	DIP	PLCC		
MODE0/$\overline{\text{RESET}}$	9	10	I	**Internal/External Refresh Select;** This pin is used to select refresh mode, internal refresh or external refresh. If MODE0/$\overline{\text{RESET}}$ = "H", internal refresh mode is selected. If MODE0/$\overline{\text{RESET}}$ = "L", external refresh mode. The falling edge of MODE0/$\overline{\text{RESET}}$ resets the refresh address counter.
MODE1/$\overline{\text{RFRQ}}$	38	40	I	**Internal Interval Select/External Refresh Request;** When Internal Refresh mode is selected (MODE0/$\overline{\text{RESET}}$ = "H"), this pin is used as refresh interval selection. If CLK ≥ 15MHz, it must be "L", and if CLK -24 to 25MHz, it must be "H". When External Refresh mode is selected (MODE0/$\overline{\text{RESET}}$ = "L"), this pin is used as refresh request. And the refresh starts when MODE1/$\overline{\text{RERQ}}$ = "L" is strobed by the falling edge of CLK.
$\overline{\text{AS}}$	40	42	I	**Address Strobe;** Memory access starts when $\overline{\text{AS}}$ = "L" is strobed by the falling edge of CLK, and ends at the rising edge of $\overline{\text{AS}}$, that is, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ become "H" (inactive) when $\overline{\text{AS}}$ turns "H" except refresh mode. The $\overline{\text{AS}}$ must be kept "L" until $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths have been satisfied for $\overline{\text{DRAM}}$ specifications.
R/$\overline{\text{W}}$	39	41	I	**Read/Write Control;** This pin is used to select memory read or write mode. If R/$\overline{\text{W}}$ = "H", read mode is selected. If R/$\overline{\text{W}}$ = "L", write mode.
$\overline{\text{CS}}$	42	44	I	**Chip Select;** This pin is used to control the states of output pins except for RDY. When $\overline{\text{CS}}$ = "H", $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and MA (MA0 to MA8) become high impedance state.
BS	41	43	I	**Bank Select;** This pin is used to select either of the two banks of DRAM arrays. If BS = "L", the lower bank ($\overline{\text{RAS0}}$) is selected. If BS = "H", the upper bank ($\overline{\text{RAS1}}$) is selected.
CLK	10	11	I	**Clock input;** This input provides basic timing for the internal logic. 8086 (5MHz) → CLK = 15MHz 8086 (8MHz) → CLK = 24MHz 68000 (8MHz) → CLK = 16MHz 68000 (12.5MHz) → CLK = 25MHz The CLK frequency should be higher or equals to 15MHz.
RA0 RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8	1 3 5 7 12 14 16 18 20	2 4 6 8 13 15 17 19 21	I	**Row Address;** These inputs are used to generate memory row address.

I: Input, O*: 3-State output

Table 2 – PIN DESCRIPTION (Continuted)

Symbol	Pin		Type	Pin Name and Function
	DIP	PLCC		
CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 CA8	2 4 6 8 13 15 17 19 21	3 5 7 9 14 16 18 20 22	I	**Column Address;** These inputs are used to generate memory column address.
$\overline{\text{RAS}}$0 $\overline{\text{RAS}}$1	37 36	39 38	O*	**Row Address Strobe;** These outputs are used by DRAM to strobe Row Address present on MA0 to MA8. Either $\overline{\text{RAS}}$0 or $\overline{\text{RAS}}$1 is selected by BS. The selected $\overline{\text{RAS}}$ is issued after $\overline{\text{AS}}$ = "L" is strobed by the falling edge of CLK. In the refresh mode (both Internal and External), both $\overline{\text{RAS}}$0 and $\overline{\text{RAS}}$1 are issued. These outputs become high impedance state if $\overline{\text{CS}}$ = "H". Each output drives maximum 22 DRAMs directly without external driver.
$\overline{\text{CAS}}$0 $\overline{\text{CAS}}$1	35 34	37 36	O*	**Column Address Strobe;** These outputs are used by DRAM to strobe column address, present on MA0 to MA8. These outputs are issued from the CLK rising edge, which is 1.5 CLK cycles after $\overline{\text{AS}}$ = "L" is strobed, with delay time of t_{CASN}. (See Fig. 4 and 5.) These outputs are not controlled by BS, i.e., both $\overline{\text{CAS}}$0 and $\overline{\text{CAS}}$1 are issued every memory access. In the refresh mode (both Internal and External), these outputs are kept "H". These outputs become high impedance state if $\overline{\text{CS}}$ = "H". Each output drives maximum 22 DRAMs directly without external driver.
$\overline{\text{WE}}$	22	24	O*	**Write Enable;** This output is used by DRAM to control read or write cycle. This output depends on R/$\overline{\text{W}}$ input, i.e., it is asynchronous with CLK. This output drives maximum 44 DRAMs directly without external driver.
RDY	23	25	O	**Ready;** This output identifies whether the memory arrays is refresh mode. If RDY = "L", refresh is excuted. If RDY = "H", refresh is not executed.
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8	33 31 30 29 28 27 26 25 24	35 33 32 31 30 29 28 27 26	O*	**Memory Address;** These outputs are used by DRAM for address inputs, row, column and refresh row address. These outputs can drive maximum 44 DRAMs directly without external driver. These outputs become high impedance state if $\overline{\text{CS}}$ = "H".

I: Input, O*: 3-State output, O: Output

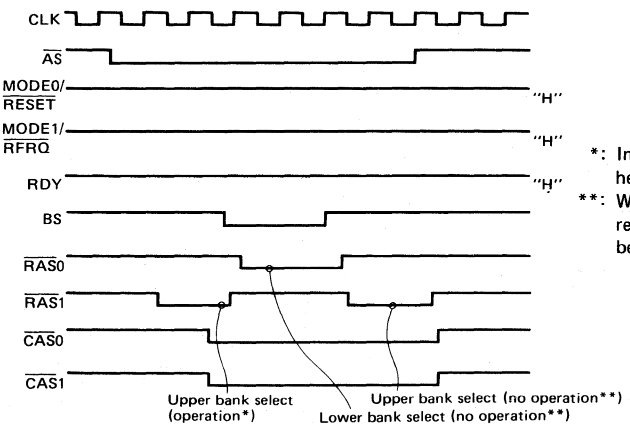
FUNCTIONAL DESCRIPTION

Read/Write Cycle Mode;

The memory read and write cycle starts from $\overline{\text{AS}}$ = "L". The selected $\overline{\text{RAS}}$ is issued after half cycle period from the falling edge of CLK which strobes $\overline{\text{AS}}$ = "L". The $\overline{\text{CAS}}$ is issued after 1.5 cycles from $\overline{\text{AS}}$ strobed. The $\overline{\text{AS}}$ input must satisfy the set up time, T_{ASSL}, referenced to the falling edge of CLK. The address at MA0 to MA8 are changed from row to column at the 3rd rising edge of CLK. The $\overline{\text{WE}}$ output depends on R/$\overline{\text{W}}$ input, controlled by neither CLK nor $\overline{\text{AS}}$, i.e., if R/$\overline{\text{W}}$ changes from "H" to "L" in memory cycle ($\overline{\text{AS}}$ = "L"), $\overline{\text{WE}}$ is changed regardless of states of $\overline{\text{AS}}$ and CLK. Therefore, Read-Modify-Write cycle can be executed. Refer to the "APPLICATION" section below.

The bank select (BS) must not change during $\overline{\text{AS}}$ = "L" because the $\overline{\text{RAS}}$'s are controlled by BS. If BS were changed during $\overline{\text{AS}}$ = "L", the both $\overline{\text{RAS}}$ ($\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$) would be selected during one memory access cycle. Refer to the Fig. 2.

Fig. 2 – BANK SELECTION


CLK
$\overline{\text{AS}}$
MODE0/$\overline{\text{RESET}}$
"H"
MODE1/$\overline{\text{RFRQ}}$
"H"
RDY
"H"
BS
$\overline{\text{RAS0}}$
$\overline{\text{RAS1}}$
$\overline{\text{CAS0}}$
$\overline{\text{CAS1}}$
Upper bank select (operation*)
Upper bank select (no operation**)
Lower bank select (no operation**)

*: In the read cycle, the data on upper bank are held valid until $\overline{\text{CAS}}$ goes "H".

**: When the DRAM has the "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh mode, the DRAM executes the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

Refresh Mode;

The MB 1422A provides two types of refresh modes as internal refresh mode and external refresh mode selected by MODE0/$\overline{\text{RESET}}$. Both $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ are issued during refresh mode Both $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ are set "H" until completion of the refresh cycles.

The refresh addresses are provided by internal refresh counter on MA0 to MA8 before issuing $\overline{\text{RAS}}$.

During refresh mode (both internal and external), RDY is set "L" to identify the MB 1422A is in refresh cycle.

When $\overline{\text{AS}}$ is brought "L" during RDY = "L", the memory access (both Read and Write Cycle) is ignored and the MB 1422A executes $\overline{\text{RAS}}$-only refresh.

1. Internal Refresh Mode;

   The internal refresh mode is selected by MODE0/$\overline{\text{RESET}}$ = "H" and executed by internal refresh request.

   In the internal refresh mode, the refresh is automatically taken place by the specified period since internal refresh request signal is generated by the refresh time generator. The internal refresh will be completed within ten CLK cycles, therefore, the RDY remains "L" until ten CLK cycles.

2. External Refresh Mode;

   The external refresh mode is selected by MODE0/$\overline{\text{RESET}}$ = "L" and executed when the MODE1/$\overline{\text{REFQ}}$ = "L" is strobed by the falling edge of CLK.

   The external refresh will be completed within twelve CLK cycles after MODE1/$\overline{\text{RFRQ}}$ = "L" is strobed by the falling of CLK. However, the RDY is kept "L" within ten CLK cycles. Because the first falling edge of CLK after MODE1/$\overline{\text{RFRQ}}$ = "L" is used to check the status of $\overline{\text{AS}}$ and the second falling edge is used to issue RDY signal.

   If $\overline{\text{AS}}$ = "L" is strobed by the first falling edge of CLK, the MB 1422A executes memory access (read or write) first and refresh mode.

Arbitration of memory access and refresh request;

The MB 1422A arbitrates memory access and refresh request. If refresh request, either external or internal, is strobed during memory access cycle, the MB 1422A executes memory access cycle first and refresh cycle. On the other hands, if memory access request is strobed during refresh mode the memory access request will be ignored until the end of refresh cycle.

FUNCTIONAL TRUTH TABLE

BS	READ/WRITE CYCLE		REFRESH CYCLE	
	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS0}$	$\overline{RAS1}$
L	Valid	H	Valid	
H	H	Valid		

$\overline{CS}$	MA0 to MA8	$\overline{RAS0}$ $\overline{RAS1}$	$\overline{CAS0}$ $\overline{CAS1}$	$\overline{WE}$
L	Valid			
H	High-Z			

MODE0/$\overline{RESET}$	MODE1/$\overline{RFRQ}$	Function
H	L	Internal Refresh mode, CLK ≥ 15MHz*
H	H	Internal Refresh mode, CLK = 24 to 25 MHz**
L	$\overline{RFRQ}$	External refresh mode

*: For 8086 (5MHz) and 68000 (8MHz), the refresh is executed once in every 232 CLK cycles.

**: For 8086 (8MHz) and 68000 (12.5MHz), the refresh is executed once in every 372 CLK cycles.

DRAM INTERFACE

Addressing;

The MB 1422A is capable to address directly maximum 512K address with 256K DRAM. Fig. 3 shows the example of interfacing between MPU and MB 1422A for both 64K and 256K DRAM system. The DRAMs require address set-up and hold times on both row and column addresses. The MB 1422A resolves such critical timing requirement. Fig. 4 shows an example of calculation of address set up and hold times.

Fig. 3 – INTERFACING BETWEEN MPU AND DRAM

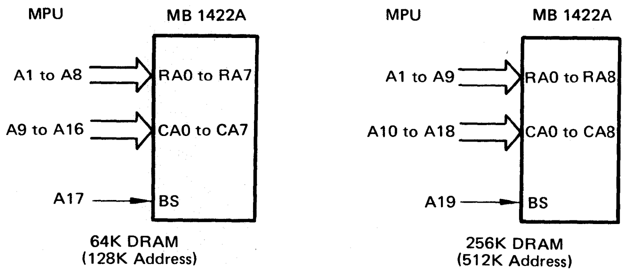
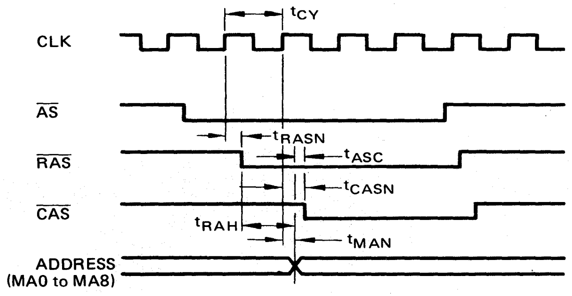


Fig. 4 – EXAMPLE OF ADDRESS SET UP AND HOLD TIME CALCULATION



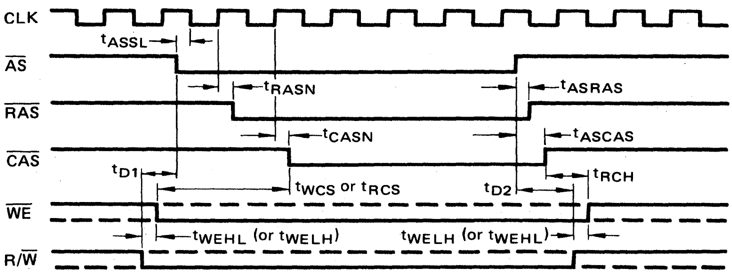
$t_{ASC} = t_{CASN}\,(\text{Min}) - t_{MAN}\,(\text{Max})$

$t_{RAH} = t_{CY}\,(\text{Min}) + t_{MAN}\,(\text{Min}) - t_{RASN}\,(\text{Max})$

Read/Write Command;

Since the $\overline{\text{WE}}$ depends on R/$\overline{\text{W}}$, it must be taken a care to set-up and hold times for Read and Write command. Therefore, R/$\overline{\text{W}}$ must be valid before $\overline{\text{CAS}}$ = "L", and R/$\overline{\text{W}}$ must not be changed until Read or Write command hold time has been satisfied except for read-modify-write cycle. Fig. 5 shows an example of calculation of Read/Write command set up times.

Fig. 5 – READ/WRITE COMMAND SET UP/HOLD TIME



Set Up Time;

$t_{WCS} = (t_{CASN} + 1.5t_{CY} + t_{ASSL}) - (t_{D1} + t_{WEHL})$

$t_{RCS} = (t_{CASN} + 1.5t_{CY} + t_{ASSL}) - (t_{D1} + t_{WELH})$

Hold Time;

$t_{RCH} = t_{D2} - t_{ASCAS} + t_{WEHL}$

Initiallization;

In the single power supplied DRAM which has substrate bias generator, it is necessary 200μs pause time to let substrate stable and after that eight dummy $\overline{\text{RAS}}$ cycles must be done for initiallization of internal dynamic circuitly.

Therefore, memory access is not executed correctly until the above pause time and eight dummy cycles have been satisfied. In the case of using internal refresh mode, eight $\overline{\text{AS}}$ clocks or eight refresh cycles must be applied after 200μs pause time.

On the other hand, in the case of using external refresh mode eight refresh cycles (keeping MODE1/$\overline{\text{RFRQ}}$ = "L" until eight $\overline{\text{RAS}}$ = "L" is detected) or eight $\overline{\text{AS}}$ cycles must be applied.

Refresh;

The MB 1422A is capable of doing refresh mode for both 2ms/128 cycles and 4 ms/256 cycles.

MPU INTERFACE

The MB 1422A is capable of interfacing with both 8086 and 6800.
The examples of interfacing with these MPU's are shown in Fig. 6 and 7.

Fig. 6 – EXAMPLE OF INTERFACE BETWEEN MB 1422A AND 8086

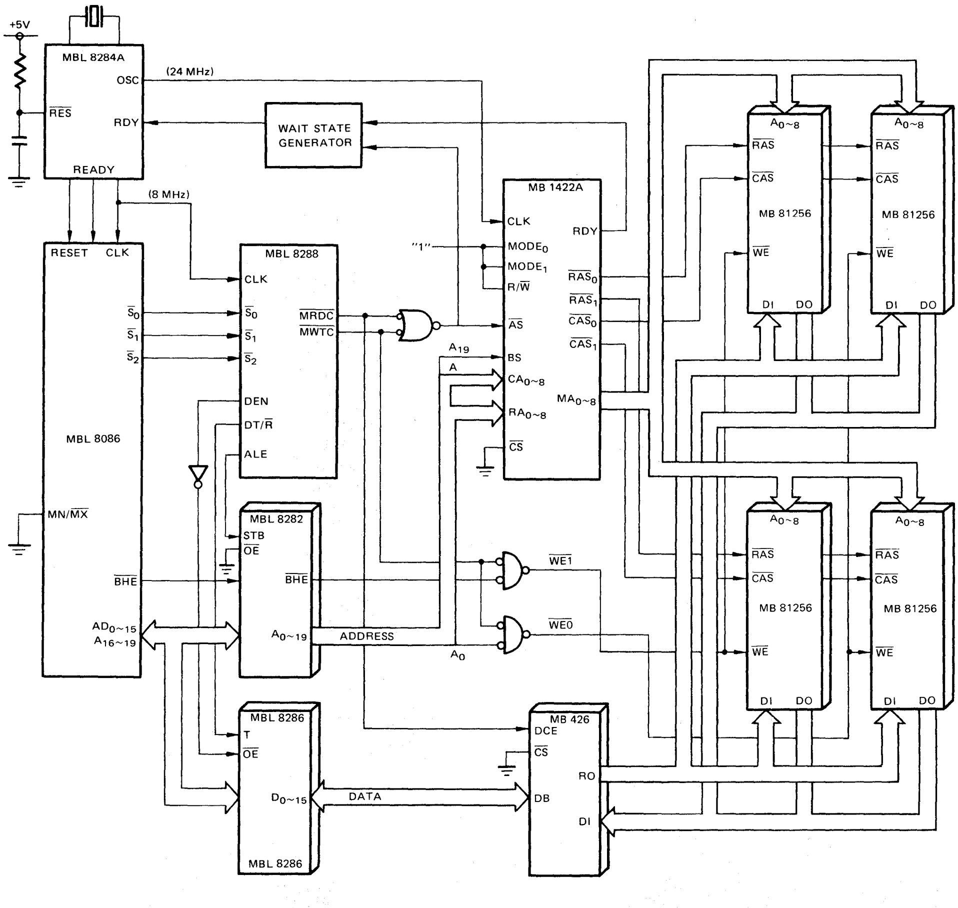
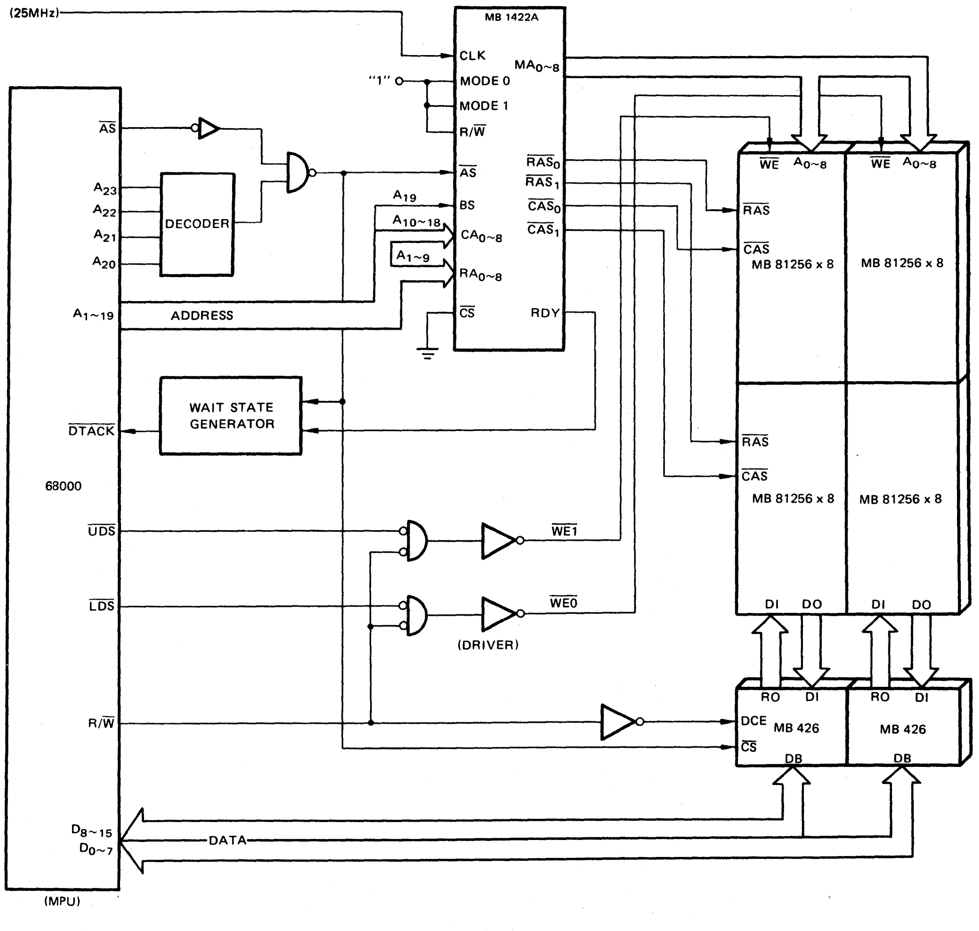


Fig. 7 – EXAMPLE OF INTERFACE BETWEEN MB 1422A AND 68000

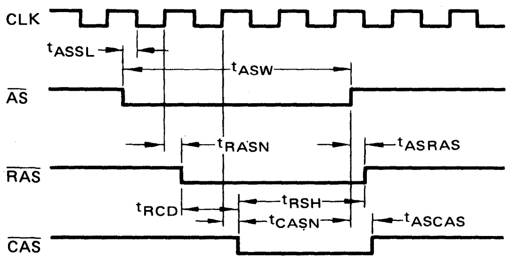


APPLICATION

Memory Access Cycle Time;

Since memory access cycle depends on $\overline{AS}$, the memory cycle time can be controlled by $\overline{AS}$. The minimum cycle time can be calculated with Fig. 8.

Fig. 8 – MEMORY ACCESS CYCLE TIME



Hence, $t_{RCD} = t_{CY} + t_{CASN} - t_{RASN}$
$t_{RSH} = 75ns$ (min) → MB 81256-15

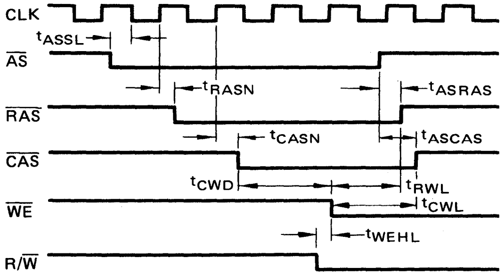
The minimum $\overline{AS}$ Pulse Width must be $t_{RSH} + t_{RCD} + t_{RASN} + 0.5t_{CY} + t_{ASSL} - t_{ASRAS}$.

The maximum $\overline{AS}$ pulse width must not be greater than maximum t_{RAS} of DRAM.

Read-Modify-Write;

The MB 1422A provides a capable of read-modify-write and delayed write cycle by delayed write command input on R/$\overline{W}$. Fig. 9 shows an example of write command on R/$\overline{W}$ for read-modify-write cycle.

Fig. 9 – WRITE COMMAND INPUT FOR READ-MODIFY-WRITE



In the Read-Modify-Write cycle, the write command ($\overline{WE}$) should be delayed with t_{CWD}. Therefore, the write command on the R/$\overline{W}$ should be delayed.

Delay Time of R/$\overline{W}$ from $\overline{AS}$ is;

$t_{ASSL} + 1.5t_{CY} + t_{CASN} + t_{CWD} - t_{WEHL}$.

The t_{RWL} and t_{CWL} must be noticed in the read-modify-write cycle.
Therefore, $\overline{AS}$ must be "L" until delay time of $t_{CWL} - t_{ASCAS}$ and $t_{RWL} - t_{ASRAS}$ have been satisfied.

Refresh;

There are two ways for refreshing DRAM in the memory system as cycle steal (or distributed) refresh and burst refresh.

The MB 1422A provides both ways.

In the internal refresh mode, cycle steal refresh is taken place automatically without any external control circuit.

On the other hands, in the external refresh mode, both ways can be used by controlling MODE1/$\overline{\text{RFRQ}}$ input.

1. Cycle Steal Refresh

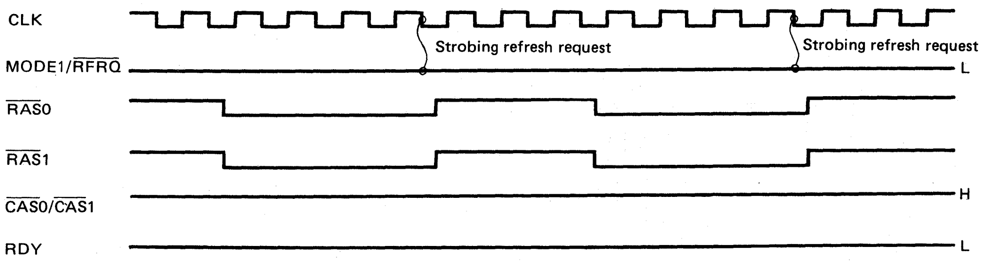
   The cycle steal refresh is taken place by the period divided required refresh period by required refresh cycle, i.e., 4ms/256 = 15.6μs, and the refresh request should be applied at a period of 15.6μs. In the external refresh mode the refresh period counter is necessary for this purpose.

2. Burst Refresh

   The burst refresh is taken place by doing refresh for all required refresh cycles continuously, i.e., the refresh request should be applied at a period of required refresh cycles. When MODE1/$\overline{\text{RFRQ}}$ is kept "L" through all refresh cycles (256 or 128), one refresh cycle will be completed within seven CLK cycles because next refresh request is strobed during the refresh cycle.

   Fig. 10 shows an example of burst refresh cycle with keep MODE1/$\overline{\text{RFRQ}}$ = "L" through the cycle.

Fig. 10 – BURST REFRESH



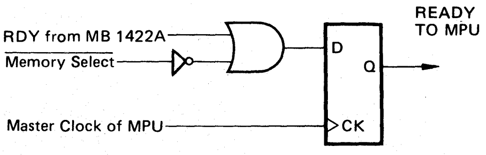
RDY Output;

The MB 1422A issues ready signal to identify whether DRAM array is ready or not. The following cautions are necessary to send RDY to MPU.

- RDY must be sent only when the DRAM array is being accessed.
- RDY must be sent synchronously with MPU operation.
- RDY must be sent before MPU starts operation, and if RDY is issued during MPU operation, RDY must be held until the completion of current MPU operation and then sent to MPU.

The Fig. 11 shows an example of external circuit to send RDY to MPU.

Fig. 11 – EXAMPLE OF RDY INTERFACE TO MPU



In this case, both set up and hold times on READY of MPU must be satisfied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	*V_{CC}	4.5	5.0	5.5	V
Output High Current	I_{OH}	–	–	-3.3	mA
Output Low Current	I_{OL}	–	–	10	mA
Ambient Temperature	T_A	0	–	70	°C

***: Referenced to GND**

DC CHARACTERISTICS

(Recommended Operation Conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Conditions
			Min.	Typ.	Max.		
Supply Current		I_{CC}		88*	145	mA	V_{CC} = 5.5V
Input Low Current	Except for CLK and $\overline{CS}$	I_{IL}			-200	μA	V_{CC} = 5.5V, V_{IN} = 0.5V
	CLK, $\overline{CS}$				-400		
Input High Current		I_{IH1}			20	μA	V_{CC} = 5.5V V_{IN} = 2.4V
		I_{IH2}			100		V_{CC} = 5.5V, V_{IN} = 5.5V
Input Clamp Voltage		V_{IC}			-1.5	V	V_{CC} = 4.5V, I_{IN} = –18mA
Output Low Voltage		V_{OL}			0.5	V	V_{CC} = 4.5V, I_{OL} = 10mA
Output High Voltage		V_{OH}	2.4			V	V_{CC} = 4.5V, I_{OH} = –3.3mA
Output Leakage Current (High-Z)		I_{OZ}	-100		100	μA	V_{CC} = 5.5V, V_{OUT} = 0.5V/2.4V
Output Short Circuit Current		I_{OS}	-50	-100*	-200	mA	V_{CC} = 5.5V, V_{OUT} = 0V
Input Low Voltage		V_{IL}	–	–	0.8	V	
Input High Voltage		V_{IH}	2.0	–	–	V	

*: All typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

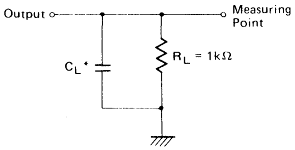
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
$\overline{AS}$ Low Set up Time to CLK	t_{ASSL}	10			ns
$\overline{FRRQ}$ Low Set up Time to CLK	t_{RFRQS}	10			ns
$\overline{RFRQ}$ Low Hold Time to CLK	t_{RFRQH}	10			ns
$\overline{RFRQ}$ High Set up Time to CLK	t_{REFSS}	10			ns
$\overline{AS}$ High Set up Time to CLK	t_{ASSH}	10			ns
BS Set up Time to CLK	t_{BSS}	10			ns
BS Hold Time to $\overline{AS}$	t_{BSH}	10			ns
CLK High Time	t_{WP}	15			ns
CLK Low Time	t_{WN}	15			ns
Delay Time from CLK to $\overline{RAS}$n	t_{RASN}		20	32	ns
Delay Time from $\overline{AS}$ to $\overline{RAS}$n	t_{ASRAS}		18	30	ns
Delay Time from CLK to $\overline{CAS}$n	t_{CASN}		37	52	ns
Delay Time from $\overline{AS}$ to $\overline{CAS}$n	t_{ASCAS}		36	53	ns
Delay Time from RAm to MAm	t_{RAMA}		21	35	ns
Delay Time from CLK to MAm	t_{MAN}		27	42	ns
Delay Time from CAm to MAm	t_{CAMA}		21	35	ns
Delay Time from $\overline{AS}$ to MAm	t_{ASMA}		23	39	ns
Delay Time from R/$\overline{W}$ to $\overline{WE}$	t_{WEHL}		16	25	ns
	t_{WELH}		17	28	ns
Delay Time from CLK to $\overline{RAS}$n (Refresh cycle)	t_{RASRHL}		24	36	ns
	t_{RASRLH}		25	37	ns
Delay Time from CLK to MAm (Refresh cycle)	t_{MAR}		33	51	ns
Delay Time from CLK to RDY (Refresh cycle)	t_{RDYHL}		23	35	ns
	t_{RDYLH}		21	32	ns
Address Enable Time from $\overline{CS}$	t_{PZHMA}		24	43	ns
	t_{PZLMA}		24	41	ns
$\overline{WE}$ Enable Time from $\overline{CS}$	t_{PZHWE}		24	43	ns
	t_{PZLWE}		24	41	ns
$\overline{RAS}$/$\overline{CAS}$ Enable Time from $\overline{CS}$	t_{PZHRC}		20	38	ns
	t_{PZLRC}		23	41	ns
Address Disable Time from $\overline{CS}$	t_{PHZMA}		36	56	ns
	t_{PLZMA}		32	48	ns
$\overline{WE}$ Disable Time from $\overline{CS}$	t_{PHZWE}		36	56	ns
	t_{PLZWE}		32	48	ns
$\overline{RAS}$/$\overline{CAS}$ Disable Time from $\overline{CS}$	t_{PHZRC}		33	48	ns
	t_{PLZRC}		23	39	ns
Column Address to $\overline{CAS}$ Set up Time	t_{ASC}	0			ns
$\overline{RAS}$ Puls Width (Refresh cycle)	t_{WRAS}	150			ns
Delay Time from $\overline{RAS}$ to $\overline{CAS}$	t_{RCA}	25			ns
Row Address Hold Time	t_{RAH}	20			ns

n; 0, 1

m; 0, 1, 2, 4, 5, 6, 7, 8

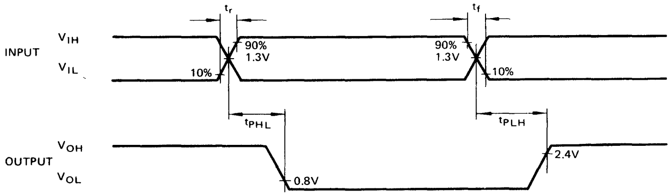
AC CHARACTERISTICS TEST CONDITIONS

1. DELAY TIME



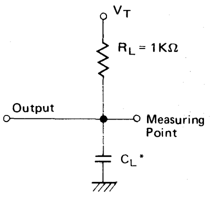
Pin Name	C_L (std)
MA0 to MA8	300pF
$\overline{WE}$	300pF
$\overline{RAS0}$ and $\overline{RAS1}$	200pF
$\overline{CAS0}$ and $\overline{CAS1}$	200pF
RDY	150pF

* Including jig capacitance.



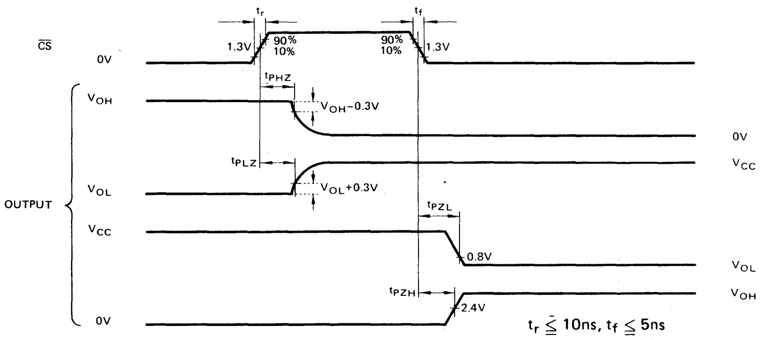
Input conditions;
$V_{IH} = 3V, V_{IL} = 0V, t_r \leq 10ns, t_f \leq 5ns$

2. ENABLE/DISABLE TIME



	Symbol	Pin Name	CL (pF)	VT (V)
Disable time measure-ment	t_{PLZ}	MA0 to MA8, $\overline{WE}$	300	V_{CC}
		$\overline{RAS}$, $\overline{CAS}$	200	
	t_{PHZ}	MA0 to MA8, $\overline{WE}$	300	0
		$\overline{RAS}$, $\overline{CAS}$	200	
Enable time measure-ment	t_{PZL}	MA0 to MA8, $\overline{WE}$	300	V_{CC}
		$\overline{RAS}$, $\overline{CAS}$	200	
	t_{PZH}	MA0 to MA8, $\overline{WE}$	300	0
		$\overline{RAS}$, $\overline{CAS}$	200	

* Including jig capacitance.



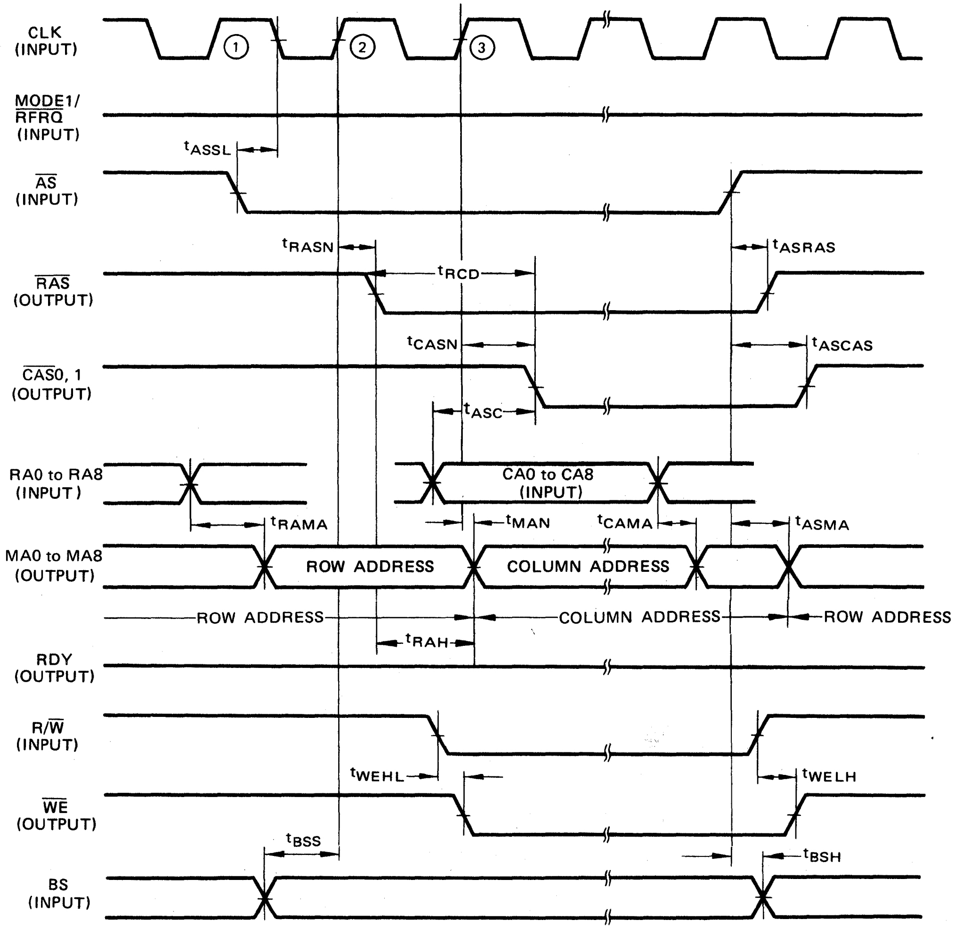
Delay time calcuration

When the load capacitance is different from the standard value shown above, the delay time is specified according to the following equation.

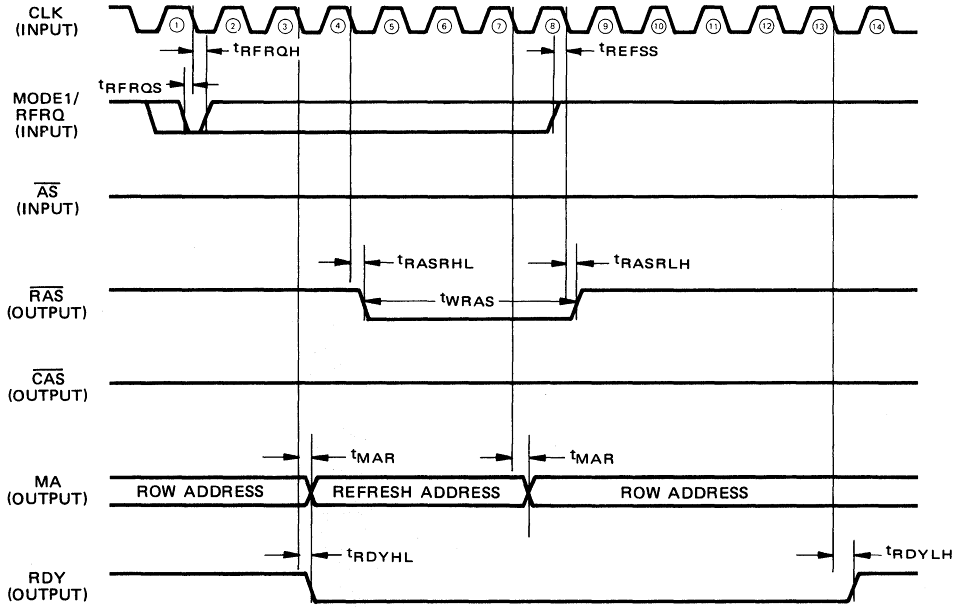
$t_{pd(CL)} = t_{pd(Std)} + 0.04 \times \triangle C_L, \triangle C_L = C_L - C_{L(Std)}$

Unit: t_{pd} = ns
C_L = pF

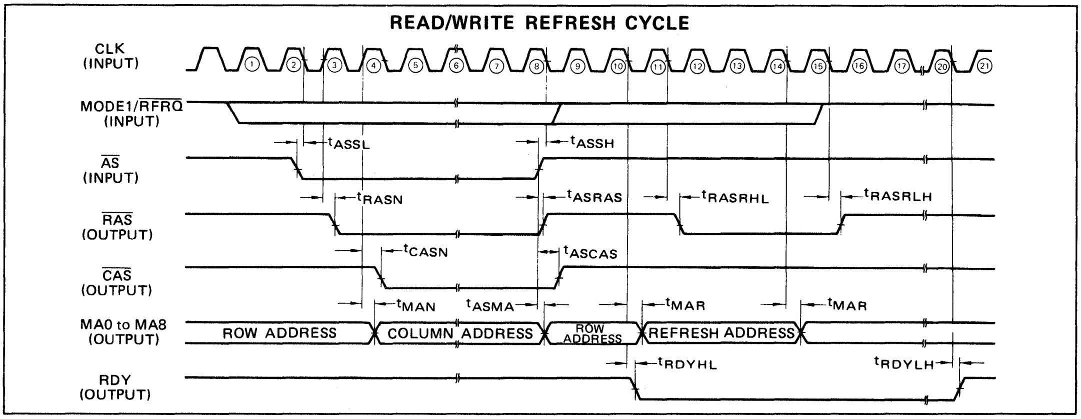
READ/WRITE CYCLE TIMING DIAGRAM



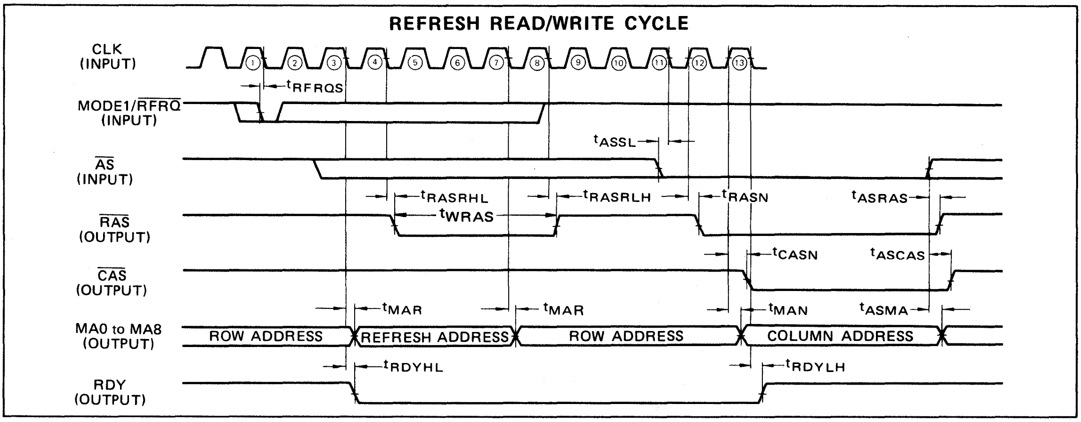
EXTERNAL REFRESH CYCLE TIMING DIAGRAM



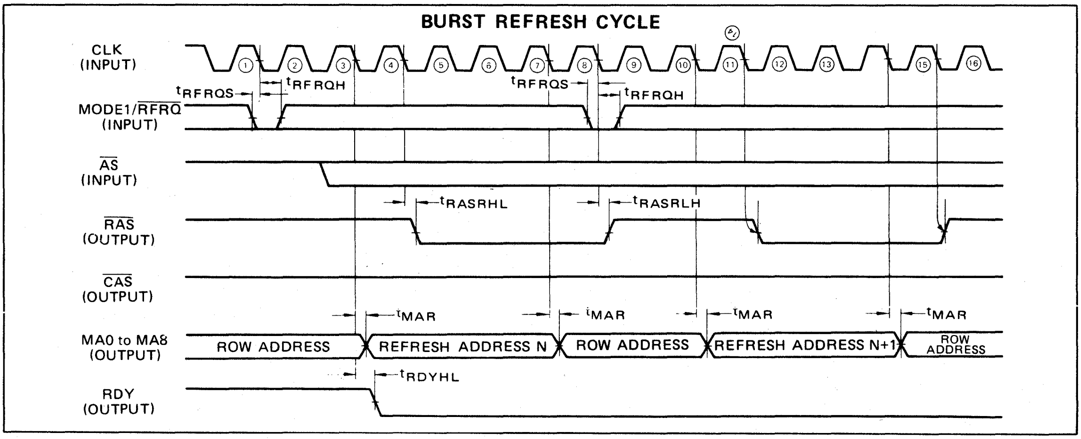
READ/WRITE REFRESH CYCLE



REFRESH READ/WRITE CYCLE



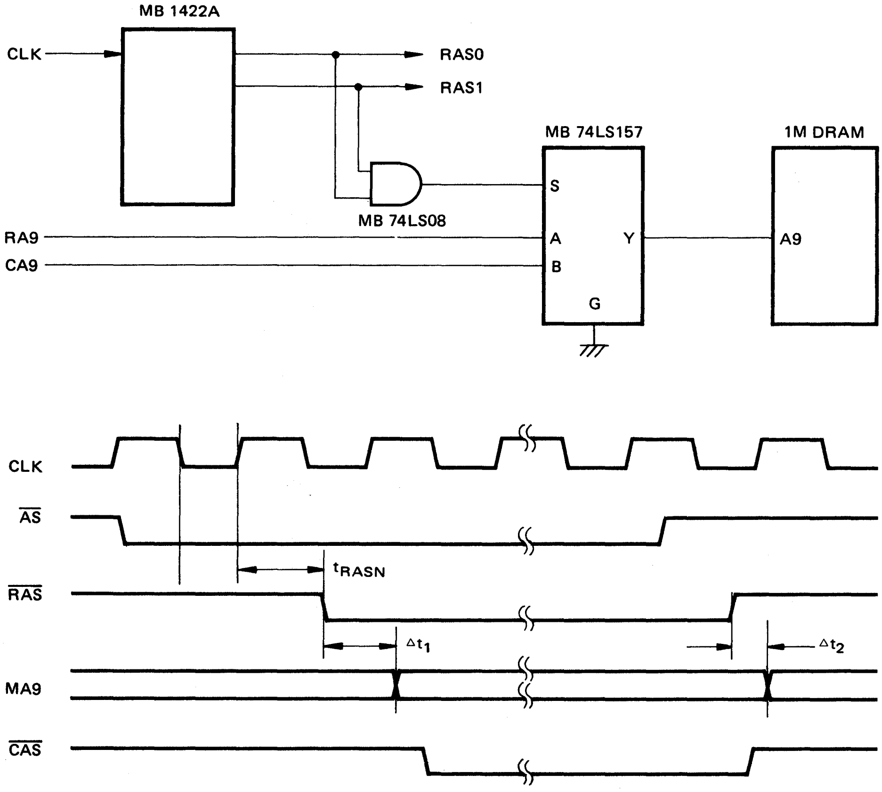
BURST REFRESH CYCLE



APPLICATION FOR 1M DRAM

The Fujitsu MB 1422A is designed to refresh all nine bits of memory addresses (MA0 to MA8). It can also, control 1M DRAMs by adding some external circuits.
Refer to the application circuits described below.

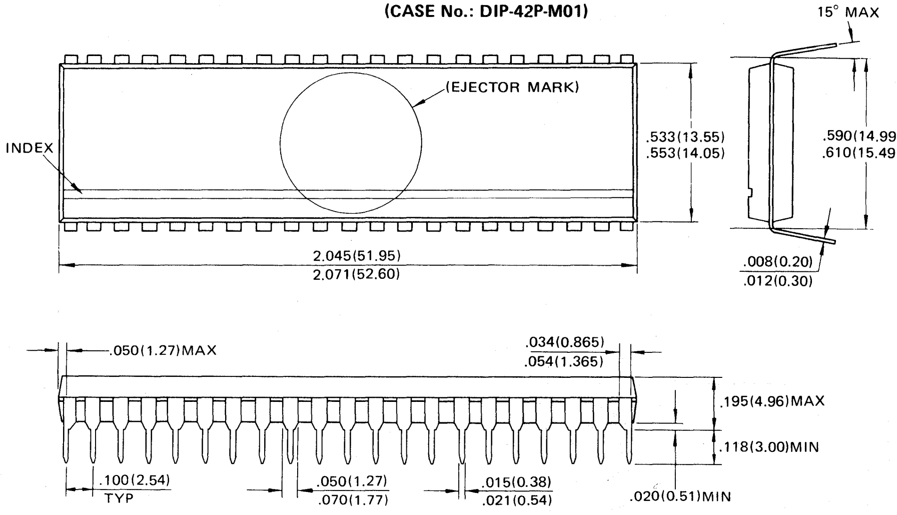
Fig. 12 – ADDITIONAL EXTERNAL CIRCUIT



$\Delta t1 = t_{PHL}$ (LS08) + t_{PLH} or t_{PHL} (LS157) $\geqq t_{RAH}$ (Row Address Hold Time)
$\Delta t2 = t_{PLH}$ (LS08) + t_{PLH} or t_{PHL} (LS157)

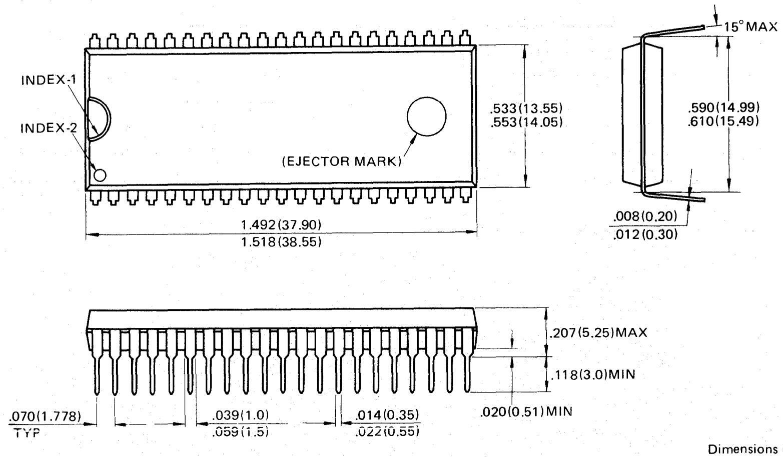
PACKAGE DIMENSIONS

42-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42P-M01)



Dimensions in
inches (millimeters)

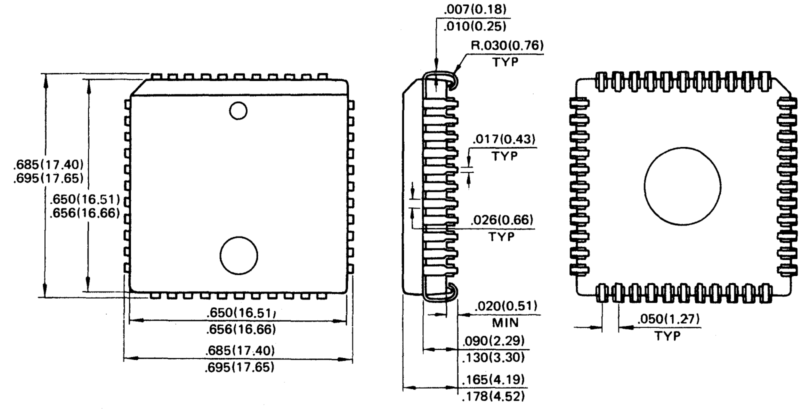
42-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-42P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

44-LEAD PLASTIC CHIP CARRIER
(CASE No.: LCC-44P-M01)



Dimensions in
inches (millimeters)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	15	RA5	29	MA5
2	RA0	16	CA5	30	MA4
3	CA0	17	RA6	31	MA3
4	RA1	18	CA6	32	MA2
5	CA1	19	RA7	33	MA1
6	RA2	20	CA7	34	VCC
7	CA2	21	RA8	35	MA0
8	RA8	22	CA8	36	CAS1
9	CA3	23	GND	37	CAS0
10	MODE0/RESET	24	WE	38	RAS1
11	CLK	25	RDY	39	RAS0
12	GND	26	MA8	40	MODE1/RFRQ
13	RA4	27	MA7	41	R/W
14	CA4	28	MA6	42	AS
				43	BS
				44	CS

FUJITSU

DYNAMIC RAM CONTROLLER

MB1430

ADVANCE INFORMATION

DESCRIPTION

The Fujitsu MB1430 Dynamic RAM (DRAM) Controller is a high-performance device that provides all control functions required to implement and supervise a multiple-DRAM memory. Major functions include multiplexed address control, memory refresh, and refresh arbitration. The MB1430 is designed to operate with systems based on the MBL8086, MBL80186, and the MBL80286 (5, 8, and 10 MHz) or the 68000 (8 and 12.5 MHz) microprocesors. Interface connections for 64K, 256K, and 1-megabit DRAMs are simple and straightforward. For optimum flexibility and to provide a high order of efficiency, the MB1430 supports all useful modes of operation; these include read-modify-write, nibble, fast page, and CAS-controlled byte operations. The MB1430 is fabricated using a low-power Schottky TTL process and the device is housed in a 48-pin plastic DIP.

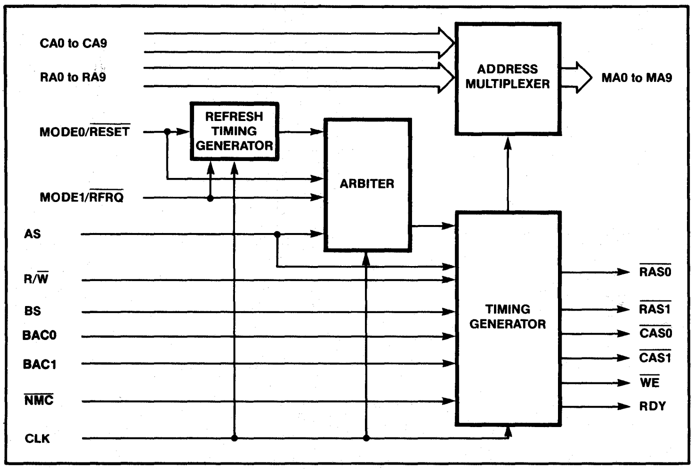
FEATURES

- Full-featured control for 64K-, 256K-, and 1-megabit DRAMs.
- Direct address-and-drive capabilities for up to 44 DRAM devices.
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.
- Internal/external refresh capability.
- Supports multiple operating modes.
- Easy interface to MBL8086, MBL80186, MBL80286 and 68000 microprocessor-based systems.
- TTL-compatible I/O.
- Low power consumption (typically 425 mW).
- Single +5V supply.

PIN CONFIGURATION

RA0	1	48	R/$\overline{\text{W}}$
CA0	2	47	FPC
RA1	3	46	MODE1/$\overline{\text{RFRQ}}$
CA1	4	45	$\overline{\text{RAS0}}$
RA2	5	44	$\overline{\text{RAS1}}$
CA2	6	43	$\overline{\text{CAS0}}$
RA3	7	42	$\overline{\text{CAS1}}$
CA3	8	41	MA0
RA4	9	40	MA1
MODE0/$\overline{\text{RESET}}$	10	39	MA2
CLK	11	38	MA3
GND	12	37	GND
$\overline{\text{AS}}$	13	36	VCC
CA4	14	35	MA4
RA5	15	34	MA5
CA5	16	33	MA6
RA6	17	32	MA7
CA6	18	31	MA8
RA7	19	30	MA9
CA7	20	29	$\overline{\text{RDY}}$
RA8	21	28	$\overline{\text{WE}}$
CA8	22	27	BAC1
RA9	23	26	BAC0
CA9	24	25	BS

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

LS-TTL ERROR CHECKING AND CORRECTION CIRCUIT

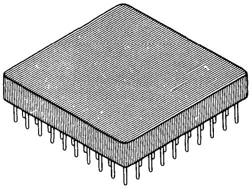
MB 1412A

May 1981

FUJITSU MB 1412A EIGHT-BIT SLICE ECC LSI

The MB 1412A is an 8-bit slice Error Checking and Correction (ECC) monolithic integrated circuit fabricated in a low-power Schottky TTL process. The device is utilized in memory system designs, and is suitable for constructing 2-byte, 4-byte, or 8-byte ECC circuitry. The MB 1412A will detect and correct single-bit errors, and detect double-bit errors utilizing a built-in modified Hamming single-error-correction, double-error-detection (SEC-DED) code. A 64-pin square package with 100 mil pin spacing is utilized for the MB 1412A to provide high board packing density.

- 8-bit slice ECC function in one LSI.
- 100% single-bit error detection/correction and double-bit error detection.
- Simplified circuit design for 2, 4, or 8-byte memory systems. 4/8-byte system requires only 4/8 ECC circuits and 4/8 TTL SSI devices.
- Uses built-in modified Hamming SEC-DED Code.
- 4/8-byte data word requires only 7/8 check bits for full SEC-DED operation.
- High speed: 31/47 nsec. typical for 4/8-byte detect system, 40/56 nsec, for 4/8-byte correct.
- Low-power dissipation: 1.6 watts maximum. For 8-byte system, 8.7 watts typical system power including peripheral circuitry.
- Low-power Schottky TTL process; single +5 volt supply.
- Space-saving 64-pin square-pack with 100 mil pin spacing.



CERAMIC PACKAGE
PGA-64C-M01

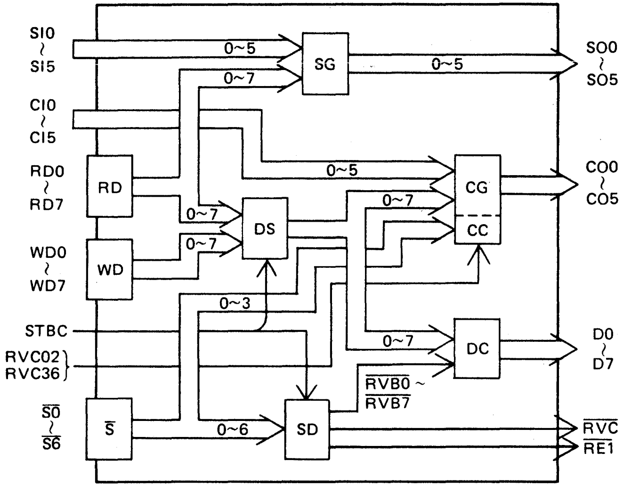
Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltates to this device.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	-0.5~+5.5	V
Temperature Under Operation	T_{op}	-25~+85	°C
Temperature Under Storage	T_{stg}	-65~+150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 MB 1412A BLOCK DIAGRAM



RD:	Read Data Buffer
SG:	Syndrome Generator
WD:	Write Data Buffer
DS:	Data Selector
CG:	Check-bit Generator
CC:	Check-bit Corrector
$\overline{S}$:	Syndrome Input Buffer
DC:	Data Corrector
SD:	Syndrome Decoder/Locator

FUNCTIONS OF BLOCK ELEMENTS

RD (Read Data Buffer)
Input buffer gate for memory read data.

SG (Syndrome Generator)
Generates syndrome for the data to be checked in the read data buffer.

WD (Write Data Buffer)
Input buffer gate for memory write data.

DS (Data Selector)
Selects RD or WD depending on the mode ("0" or "1") of the STBC input.

CG (Check-Bit Generator)
Generates check-bits for memory data being checked.

$\overline{S}$ (Syndrome Input Buffer)
Input buffer gate for synthesized syndrome input data.

SD (Syndrome Decoder/Locater)
Locates a data bit for correction and indicates when a one-bit error is detected.

DC (Data Corrector)
Corrects the data bit indicated as an error by the syndrome decoder.

CC (Check-bit Corrector)
Corrects one check-bit by reversing depending on the mode of RVC and $\overline{S}$.

INPUT/OUTPUT PINS

Input Pins:

RD0–RD7 (Read Data)
Memory data inputs. READ data operation is dictated when STBC is "0" (low).

WD0–WD7 (Write Data)
WRITE data inputs. WRITE data operation is dictated when STBC is "1" (high).

SI0–SI5 (Syndrome Input)
Syndrome code inputs to read the synthesized syndrome from the previous ECC LSI (SO output) in a cascaded multi-byte ECC system configuration. The syndrome inputs for the first ECC LSI in the system read memory check-bit data previously generated.

CI0–CI5 (Check-Bit Input)
Reads check-bits into the internal Check-Bit generator in a cascaded ECC system.

STBC (Store Byte Control)
Set "0" (low) to read RD inputs; set "1" (high) to read WD inputs.

$\overline{S0}$–$\overline{S5}$ (Synthesized Syndrome Input)
Reads the synthesized syndrome code output from the last ECC LSI (SO outputs) in a cascaded multi-byte ECC system configuration. $\overline{S0}$–$\overline{S5}$ must correspond to the order of the SO0–SO5 outputs on the same ECC LSI to accomplish syndrome decoding (see ECC system examples). In the event of a single data bit error (during memory READ), the syndrome decoder (SD) decodes $\overline{S0}$–$\overline{S5}$ to locate the error bit to be corrected. The binary location of the error bit is read from $\overline{S0}$–$\overline{S2}$ (e.g., $\overline{S0}$ = 0, $\overline{S1}$ = 1, $\overline{S2}$ = 0 is binary 010 or decimal "2" which corresponds to input data bit "2").

$\overline{S6}$ (Synthesized Syndrome Input #6)
Reads a synthesized syndrome bit output from a cascaded multi-byte ECC system configuration. A "0" input indicates that no bit error is detected within the read memory byte for the ECC IC, and forces the $\overline{RE1}$ and $\overline{RVC}$ outputs high (1). A "1" input indicates that a 1-bit error is detected within the read memory byte.

RVC02 (Reverse Check-Bit #02)
A "0" (low) input indicates no error detected. A "1" (high) indicates an error is detected within the input memory data byte, and corrects the first three check bits (see Fig. 13, C0–C2). A "0" on syndrome data $\overline{S0}$, $\overline{S1}$, or $\overline{S2}$ dictates correction of C0, C1, or C2 respectively.

RVC36 (Reverse Check-Bit #36)
A "0" (low) input indicates no correction to check-bit C3. A "1" (high) input performs correction of check-bit C3.

Output Pins:

SO0–SO5 (Syndrome Output)
Synthesized syndrome output code, normally connected to Syndrome Input (SI) in the next sequential ECC IC in a cascaded multi-byte ECC configuration. Syndromes are effective for the system at the output of the last ECC LSI in sequence.

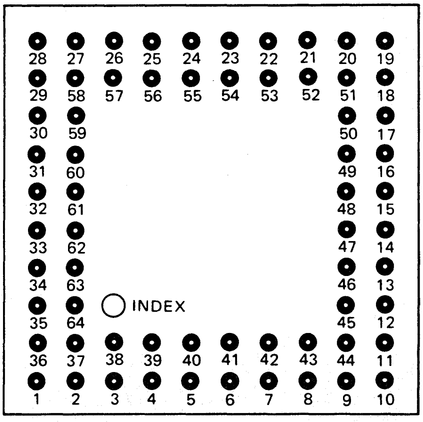
CO0–CO5 (Check-Bit Output)
Check-bit output code, normally connected to Check-Bit Input (CI) in the next sequential ECC LSI in a cascaded multi-byte ECC configuration. Check-bits are effective for the system at the output of the last ECC LSI in sequence.

$\overline{RE1}$ (Read Error One)
A "0" (low) indicates that a one-bit error has occurred in fetched data or check bits.

$\overline{RVC}$ (Reverse Check-Bit)
A "0" (low) indicates that an error in check-bit must be corrected.

D0–D7 (Data Output)
Corrected data output.

Fig. 2 PIN ASSIGNMENT OF PACKAGE



TOP VIEW

Fig. 3 PIN ASSIGNMENT TABLE

PIN NO.	I/O	NAME	PIN NO.	I/O	NAME
1	I	RVC02	33	O	D7
2	O	CO0	34	O	D5
3	I	CI1	35	O	D3
4	I	CI2	36	O	D1
5	O	CO2	37	O	D0
6	I	RVC36	38	I	CI0
7	I	CI3	39	O	CO1
8	I	CI4	40	–	GND
9	I	CI5	41	O	CO3
10	I	WD1	42	O	CO4
11	I	WD3	43	O	CO5
12	I	WD4	44	I	WD0
13	I	WD6	45	I	WD2
14	I	WD7	46	I	WD5
15	I	STBC	47	–	VCC
16	I	RD1	48	I	RD0
17	I	RD3	49	I	RD2
18	I	RD5	50	I	RD4
19	I	RD7	51	I	RD6
20	O	SO0	52	I	SI0
21	I	SI1	53	O	SO1
22	I	SI2	54	–	GND
23	O	SO2	55	I	SI3
24	O	SO3	56	I	SI4
25	O	SO4	57	I	SI5
26	O	SO5	58	I	$\overline{S1}$
27	I	$\overline{S0}$	59	I	$\overline{S3}$
28	I	$\overline{S2}$	60	I	$\overline{S6}$
29	I	$\overline{S4}$	61	–	VCC
30	I	$\overline{S5}$	62	O	D6
31	O	$\overline{RE1}$	63	O	D4
32	O	$\overline{RVC}$	64	O	D2

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	T_{OP}
Power Supply Voltage	V_{CC}	5.0V ±5%	0°C – 70°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
Output Low Level		V_{OL}			0.5	V	V_{CC}=4.75V, V_{IL}=0.8V V_{IH}=2.0V, I_{OL}=20mA
Output High Level		V_{OH}	2.7			V	V_{CC}=4.75V, V_{IL}=0.8V V_{IH}=2.0V, I_{OH}=1mA
Input Low Current	RDn, WDn, $\overline{\text{Sn}}$, RVC02, RVC36	I_{IL1}			1.6	mA	V_{CC}=5.25V, V_{IL}=0.5V
	STBC	I_{IL2}			3.2	mA	
	SIn, CIn	I_{IL3}			4.8	mA	
Input High Current	RDn, WDn, $\overline{\text{Sn}}$, RVC02, RVC36	I_{IH1}			20	μA	V_{CC}=5.25V, V_{IH}=2.7V
	STBC	I_{IH2}			40	μA	
	SIn, CIn	I_{IH3}			60	μA	
Input High Current		I_{IH}			1	mA	V_{CC}=5.25V, V_{IH}=5.5V
Output Short Current		I_{OS}	30		120	mA	V_{CC}=5.25V, V_O=0.5V
Power Supply Current		I_{CC}		190	300	mA	V_{CC}=5.25V
Input Clamp Voltage		V_{IC}			1.2	V	V_{CC}=4.75V, I_{IL}=18mA

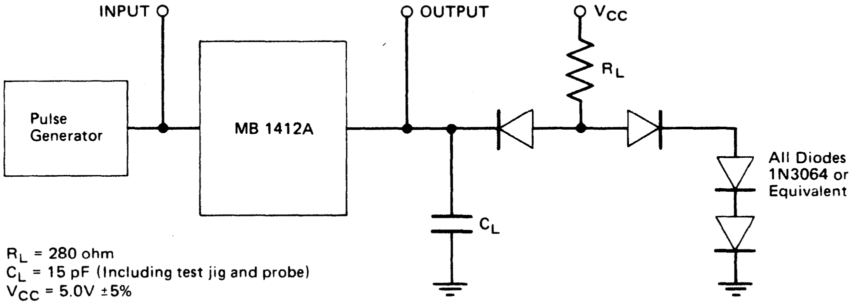
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
(RD1 ~ RD7) to (SO0 ~ SO2) *	t_{pd1}		14	19	ns
(RD0 ~ RD7) to SO3, SO4	t_{pd2}			25	ns
RD0 to SO5	t_{pd4}			17	ns
(RD0 ~ RD7) to (CO0 ~ CO5)	t_{pd3}			36	ns
(RD0 ~ RD7) to (D0 ~ D7)	t_{pd4}			18	ns
(SI0 ~ SI5) to (SO0 ~ SO5) *	t_{pd5}		4	9	ns
(CI0 ~CI5) to (CO0 ~ CO5) *	t_{pd6}		4	9	ns
(WD0 ~ WD7) to (CO0 ~ CO5) *	t_{pd7}		25	36	ns
(WD0 ~ WD7) to (D0 ~ D7)	t_{pd8}			18	ns
($\overline{\text{S0}}$ ~ $\overline{\text{S6}}$) to (CO0 ~ CO5)	t_{pd9}			22	ns
($\overline{\text{S0}}$ ~ $\overline{\text{S6}}$) to (D0 ~ D7) *	t_{pd10}		14	19	ns
($\overline{\text{S0}}$ ~ $\overline{\text{S6}}$) to $\overline{\text{RE1}}$	t_{pd11}			22	ns
($\overline{\text{S0}}$ ~ $\overline{\text{S6}}$) to $\overline{\text{RVC}}$	t_{pd12}			21	ns
RVC02 to (CO0 ~ CO3)	t_{pd13}			18	ns
RVC36 to (CO0 ~ CO3)	t_{pd14}			17	ns
STBC to (CO0 ~ CO5)	t_{pd15}			36	ns
STBC to (D0 ~ D7)	t_{pd16}			22	ns
STBC to $\overline{\text{RVC}}$	t_{pd17}			18	ns

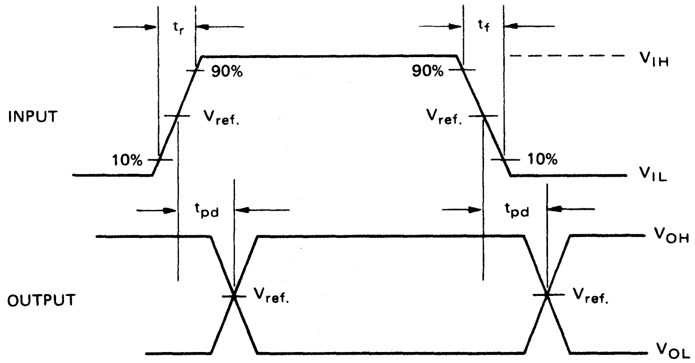
* Note: Critical path on a chip

Fig. 4 DELAY TIME MEASUREMENT CIRCUIT



R_L = 280 ohm
C_L = 15 pF (Including test jig and probe)
V_{CC} = 5.0V ±5%

Fig. 5 INPUT SIGNAL/OUTPUT SIGNAL TIMING



V_{IL} = 0V
V_{IH} = 3.0V
$t_r = t_f$ = 2.5 ns
PRR = 1MHz
$V_{ref.}$ = 1.3V

CRITICAL PATH TIMING

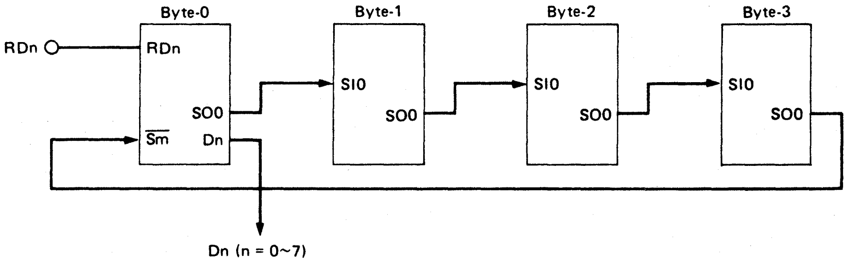
Critical timing paths for the MB 1412A are shown under AC Characteristics as indicated by the notation "Critical Path on Chip". In a typical, multi-chip ECC system application, system delay time would be measured from the RD input to the D output for processing of the complete data input. The equation is as follows, where ℓ is the number of bytes in the data input:

$$t_{pd}\,(RDn - Dn) = t_{pd}\,(RDn - SO0) + (\ell - 1) \times t_{pd}\,(SI0 - SO0) + t_{pd}\,(\overline{Sm} - Dn)$$

For a 4-byte system (see Figure 6), delay time from READ data (RD) to corrected data (D) is 40 nsec typical:

$$t_{pd}\,(RD - D)_4 = 14\text{ns} + (\,3 \times 4\text{ ns}) + 14\text{ ns} = 40\text{ nsec.}$$

Fig. 6 CRITICAL PATH TIMING (Data Correction)



THEORY AND APPLICATION OF ECC

In most any data processing system, binary bit errors are going to occur when blocks of data are moved from one location to another. As such errors are not uncommon and can lead to entirely bogus or meaningless results in routine programs, it has become requisite design discipline to include ECC (Error Checking and Correction) Circuitry in main memory control logic. The MB 1412A accomplishes this in a highly integrated form which allows ECC implementation with a minimal package count.

The MB 1412A will correct one-bit errors in every input data word, and flag the occurence of two-bit errors. One-bit error correction is considered adequate, as the probability of more than a one-bit error is quite low. As an example, consider a data word of 5-bits with the error possibility of .0001 (one in ten-thousand) per bit. The chances of an error occuring in a data word are:

no error	$P_0 = (1 - P)^5 = 0.9995$
one error	$P_1 = {}_5C_1 \cdot P\,(1 - P)^4 = 0.0005$
two errors	$P_2 = {}_5C_2 \cdot P^2\,(1 - P)^3 = 0.00000025$

Thus, one-bit detection and correction and two-bit detection only should provide adequate insurance, and satisfactory system performance. When a two-bit error occurs, of course, the program must be interrupted to prevent miscalculation.

In order to detect data bit errors, memory check-bits must be stored with the data words. For 1-bit error detection of a word of n-bits, assume the number of check-bits required is C_n. The number of possible bit combinations for no error is therefore 1 (all bits, both data bits and check-bits correct); and the number of possible bit combinations for a 1-bit error is: $n + C_n$.

The number of combinations made by check-bits is 2^{C_n}. To detect 1-bit errors a hundred percent, the following must be satisfied:

$$1 + (n + C_n) \leqslant 2^{C_n}.$$

This means, for example, that a 1-bit error in 16-bits of data can be detected by five additiônal check-bits. Following the same calculation, 1-bit errors in 32-bit data words require 6 check-bits, and 64-bit data words require 7 check bits. To detect 2-bit errors, one additional bit is required; e.g., 6 check-bits for a 16-bit word.

The MB 1412A is designed for use in a memory system configuration of either 2-bytes (16 data bits), 4-bytes (32 data bits), or 8-bytes (64 data bits). Simple external gating, as shown in Figures 7 and 8, is required in the error indication and reverse check-bit circuitry.

When data is first written into memory, the ECC system does not correct or detect errors. But it does generate the necessary check-bits (as a function of the number of bytes of data in the memory system configuration) which are stored in memory along with the data bits. The check-bit code conforms to the ECC system output of the modified Hamming code check-bit generator as shown in Figure 9. The check-bit generator takes the parity of all the data bits marked by an X in the rows of the input data bits.

When memory is read, both data bits and check-bits form inputs into the ECC system. Data bits are entered in parallel, one byte per ECC IC in the ECC system. The check-bits are entered into the first ECC IC in the chain, and additional ECC IC's as shown in the example in Figure 15.

These fetched check-bits are exclusive-ORed with newly generated check-bits created from the data input in order to generate a syndrome code for the fetched data as shown in Figure 9. From the syndrome code, the ECC system can determine if there is an error in the input data bits, as follows:

- If the syndrome code is all "0", there is no error.
- If one syndrome bit is "1", the corresponding check-bit is in error. As a result, $\overline{\text{RE1}}$ will go to "0" and $\overline{\text{RVC}}$ will go to "1" so that no correction will be made in the data bits.
- If more than one syndrome bit is "1", and the parity of all syndrome bits is even, a multiple error has occurred. No correction is made, and the program should be interrupted.
- If more than one syndrome bit is "1", and the parity of all syndrome bits is odd, a single error has occurred in the data bits. The binary location of the error in the input data bits can be determined by decoding of the syndrome code as shown in Figure 10.

In the event of multiple errors, no data correction is made; rather the event is flagged and system software should be interrupted. As a two-bit error without ECC would normally result in program execution errors, program interruption is presumed to be the only satisfactory outcome of the multiple error detection event.

When one error is detected in the fetched check-bits, the ECC system, in effect, generates a new set of check-bits (and "ignores" the fetched check-bits) with respect to processing the input data bits.

WRITE Mode:

A "1" input on STBC initiates the WRITE mode operation and tells the Data Selector (DS) to read data from the Write Data (WD) buffer (WD0–WD7 inputs). The $\overline{\text{RVC}}$ (Reverse Check Bit) and $\overline{\text{RE1}}$ (Read Error One) outputs of the Syndrome Decoder/Locator (SD) go high so that no error indication for the data is possible. Further, the function of the Check-bit Corrector (CC) is inhibited by feedback of the $\overline{\text{RVC}}$ signal (high state) to the RVC02 and $\overline{\text{RVC36}}$ inputs. Data correction can not occur because the $\overline{\text{RVC}}$ output is high.

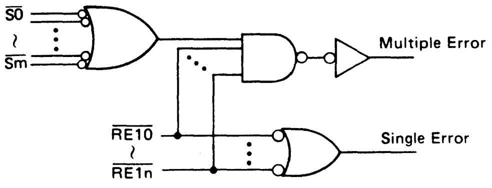
The Check-bit Generator (CG) will generate check-bit data from the WRITE data transferred from the Data Selector (DS) and output it on CO0–CO5 in accordance with the logic table shown in Figure 9. At the same time, the Data Corrector (DC) will transfer the WRITE data onto outputs D0–D7. Thus the WRITE data on D0–D7 can be stored in main memory along with the appropriate output check-bits corresponding to the data bits input into the ECC system.

READ Mode:
A "0" input on STBC indicates the READ mode operation and tells the Data Selector (DS) to transfer read data from inputs RD0—RD7 through the Read Data (RD) buffer to the Data Corrector (DC) and Check-bit Generator (CG). The Syndrome Generator (SG) will generate check-bits from the same data inputs and XOR (exclusive-OR) them with the data on SI0—SI5 (Syndrome Inputs). XORed data becomes the output on SO0—SO5 (Syndrome Output) according to the logic table shown in Figure 9. At the same time, the Check-bit Generator (CG) will generate check-bits from the input read data and will accept check-bit correction if the data from memory contains an error. Note that by performing syndrome generation and check-bit correction simultaneously, high speed operation is maintained.

A "0" on STBC also gates the Syndrome Decoder/Locator (SD) to decode syndrome inputs on $\overline{\text{S0}}$—$\overline{\text{S6}}$. When syndrome data is not all "0", both $\overline{\text{RVC}}$ (Reverse Check-Bit) and $\overline{\text{RE1}}$ (Read Error-One) go "0" (low) to indicate error detection. Logic tables are shown in Figure 10. The error bit position is indicated to the Data Corrector (DC), and the data output at D0—D7 is corrected.

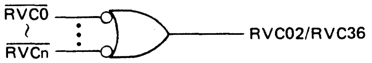
$\overline{\text{RVC}}$ is fedback to the RVC02 and RVC36 inputs. So when an error is detected ($\overline{\text{RVC}}$ = low), the input syndrome data from the Syndrome Buffer ($\overline{\text{S}}$) is gated into the Check-bit Corrector (CC). The check-bits are corrected in accordance with the logic table shown in Figure 9.

Fig. 7 ERROR INDICATION CIRCUIT



(m: Bit size of Syndrome-1)

Fig. 8 REVERSE CHECK-BIT CIRCUIT



(n: Byte size-1)

Fig. 9 LOGICAL DESCRIPTION OF SYNDROME GENERATION/DECODING AND CHECK-BIT GENERATION

Table 1 Syndrome Generation (See Note *)

SI						RD								XOR TREE	OUTPUT
0	1	2	3	4	5	0	1	2	3	4	5	6	7		
X							X		X		X		X	EVEN	SO0
	X							X	X			X	X	EVEN	SO1
		X								X	X	X	X	EVEN	SO2
			X			X	X	X	X	X	X	X	X	ODD	SO3
				X		X	X	X		X			X	ODD	SO4
					X	X								ODD	SO5

Table 2 Check-Bit Generation (See Note *)

CI						RD (STBC=0)/WD (STBC=1)								XOR TREE	MODIFICATION **	OUT-PUT
0	1	2	3	4	5	0	1	2	3	4	5	6	7			
X							X		X		X		X	ODD	⊕ RVC02·S0	CO0
	X							X	X			X	X	ODD	⊕ RVC02·S1	CO1
		X								X	X	X	X	ODD	⊕ RVC02·S2	CO2
			X			X	X	X	X	X	X	X	X	EVEN	⊕ RVC36·S3	CO3
				X		X	X	X		X			X	EVEN		CO4
					X	X								EVEN		CO5

Note:
* Inputs marked "X" are gated to the XOR-TREE.
** ⊕ indicates XOR.

Fig. 10 SYNDROME DECODING

For data

S							Error Indication / Error Location
0	1	2	3	4	5	6	
0	0	0	1	1	1	0	Data Bit 0
1	0	0	1	1	0	0	Data Bit 1
0	1	0	1	1	0	0	Data Bit 2
1	1	0	1	0	0	0	Data Bit 3
0	0	1	1	1	0	0	Data Bit 4
1	0	1	1	0	0	0	Data Bit 5
0	1	1	1	0	0	0	Data Bit 6
1	1	1	1	1	0	0	Data Bit 7

For check-bit

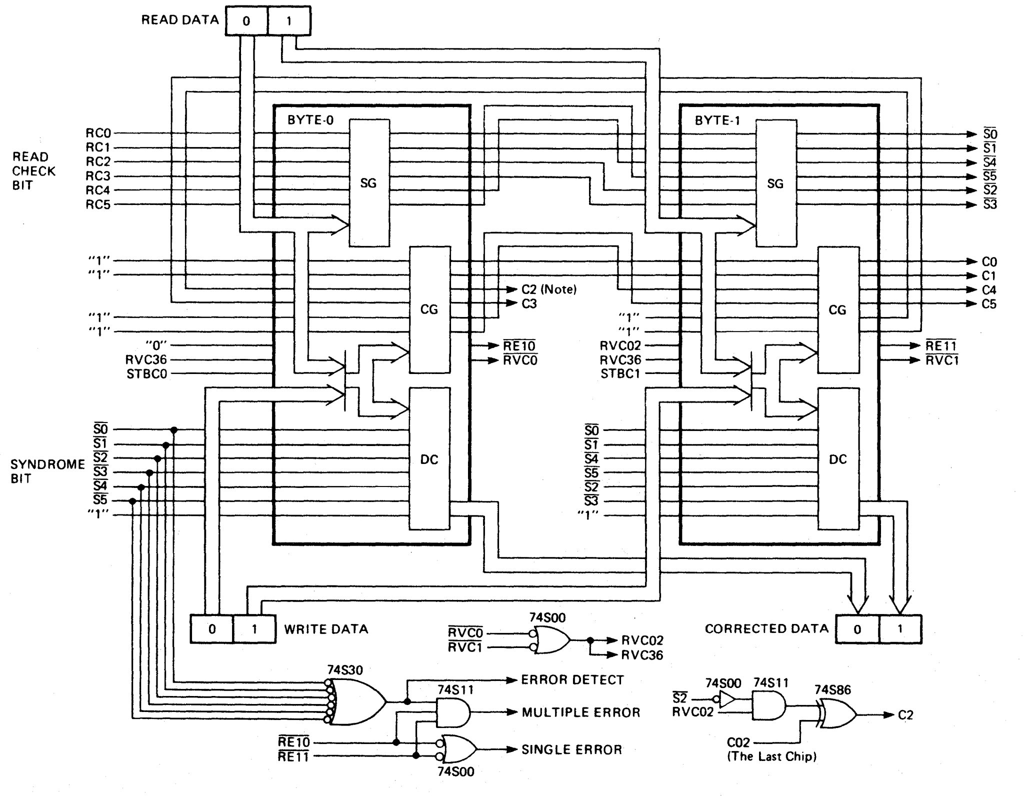
S							Error Indication / Error Location
0	1	2	3	4	5	6	
1	0	0	0	0	0	0	Check-Bit 0
0	1	0	0	0	0	0	Check-Bit 1
0	0	1	0	0	0	0	Check-Bit 2
0	0	0	1	0	0	0	Check Bit 3

EXAMPLE OF A 2-BYTE SYSTEM

Figure 11 is a block diagram of a 2-byte ECC system configuration, including the external gate requirements. Two MB 1412As are connected so that the bits indicated by an X in the Hamming code shown in Figure 12 are exclusive-ORed in the Check-Bit Generator. In the example, the 16-bit input data word is 00011100 01011101, and the check-bits generated in WRITE mode are 101000.

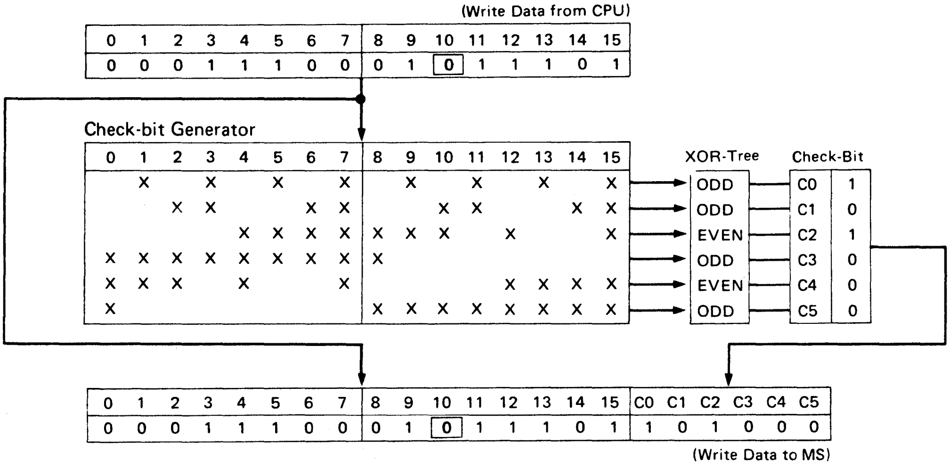
In the READ mode shown in Figure 13, we assume that bit 10 has been inverted (error). The data bits are gated to the exclusive-OR tree to regenerate check-bits (now 110001) which are exclusive-ORed with the original check-bits (101000). The syndrome bits (011001) are then decoded as shown which indicates an error on bit 10 of the input data. This is corrected by inverting (change "1" to "0").

Fig. 11 TWO-BYTE ERROR CHECKING AND CORRECTION SYSTEM



Note: When ECC system is used in "Partial Write Mode", C2 must be connected to the C02 input of the external reverse check bit circuit.

Fig. 12 WRITE OPERATION IN 2-BYTE ECC SYSTEM



(Write Data from CPU)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1	1	1	0	0	0	1	$\boxed{0}$	1	1	1	0	1

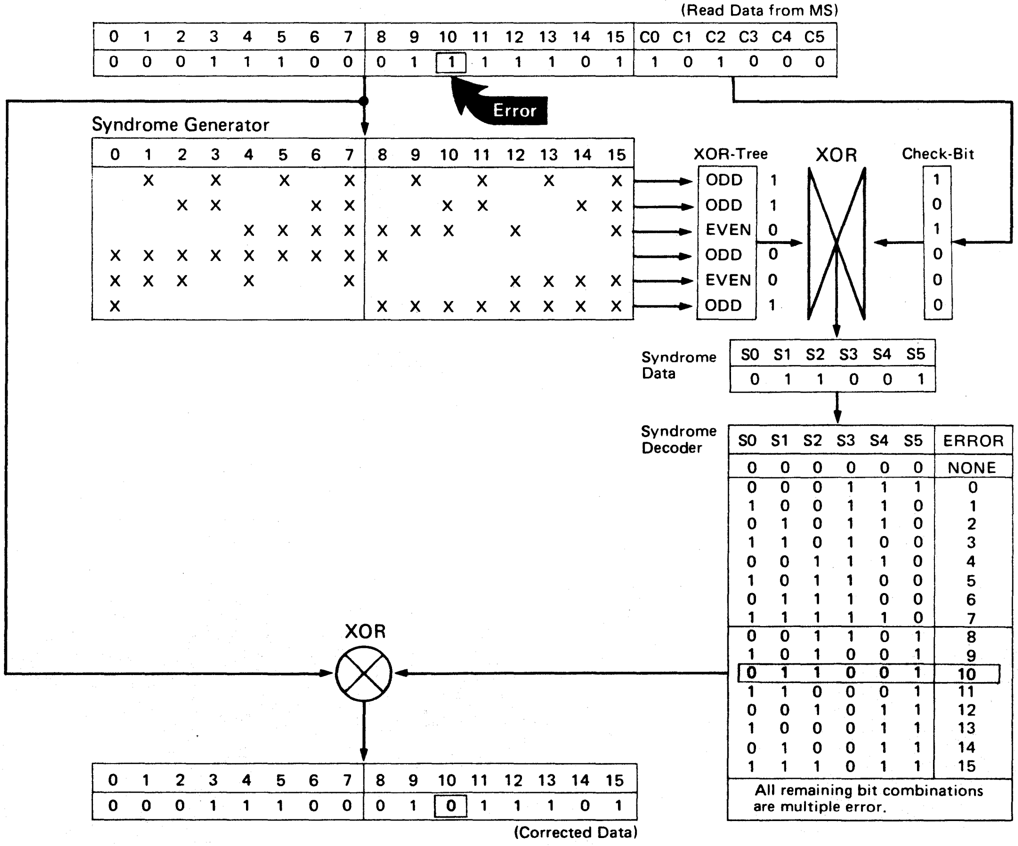
Check-bit Generator

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	XOR-Tree	Check-Bit	
	X		X		X		X		X		X		X		X	ODD	C0	1
		X	X			X	X			X	X			X	X	ODD	C1	0
				X	X	X	X	X	X	X		X			X	EVEN	C2	1
X	X	X	X	X	X	X	X	X								ODD	C3	0
X	X	X		X			X					X	X	X	X	EVEN	C4	0
X								X	X	X	X	X	X	X	X	ODD	C5	0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	C0	C1	C2	C3	C4	C5
0	0	0	1	1	1	0	0	0	1	$\boxed{0}$	1	1	1	0	1	1	0	1	0	0	0

(Write Data to MS)

Fig. 13 READ OPERATION IN 2-BYTE ECC SYSTEM



(Read Data from MS)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	C0	C1	C2	C3	C4	C5
0	0	0	1	1	1	0	0	0	1	$\boxed{1}$	1	1	1	0	1	1	0	1	0	0	0

Syndrome Generator

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	XOR-Tree		Check-Bit
	X		X		X		X		X		X		X		X	ODD	1	1
		X	X			X	X			X	X			X	X	ODD	1	0
				X	X	X	X	X	X	X		X			X	EVEN	0	1
X	X	X	X	X	X	X	X	X								ODD	0	0
X	X	X		X			X					X	X	X	X	EVEN	0	0
X								X	X	X	X	X	X	X	X	ODD	1	0

Syndrome Data

S0	S1	S2	S3	S4	S5
0	1	1	0	0	1

Syndrome Decoder

S0	S1	S2	S3	S4	S5	ERROR
0	0	0	0	0	0	NONE
0	0	0	1	1	1	0
1	0	0	1	1	0	1
0	1	0	1	1	0	2
1	1	0	1	0	0	3
0	0	1	1	1	0	4
1	0	1	1	0	0	5
0	1	1	1	0	0	6
1	1	1	1	1	0	7
0	0	1	1	0	1	8
1	0	1	0	0	1	9
0	1	1	0	0	1	10
1	1	0	0	0	1	11
0	0	1	0	1	1	12
1	0	0	0	1	1	13
0	1	0	0	1	1	14
1	1	1	0	1	1	15
All remaining bit combinations are multiple error.						

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1	1	1	0	0	0	1	$\boxed{0}$	1	1	1	0	1

(Corrected Data)

EXAMPLE OF A 4-BYTE SYSTEM

In a 4-Byte ECC system, four MB 1412A LSIs are connected in a cascaded manner as shown in Figure 14. The Hamming code depicted in Figure 15 is realized from the interconnection of the LSIs as shown. Data bits marked with an X in Figure 15 are gated to an exclusive-OR tree to generate check-bits. The WRITE mode is diagrammed in Figure 16, and READ mode is shown in Figure 17. Figure 18 diagrams a Partial WRITE operation on the 1st and 2nd bytes, with READ mode on the 3rd and 4th.

Fig. 14 FOUR-BYTE ERROR CHECKING AND CORRECTION SYSTEM

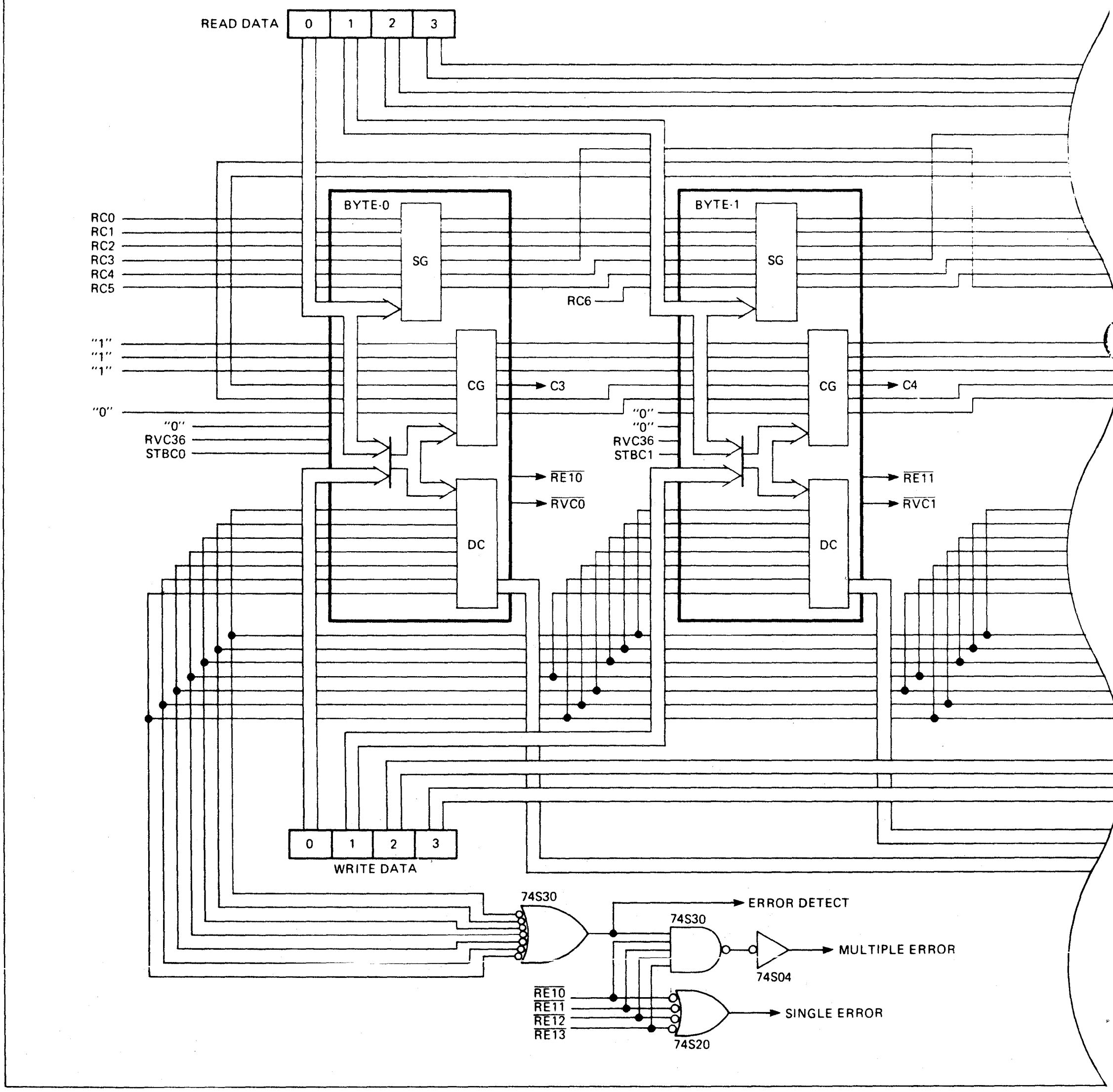


Fig. 15 FOUR-BYTE ECC CODE TABLE

Data Bits																																XOR-Tree	Check-Bit
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
	X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X	ODD	C0
		X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X	ODD	C1
				X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X	ODD	C2
X	X	X	X	X	X	X	X									X								X	X	X		X			X	EVEN	C3
X	X	X		X			X	X	X	X	X	X	X	X	X									X								EVEN	C4
X								X	X	X		X			X	X	X	X	X	X	X	X	X									EVEN	C5
								X								X	X	X		X			X	X	X	X	X	X	X	X	X	EVEN	C6

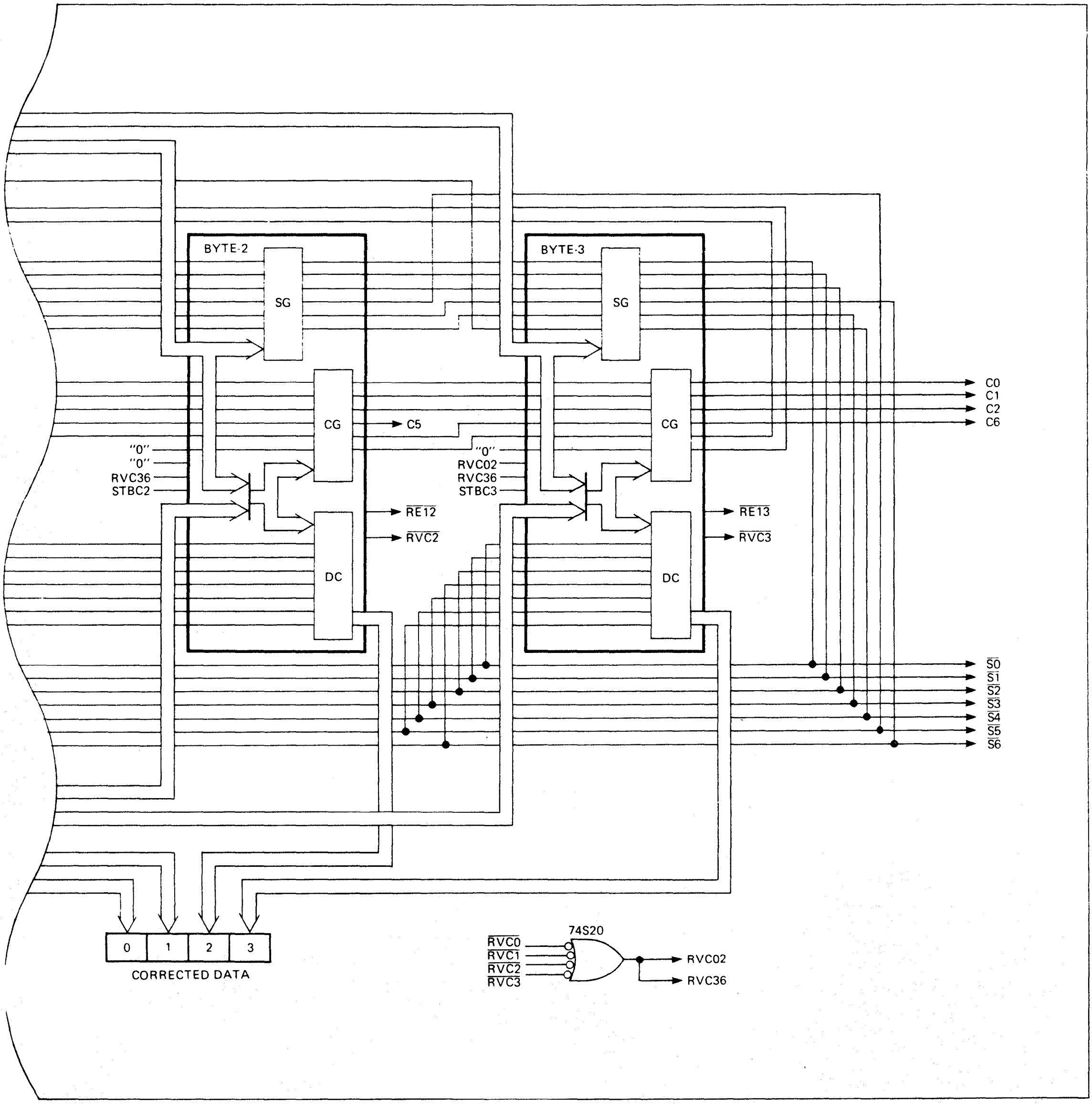
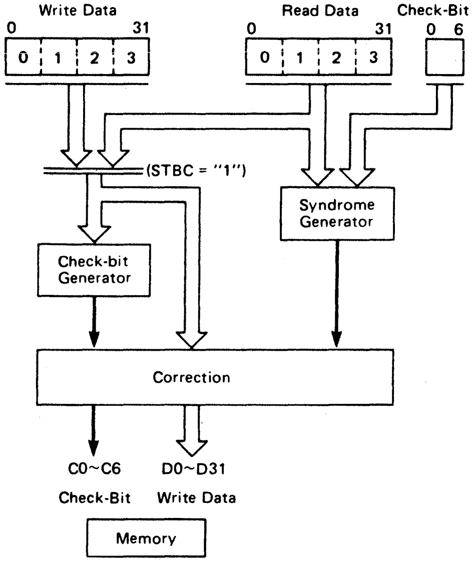
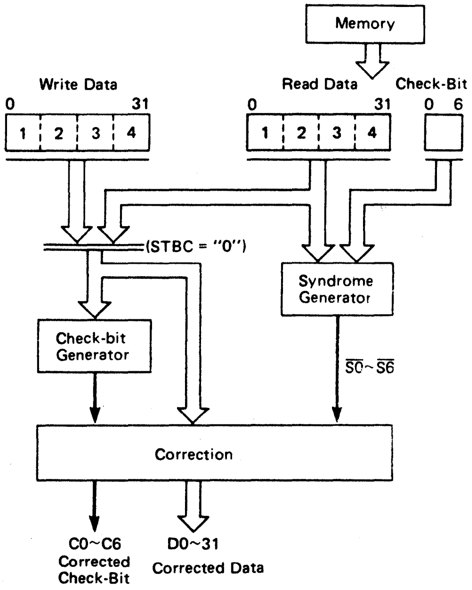


Fig. 16 WRITE OPERATION (4-BYTE)



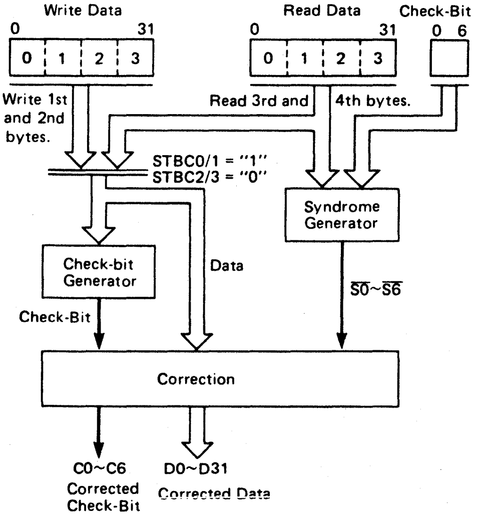
No correction is done on any byte data.

Fig. 17 READ OPERATION (4-BYTE)



One bit error in Read Data can be corrected.

Fig. 18 PARTIAL WRITE OPERATION (4-BYTE)



1. When one bit error is detected on 3rd and 4th byte data, Data and Check-bit can be corrected. (READ Data)
2. No correction is done on 1st and 2nd byte Data. (WRITE Data)
3. One bit error on check-bit need not be corrected.

EXAMPLE OF AN 8-BYTE SYSTEM

In a 8-Byte ECC system, eight MB 1412A LSIs are connected in a cascaded manner as shown in Figure 20. The Hamming code depicted in Figure 19 is realized from the interconnection of the LSIs as shown. Data bits marked with an X in Figure 19 are gated to an exclusive-OR tree to generate check-bits.

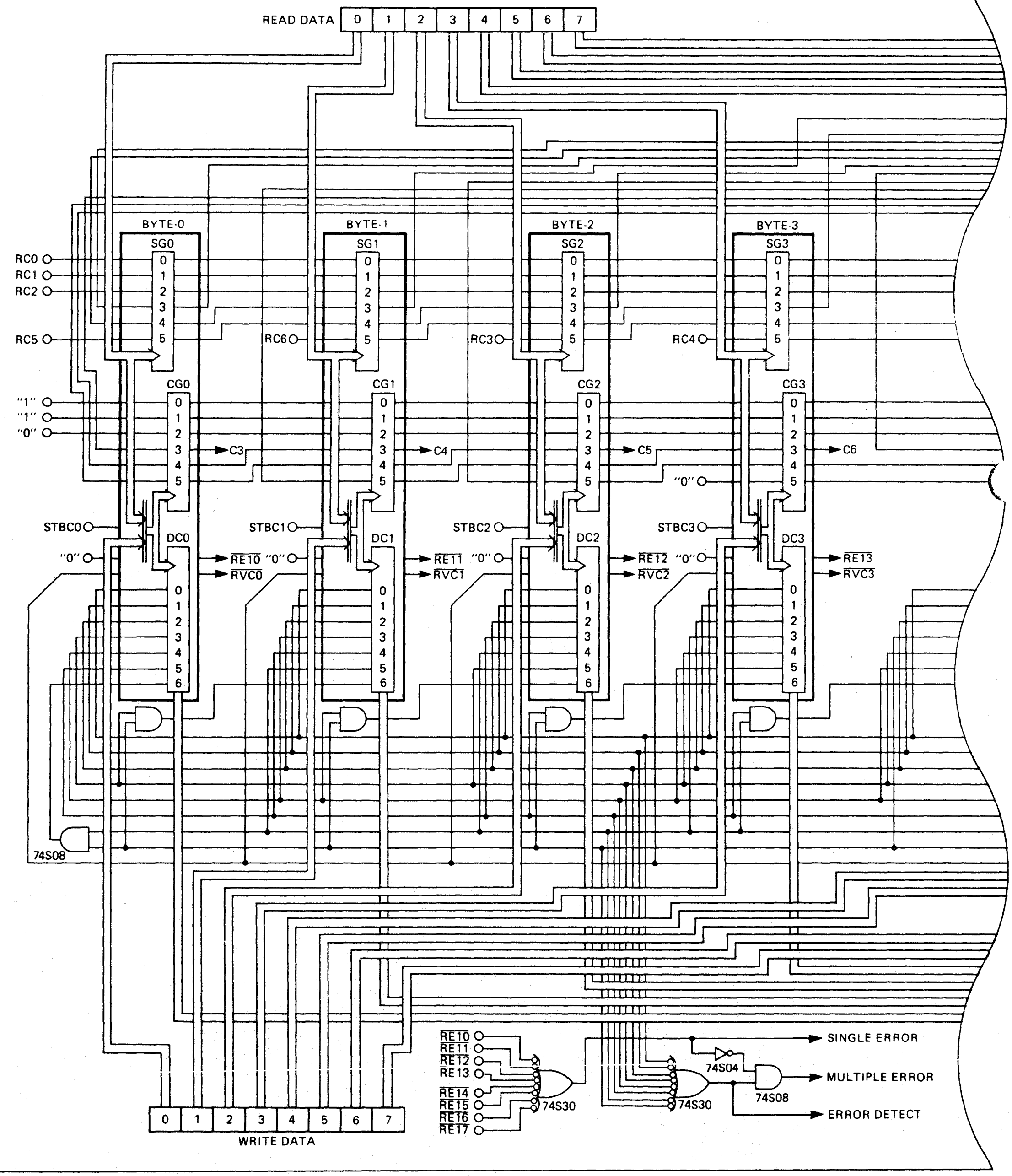
Fig. 19 EIGHT-BYTE ECC CODE TABLE

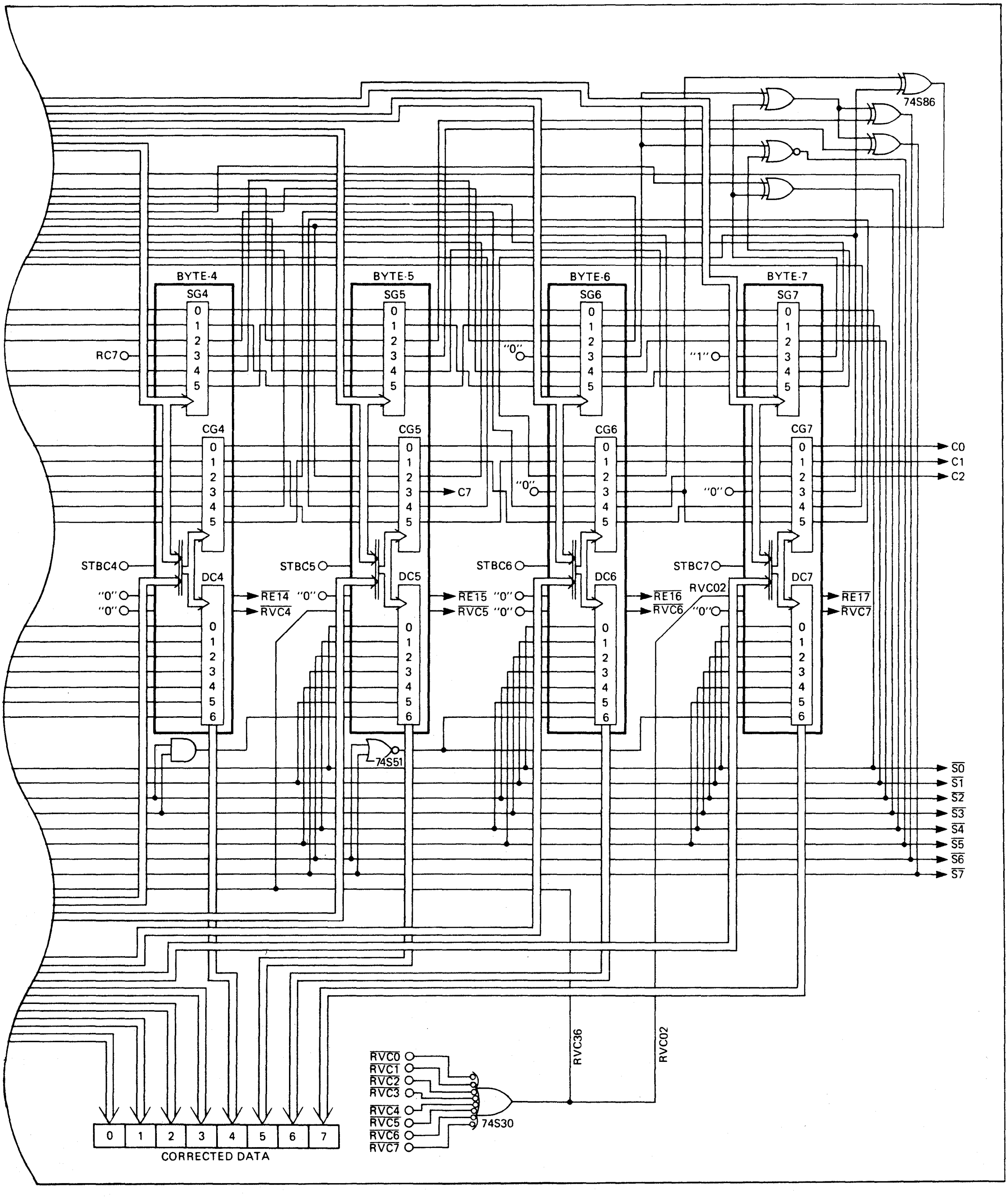
Byte-0								Byte-1								Byte-2							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	X		X		X		X		X		X		X		X		X		X		X		X
		X	X			X	X			X	X			X	X			X	X			X	X
				X	X	X	X					X	X	X	X					X	X	X	X
X	X	X	X	X	X	X	X									X							
X	X	X		X			X	X	X	X	X	X	X	X	X								
X								X	X	X		X			X	X	X	X	X	X	X	X	X
								X								X	X	X		X			X

Byte-3								Byte-4								Byte-5							
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
	X		X		X		X		X		X		X		X		X		X		X		X
		X	X			X	X			X	X			X	X	X							
				X	X	X	X					X	X	X	X								
X	X	X		X			X	X	X	X		X			X								
X								X										X	X			X	X
																X	X	X		X			X
X	X	X	X	X	X	X	X													X	X	X	X
								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Byte-6								Byte-7									
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	XOR-Tree	Check-Bit
	X		X		X		X		X		X		X		X	ODD	C0
		X	X			X	X			X	X			X	X	EVEN	C1
X	X	X		X			X					X	X	X	X	EVEN	C2
				X	X	X	X	X	X	X	X	X	X	X	X	ODD	C3
X								X	X	X		X			X	ODD	C4
X	X	X	X	X	X	X	X	X								EVEN	C5
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ODD	C6
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	EVEN	C7

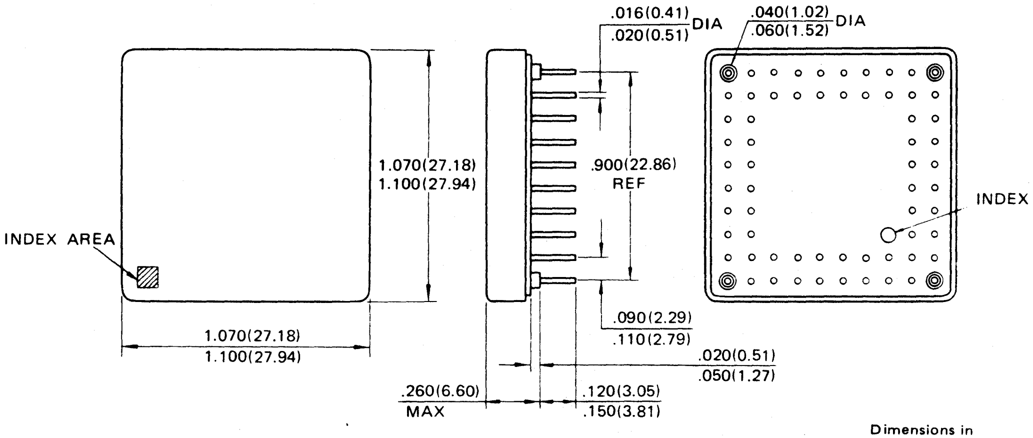
Fig. 20 EIGHT-BYTE ERROR CHECKING AND CORRECTION SYSTEM




74S86
BYTE-4
SG4
BYTE-5
SG5
BYTE-6
SG6
BYTE-7
SG7
0
1
2
3
4
5
RC7
"0"
"1"
CG4
CG5
CG6
CG7
C0
C1
C2
C7
"0"
STBC4
STBC5
STBC6
STBC7
DC4
DC5
DC6
DC7
RE14
RVC4
RE15
RVC5
RE16
RVC6
RE17
RVC7
RVC02
"0"
6
74S51
S0
S1
S2
S3
S4
S5
S6
S7
RVC36
RVC02
RVC0
RVC1
RVC2
RVC3
RVC4
RVC5
RVC6
RVC7
74S30
0
1
2
3
4
5
6
7
CORRECTED DATA

PACKAGE DIMENSIONS

64-LEAD CERAMIC (RESIN SEAL WITH METAL CAP) REPEATED QUAD IN-LINE PACKAGE
(CASE No.: PGA-64C-M01)



Dimensions in
inches (millimeters)

FUJITSU

16 BIT ERROR CHECKING & CORRECTION

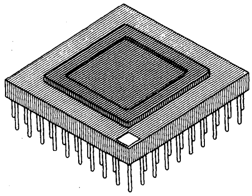
MB1426

April, 1986
Edition 1.0

DESCRIPTION

The MB1426 Error Checking and Correction (ECC) device is designed to enhance memory reliability in 16-bit systems. Using a modified Hamming Single-Error-Correction/Double-Error-Detection (SEC/DED) code, the ECC can find and correct all single-bit errors and detect all double-bit errors. The MB1426 is a TTL device fabricated in low-power Schottky and is housed in a 64-pin Pin-Grid-Array (PGA) package.

PRELIMINARY



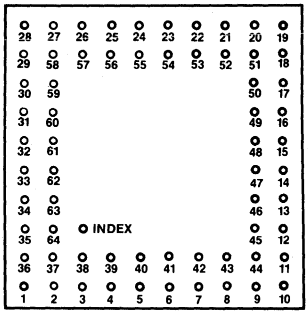
PGA-64C-A01

FEATURES

- Detects and corrects all single-bit errors
- Detects all double-bit errors
- On-chip latches for memory-read, check-bit, and syndrome data
- Separate busses for CPU and memory data
- Direct read/write by ECC-through mode
- Low power Schottky TTL for high performance
- Single +5V supply

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENTS



No.	I/O	Name	No.	I/O	Name	No.	I/O	Name	No.	I/O	Name
01	B	CD08	17	B	CB1	33	I	$\overline{\text{PWC0}}$	49	B	CB4
02	I	$\overline{\text{PWC1}}$	18	B	CB2	34	B	CD14	50	B	CB5
03	B	CD07	19	B	MD01	35	B	CD12	51	B	MD00
04	B	CD05	20	B	MD03	36	B	CD10	52	B	MD02
05	B	CD04	21	B	MD04	37	B	CD09	53	B	MD05
06	B	CD03	22	B	MD06	38	I	$\overline{\text{ECCTH}}$	54		GND
07	B	CD01	23	B	MD07	39	B	CD06	55	B	MD09
08	O	$\overline{\text{ERR}}$	24	B	MD08	40		GND	56	B	MD11
09	O	$\overline{\text{MERR}}$	25	B	MD10	41	B	CD02	57	B	MD13
10	T	STCB0	26	B	MD12	42	B	CD00	58	B	MD15
11	T	STCB1	27	B	MD14	43	I	ERREN	59	I	RCLK
12	T	STCB2	28	I	$\overline{\text{BSCNT}}$	44	I	$\overline{\text{EN}}$	60	O	$\overline{\text{PERR}}$
13	T	STCB3	29	B	P1	45	I	$\overline{\text{SLE}}$	61		VCC
14	T	STCB4	30	O	$\overline{\text{PERR1}}$	46	I	$\overline{\text{RST}}$	62	B	CD15
15	T	STCB5	31	B	P0	47		VCC	63	B	CD13
16	B	CB0	32	O	$\overline{\text{PERR0}}$	48	B	CB3	64	B	CD11

B: Bidirectional pin
I: Input pin
O: Output pin

PIN DESCRIPTIONS

Pin No.	Designator	Function
33 2	PWC0 PWC1	Partial Write Control/Read Write Control: These pins are used to control read write and they are also used to control the partial write. If both PWC0 and PWC1 = "H" the read operation is selected. If both PWC0 and PWC1 = "L" the word write operation is selected. In the partial write mode, if PWC0 = "L" and PWC1 = "H", the lower byte (MD0 to MD7) is written CPU data and the upper byte (MD8 to MD15) is written memory data which is latched during previous read operation. On the other hand, if PWC0 = "H" and PWC1 = "L" the lower byte is written memory data and the upper byte is written CPU data.
59	RCLK	Read Data Latch Clock: This pin is used to strobe the read data from memory and latch into the internal read data latch. The rising edge of RCLK strobes read data from MD00/MD15 and check bits from CB0/CB5. In the read cycle, data is strobed on the rising of RCLK.
45	SLE	Syndrome Latch Enable: This pin is used to latch syndrome bits into the internal syndrome latch. The falling edge of SLE strobes and latches the syndrome bits until RST = "L".
46	RST	Syndrome Latch Reset: This pin is used to reset syndrome latch. If RST = "L", the syndrome latch is reset and the latch is enabled to accept next string of syndrome bits.
43	ERREN	Error Enable: This pin is used to enable ERR and MERR outputs. If ERREN = "L", ERR and MERR are set "H" and disabled.
44	EN	Syndrome Output Enable: This pin is used to enable syndrome outputs (STCB0 and STCB5). If EN = "L", STCB0/STCB5 are enabled. If EN = "H", STCB0/STCB5 are disabled and in the high-impedance state.
38	ECCTH	ECC Through: This pin is used to enable the ECC-through mode. If ECCTH = "L", ECC-through mode is enabled and the read or write cycle is executed without regard to the ECC function. When ECC is utilized, the ECCTH pin must be "H".
28	BSCNT	Bus Control: This pin is used to control the operating mode of data pins CD00/CD15 and MD00/MD15, also to disable PERR0, PERR1 and PERR. If BSCNT = "L" all data pins are in the input mode and PERR0, PERR1 and PERR are disabled (set "H"). If BSCNT = "H", the operating mode of these data pins is controlled by the states of PWC0, and PWC1, and PERR0, PERR1 and PERR are enabled corresponding the the state of PWC0 and PWC1.
42 7 41 6	CD00 CD01 CD02 CD03	CPU Data: These pins have a common I/O capability and are connected to the CPU data bus. In the write cycle, these pins are in the input mode, that is, the CPU data is input to these pins and

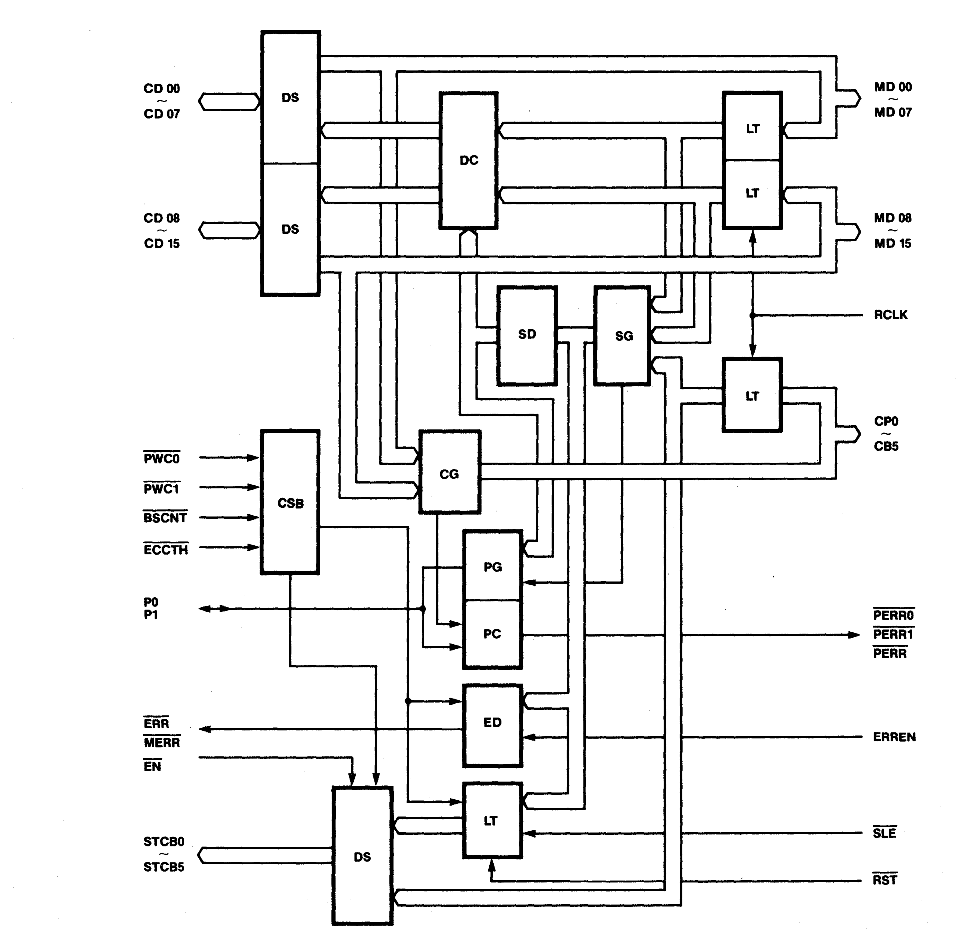
PIN DESCRIPTIONS (continued)

Pin No.	Designator	Function
5 4 39 3 1 37 36 64 35 63 34 62	CD04 CD05 CD06 CD07 CD08 CD09 CD10 CD11 CD12 CD13 CD14 CD15	output to memory through MD00/MD15. In a read cycle, these pins are in the output mode, that is, memory data from MD00/MD15 is output to the CPU via these pins.
51 19 52 20 21 53 22 23 24 55 25 56 16 57 27 58	MD00 MD01 MD02 MD03 MD04 MD05 MD06 MD07 MD08 MD09 MD10 MD11 MD12 MD13 MD14 MD15	Memory Data: These pins have a common I/O capability and they are connected to the memory data bus. In a write cycle, these pins are in the output mode, that is, CPU data from CD00/CD15 is output to memory through these pins. In a read cycle, these pins are in the input mode, that is, memory data is input to these pins and output through CD00/CD15.
31 29	P0 P1	Parity Bit: These pins have a common I/O capability and P0 and P1 correspond, respectively, to the lower byte and the upper byte. The parity bit from the CPU should be odd parity.
16 17 18 48 49 50	CB0 CB1 CB2 CB3 CB4 CB5	Check Bit: These pins have a common I/O capability and are connected to the check bit memory I/O line. In a write cycle, check bit data is generated by the check bit generator using CPU data; the check-bit pattern is output to check bit memory, that is, during a write cycle, these pins operate in the output mode. In a read cycle, the check-bit pattern from memory is input to these pins, that is, during a read cycle, these pins operate in the input mode.
10 11 12 13 14 15	STCB0 STCB1 STCB2 STCB3 STCB4 STCB5	Syndrome-Through Check Bit: These pins output the syndrome bits when read or partial write is selected. These outputs are used to analyze an error bit in the data word (CD00/CD15) and in the check bits (CB0/CB5). In the ECC-through mode, these pins output the check bits from memory.
8	$\overline{\text{ERR}}$	Error: This pin outputs the error flag when any single- or multiple-bit error is detected.

PIN DESCRIPTIONS (continued)

Pin No.	Designator	Function
9	$\overline{\text{MERR}}$	Multiple Error: This pin outputs the multiple error flag when a multiple-bit error is detected.
32 30 60	$\overline{\text{PERR0}}$ $\overline{\text{PERR1}}$ $\overline{\text{PERR}}$	Parity Error: These pins output a parity error flag when parity error occurs on CPU data. If $\overline{\text{PERR0}}$ = "L", a parity error on CD00/CD07 and P0 occurs. If $\overline{\text{PERR1}}$ = "L", a parity error on CD8/CD15 and P1 occurs. $\overline{\text{PERR}} = \overline{\text{PERR0}} \cdot \overline{\text{PERR1}}$.

BLOCK DIAGRAM



DS: Data Selector
DC: Data Corrector
LT : Latch
ED: Error Detector
SD: Syndrome Decoder
SG: Syndrome Generator
CSB: Control Signal Buffer
CG: Check Bit Generator
PG: Parity Generator
PC: Parity Checker

ANALYSIS OF BLOCK DIAGRAM

DS (Data Selector): Selects memory-read or memory-write data.

DC (Data Corrector): Corrects a single-bit error by using syndrome decoder.

LT (Latches): Latches memory-read, check-bit, and syndrome data.

ED (Error Detector): Detects single-bit or double-bit errors of memory-read data (MD00/MD15 and CB0/CB5). Single-bit or double-bit errors are determined, respectively, by the states of $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$.

SG (Syndrome Generator): Generates a syndrome-bit pattern to check memory-read data.

SD (Syndrome Decoder): Decodes syndrome-bit pattern of Syndrome Generator. When a single-bit error is detected, locates error bit and inverts the parity bit.

CSB (Control Signal Buffer): Buffers all control signals.

CG (Check Bit Generator): Generates check bit for checking memory-write data.

PG (Parity Generator): Generates odd parity bit for bus data.

PC (Parity Checker): Checks odd parity bit for bus data.

SDS (Syndrome Data Selector): Selects syndrome data or memory-check bit.

FUNCTIONAL DESCRIPTION

The error-detecting and error-correcting capabilities of the MB1426 ECC provides the user with a high order of confidence in memory reliability. Using a modified Hamming SEC/DED code, the ECC is able to detect and correct all single-bit errors and to detect all double-bit errors, even those containing consecutive strings of 0s and 1s. The detect/correct cycle for single-bit errors occurs without interrupting the CPU. Error flags notify the user when an error is detected.

The MB1426 has on-chip latches for memory-read, check-bit, and syndrome data; latching of the memory data allows the user to execute a partial (byte) write. To further enhance transmission reliability, a parity generator and checker is available to the user. A brief description of the read, write, and partial-write capabilities are described in subsequent paragraphs; for a detailed analysis of operating principles, refer to the Functional Truth Tables.

Read Cycle

The read cycle is executed by setting $\overline{\text{BSCNT}}$, $\overline{\text{PWC0}}$, and $\overline{\text{PWC1}}$ to the High state. The data and check bits from memory are read out and latched on the rising edge of RCLK; the latched data is sent to the syndrome generator and data corrector. The syndrome bit pattern is generated and decoded by the syndrome decoder; the decoded results are then sent to the data corrector.

If a single-bit error is detected, the $\overline{\text{ERR}}$ flag is raised and the error is corrected by the data corrector; the corrected data is output to CD00/CD15. When a single-bit error is detected and $\overline{\text{SLE}}$ is driven Low, the falling edge triggers the syndrome latches; this latched data is output to STCB0/STCB5 when $\overline{\text{EN}}$ is driven Low. Because data is held in the syndrome latches until $\overline{\text{RST}}$ is driven Low, "$\overline{\text{RST}}$ = L" should be executed before the syndrome data is used to identify the error-bit location.

If multiple-bit errors or a bit string (0s or 1s) error is detected, both $\overline{\text{ERR}}$ and $\overline{\text{MERR}}$ flags are raised and the latched memory data is output to CD00/CD15. For these cases, the data correction cycle is not executed.

In the read cycle, odd parity bits for bytes MD00/MD07 and MD08/MD15, respectively, are output to P0 and P1.

Write Cycle

Write capabilities of the MB1426 include both word write and partial (byte) write; either operation can be selected by setting $\overline{\text{PWC0}}$ and $\overline{\text{PWC1}}$ to the proper states—see Truth Tables that follow. If the CPU is capable of parity coding, the parity bits of P0 and P1 are utilized and, in both the word and paritial-byte write modes, the parity bits are checked.

The word write mode is executed by setting both $\overline{\text{PWC0}}$ and $\overline{\text{PWC1}}$ to the Low state. In the word-write mode, CPU data from CD00/CD15 is transferred to the check-bit generator and to MD00/MD15. Data appearing at MD00/MD15 is output and written into memory. The check-bit generator uses the CPU data to generate the check bits and these are output to CB0/CB5. The CPU and check-bit data are written into memory during the same write cycle.

The partial write mode is executed by setting either $\overline{\text{PWC0}}$ or $\overline{\text{PWC1}}$ to the Low state. If $\overline{\text{PWC0}}$ is Low and $\overline{\text{PWC1}}$ is High, the partial write is performed on byte CD00/CD07; in reverse states, byte CD08/CD15 is affected. Before a partial write is executed, the memory and check-bit data must be latched by setting $\overline{\text{BBSCNT}}$ to the Low state; this action puts CD00/CD15, MD00/MD15, P0, and P1 in the input mode and avoids data output to the CPU and memory.

The 8-bits of CPU data to be written to memory and the data to be read from memory are sent to the check-bit generator and to MD00/MD15; the data on MD00/MD15 is written into memory. Check bits are generated from 8-bits of CPU data and 8-bits of memory data and the check bits are then output to CB0/CB5. The partial write operation can be summarized as follows:

- Set $\overline{\text{BBSCNT}}$ Low and latch the 16-bit memory data and 6 check bits by executing a read cycle.
- Set either $\overline{\text{PWC0}}$ or $\overline{\text{PWC1}}$ Low and execute a write cycle. (In this case, BSCNT should be High to change MD00/MD15 from the input to the output mode.)
- Check bits are generated by 8 bits of CPU data and 8 bits of memory data.

FUNCTIONAL TRUTH TABLES

CPU Bus/Memory Bus Control

$\overline{\text{BSCNT}}$	$\overline{\text{PWC0}}$	$\overline{\text{PWC1}}$	CD00 to CD07, P0	CD08 to CD15, P1	MD00 to MD07	MD08 to MD15	Function
H	H	H	Output	Output	Input	Input	Read
	L	H	Input	Input	Output[1]	Output[2]	Partial Write
	H	L	Input	Input	Output[2]	Output[1]	
	L	L	Input	Input	Output	Output	Write
L	X	X	Input	Input	Input	Input	No function

Notes:
1. The CPU data is written into memory.
2. Memory data from previous read cycle is written into memory.

Syndrome Output Control

$\overline{\text{ECCTH}}$	$\overline{\text{PWC0}}$	$\overline{\text{PWC1}}$	$\overline{\text{EN}}$	CB0 to CB5	STCB0 to STCB5	Function
H	H	H	L	Input	Syndrome	Read
	L	H		Output	Syndrome	Partial Write
	H	L		Output		
	L	L		Output		Write
L	X	X		Input	Check Bit	ECC-Through
X	X	X	H		High-Z	

Hamming Code

Check Bit	CPU Data																Function
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
CB0		X		X		X		X		X		X		X		X	Odd
CB1			X	X			X	X			X	X			X	X	Odd
CB2					X	X	X	X	X	X	X		X			X	Even
CB3	X	X	X	X	X	X	X	X	X								Odd
CB4	X	X	X		X			X					X	X	X	X	Even
CB5	X								X	X	X	X	X	X	X	X	Odd

FUNCTIONAL TRUTH TABLES (continued)

Check Bit Generation

CB0 = $\overline{\text{CD01 + CD03 + CD05 + CD07 + CD09 + CD11 + CD13 + CD15}}$

CB1 = $\overline{\text{CD02 + CD03 + CD06 + CD07 + CD10 + CD11 + CD14 + CD15}}$

CB2 = CD04 + CD05 + CD06 + CD07 + CD08 + CD09 + CD10 + CD12 + CD15

CB3 = $\overline{\text{CD00 + CD01 + CD02 + CD03 + CD04 + CD05 + CD06 + CD07 + CD08}}$

CB4 = CD00 + CD01 + CD02 + CD04 + CD07 + CD12 + CD13 + CD14 + CD15

CB5 = $\overline{\text{CD00 + CD08 + CD09 + CD10 + CD11 + CD12 + CD13 + CD14 + CD15}}$

Syndrome Decode

Syndrome (STCB)	Error Bit																						No Error
	Memory Bus Data (MD)																Check Bit (CB)						
	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	0	1	2	3	4	5	
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	0	0	0	0
2	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0
3	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0
4	1	1	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0
5	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0

Error Detection and Correction

$\overline{\text{ERR}}$	$\overline{\text{MERR}}$	Message	Detect	Correct
H	H	No Error	—	—
L	H	Single Bit Error	Yes	Yes
L	L	Multiple Bit Error	Yes	No

Error Flag Control

ERREN	$\overline{\text{ECCTH}}$	$\overline{\text{PWC0}}$	$\overline{\text{PWC1}}$	$\overline{\text{ERR}}$ $\overline{\text{MERR}}$
0	X	X	X	disable
X	0	X	X	
1	1	0	0	
1	1	0	1	enable
		1	0	
		1	1	

Parity Error Flag Control

$\overline{\text{BSCNT}}$	$\overline{\text{PWC0}}$	$\overline{\text{PWC1}}$	$\overline{\text{PERR0}}$	$\overline{\text{PERR1}}$	$\overline{\text{PERR}}$
H	H	H	H	H	H
	L	H	enable	H	enable
	H	L	H	enable	
	L	L	enable		
L	X	X	H	H	H

H: Disable state

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_I	-0.5 to 5.5	V
Output Voltage	V_O	-0.5 to 5.5	V
Operating Temperature	T_{OP}	-25 to 85	°C
Storage Temperature	T_{STG}	-55 to 125	°C

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output High Current	I_{OH}			-3.3	mA
Output Low Current	I_{OL}			10	mA
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Conditions
			Min	Typ	Max		
Supply Current		I_{CC}		240	400	mA	V_{CC} = 5.5V
Input Low Current	Except for $\overline{\text{PWC0}}$, $\overline{\text{PWC1}}$, $\overline{\text{ECCTH}}$	I_{IL}			-200	μA	V_{CC} = 5.5V, V_{IN} = 0.5V
	$\overline{\text{PWC0}}$, $\overline{\text{PWC1}}$, $\overline{\text{ECCTH}}$				-400		
Input High Current		I_{IH1}			20	μA	V_{CC} = 5.5V, V_{IN} = 2.4V
		I_{IH2}			100		V_{CC} = 5.5V, V_{IN} = 5.5V
Input Clamp Voltage		V_{IC}			-1.5	V	V_{CC} = 4.5V, I_I = -18mA
Output Low Voltage		V_{OL}			0.5	V	V_{CC} = 4.5V, I_{OL} = 10mA
Output High Voltage		V_{OH}	2.4			V	V_{CC} = 4.5V, I_{OH} = -3.3mA
Output Leakage Current (High-Z)		I_{OZ}	-100		100	μA	V_{CC} = 5.5V, V_I = 0.5V/2.4V
Output Short Circuit Current		I_{OS}		-60		mA	V_{CC} = 5.5V, V_O = 0V
Input Low Voltage		V_{IL}			0.8	V	
Input High Voltage		V_{IH}	2.0			V	

AC CHARACTERISTICS (continued)

(Recommended operating conditions and AC test conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay Time from RCLK to CD, P0, P1	t_{CKCD}		35	57	ns
Delay Time from RCLK to $\overline{\text{ERR}}$	t_{CKER}		22	37	ns
Delay Time from RCLK to $\overline{\text{MERR}}$	t_{CKMER}		25	42	ns
Delay Time from ERREN to $\overline{\text{ERR}}$, $\overline{\text{MERR}}$	t_{EREN}		11	21	ns
MD Set Up Time referenced to RCLK	t_{MDCKS}	15			ns
MD Hold Time referenced to RCLK	t_{MDCKH}	10			ns
CB Set Up Time referenced to RCLK	t_{CBCKS}	15			ns
CB Hold Time referenced to RCLK	t_{CBCKH}	10			ns
Disable Time of MD from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$	t_{MDZD}		15	26	ns
Disable Time of CB from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$	t_{CBZD}		15	26	ns
Enable Time of CD, P0, P1 from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$	t_{CDZE}		22	36	ns
Delay Time from CD to MD	t_{CDMD}		16	27	ns
Delay Time from CD to CB	t_{CDCB}		21	34	ns
Delay Time from CD to $\overline{\text{PERR0}}$/$\overline{\text{PERR1}}$	t_{CDPEN}		22	35	ns
Delay Time from CD to $\overline{\text{PERR}}$	t_{CDPER}		23	38	ns
Delay Time from P0/P1 to $\overline{\text{PERR0}}$/$\overline{\text{PERR1}}$	t_{PPEN}		12	22	ns
Delay Time from P0/P1 to $\overline{\text{PERR}}$	t_{PPER}		14	26	ns
Enable Time of MD from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$	t_{MDZE}		20	32	ns
Enable Time of CD from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$	t_{CBZE}		20	32	ns
Disable Time of CD, P0, P1 from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$	t_{CDZD}		15	26	ns
Delay Time from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$ to $\overline{\text{PERR0}}$, $\overline{\text{PERR1}}$	t_{PWPEN}		10	18	ns
Delay Time from $\overline{\text{PWC0}}$/$\overline{\text{PWC1}}$ to $\overline{\text{PERR}}$	t_{PWPER}		12	22	ns
Enable Time of MD from $\overline{\text{BSCNT}}$	t_{BCMDZE}		20	35	ns
Delay Time from $\overline{\text{SLE}}$ to STCB	t_{SLEST}[1]		23	37	ns
Enable Time of STCB from $\overline{\text{EN}}$	t_{STZE}[1]		15	24	ns
RCLK Set Up Time referenced to $\overline{\text{SLE}}$	t_{SSL}[1]	44			ns
Delay Time from MD to CD	t_{MDCDTH}[2]		21	34	ns
Delay Time from MD to P0, P1	t_{MDPTH}[2]		28	48	ns
Delay Time from CB to STCB	t_{CBSTTH}[2]		18	30	ns
RCLK Set Up Time referenced to $\overline{\text{PWC0}}$, $\overline{\text{PWC1}}$	t_{CKS}[3]	57			ns
$\overline{\text{PWC0}}$, $\overline{\text{PWC1}}$ Set Up Time referenced to $\overline{\text{BSCNT}}$	t_{SBC}[3]	10			ns
Delay Time from PWC0/PWC1 to CD	t_{SCD}[3]		15	26	ns

AC CHARACTERISTICS (continued)

(Recommended operating conditions and AC test conditions unless otherwise noted.)

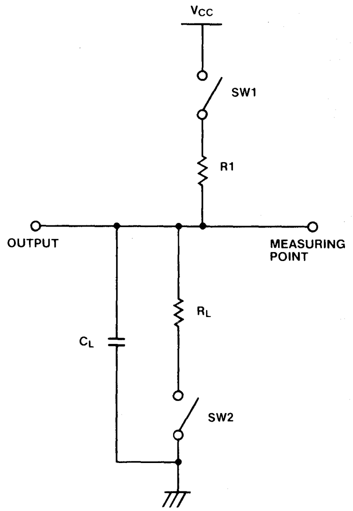
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RCLK Pulse Width	t_{WCK}	20			ns
RST Pulse Width	t_{WRST}	20			ns
SLE Pulse Width	WSLE	20			ns

Notes:

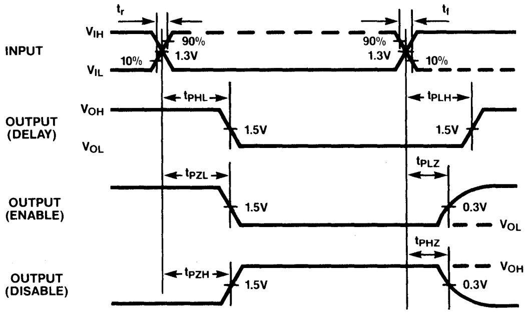
1. Syndrome Latch
2. ECC-Through Mode
3. Partial Write Mode

AC TEST CONDITONS

Output Load:



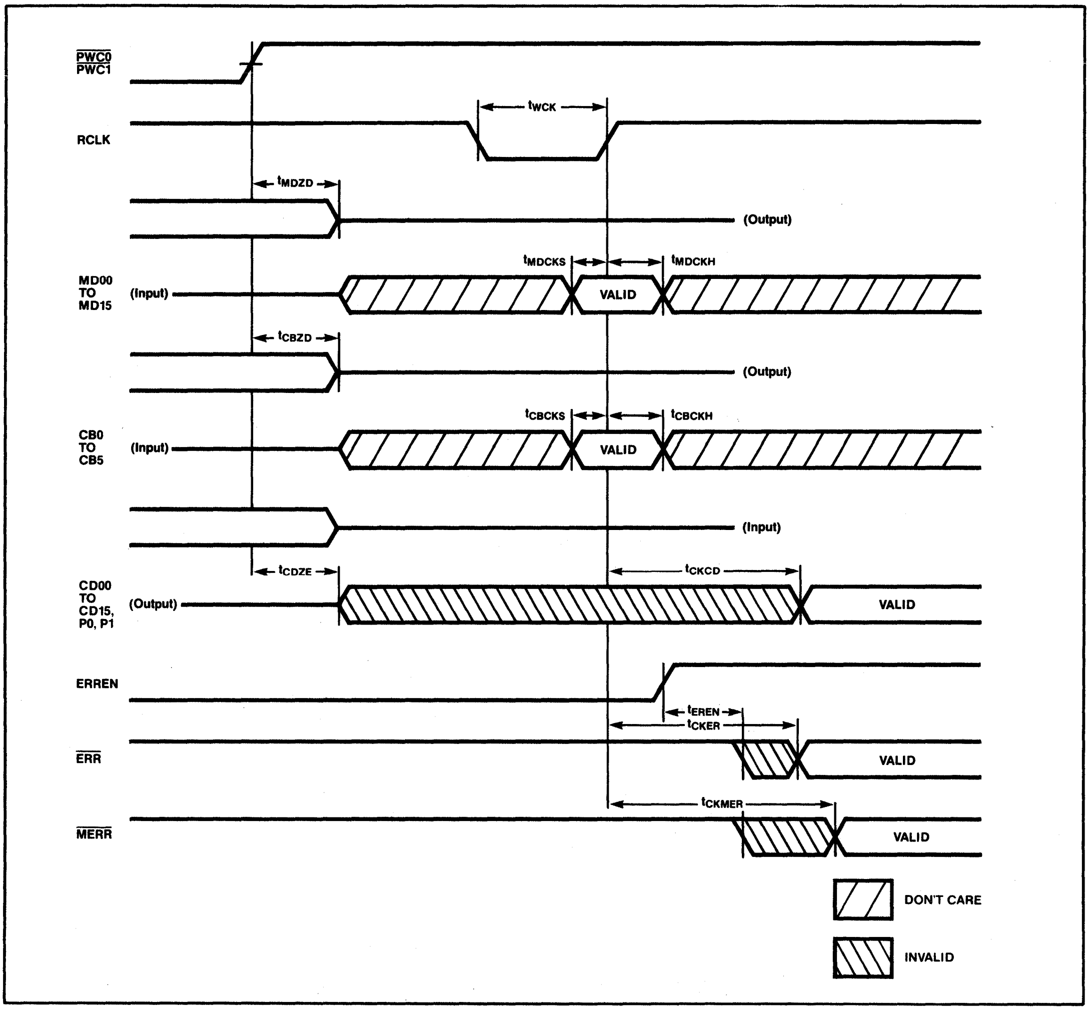
Timing Waveform:



V_{IH} = 3V, V_{IL} = 0V, tr = 10ns, tf = 5ns

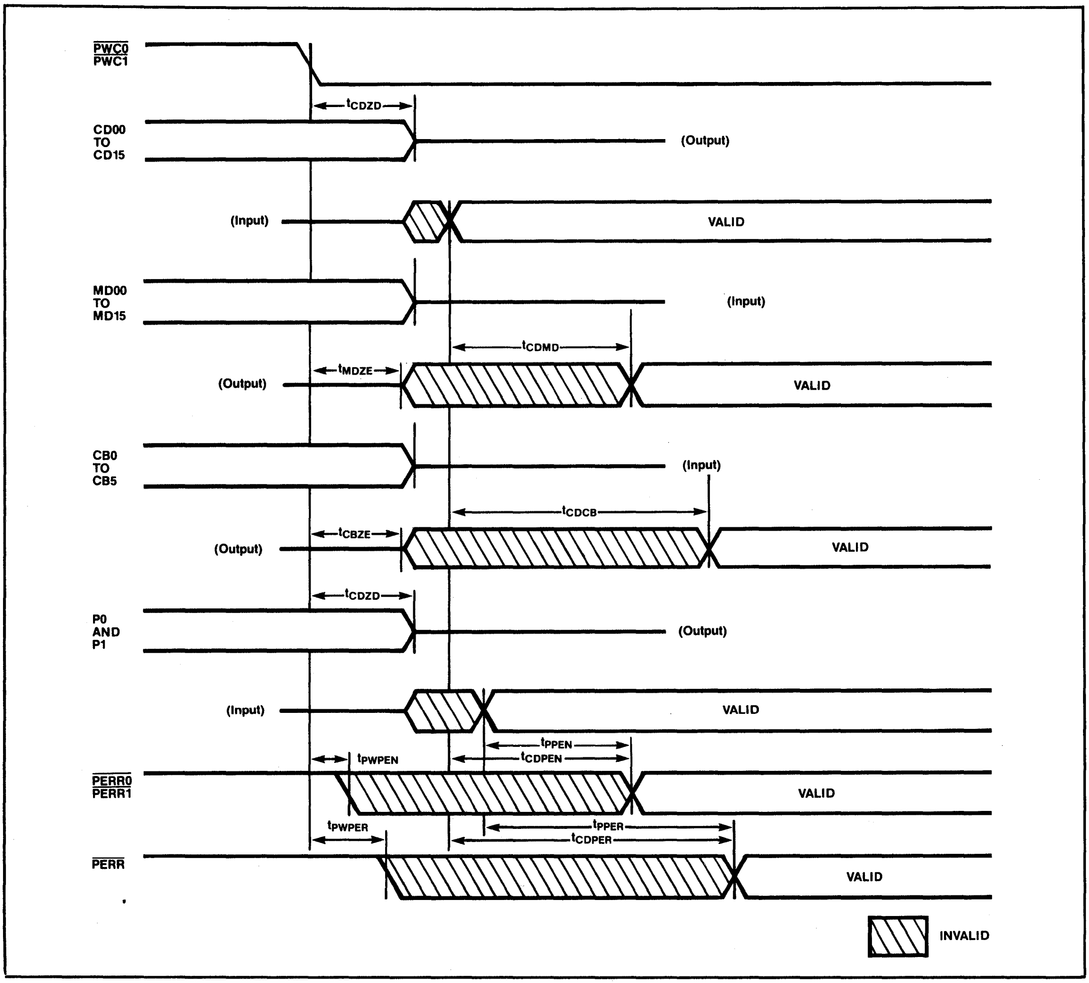
Parameter	Symbol	RL(Ω)	R1(Ω)	CL(pF)	SW1	SW2
Delay Time	t_{PLH} t_{PHL}	1.0K	—	50	Off	On
Enable Time	t_{PLZ} t_{PHZ}	1.0K	0.5K	5	On Off	On On
Disable Time	t_{PZL} t_{PZH}	1.0K	0.5K	50	On Off	On On

TIMING DIAGRAMS
Read Mode



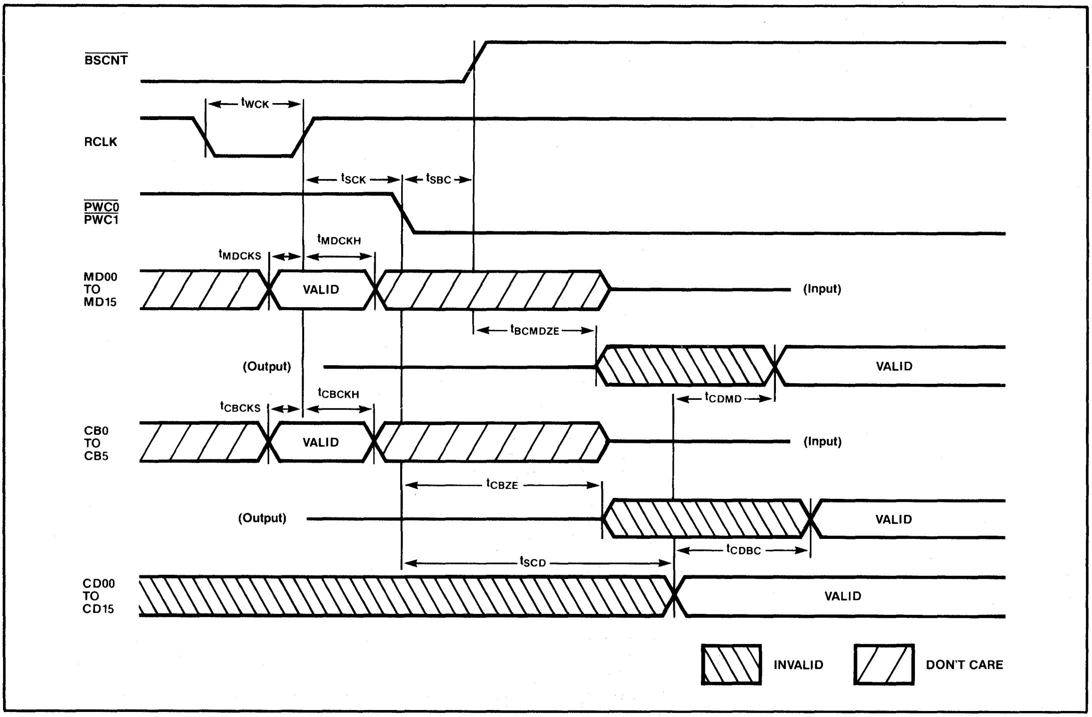
TIMING DIAGRAMS (continued)

Write Mode (Word Write)

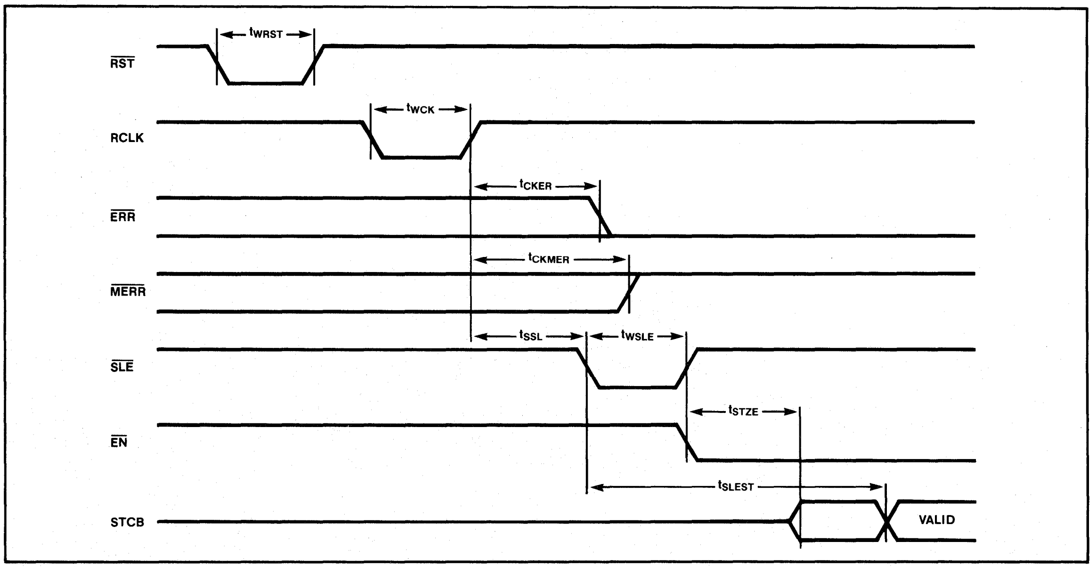


TIMING DIAGRAMS (continued)

Partial Write Mode (Byte Write)

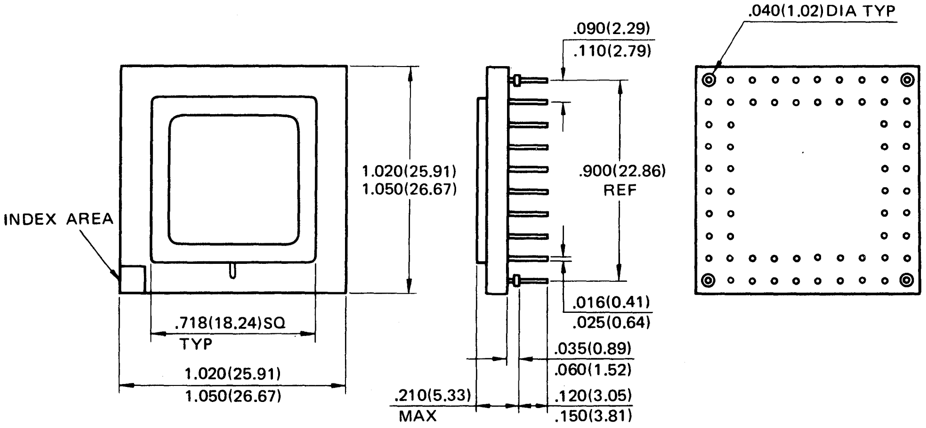


Syndrome Latch



PACKAGE DIMENSIONS

64-Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
(PGA-64C-A01)



Dimensions in
inches (millimeters)

Section 4

Peripheral Support Devices

CRT Controllers

Hard Disk Controller

Floppy Disk Controllers

Television Display Controllers

Protocol Controller

Universal Peripheral Interface Peripherals

Selector Guide for A-to-D/D-to-A Interface Peripherals

CMOS Peripherals

Advanced Products

FUJITSU

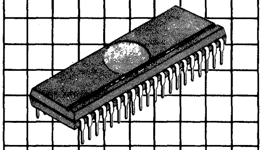
October 1986
Edition 1.0

MB89321A, MB89322A
CMOS Programmable CRT Controller

Description

The MB89321A/MB89322A Programmable CRT Controllers are single chip CMOS devices used to interface CRT raster scan displays with microcomputer systems. Both devices operate on a single +5 V power supply and have TTL-compatible I/O. The MB89321A interfaces to 6800 family microprocessors; the MB89322A to the 8080.

The MB89321A/MB89322A refresh the display by buffering information from main memory using thirty-three internal registers and keeping track of the display position of the screen. Both devices are designed to allow simple interfacing to most raster scan CRTs with a minimum of external hardware and software overhead.

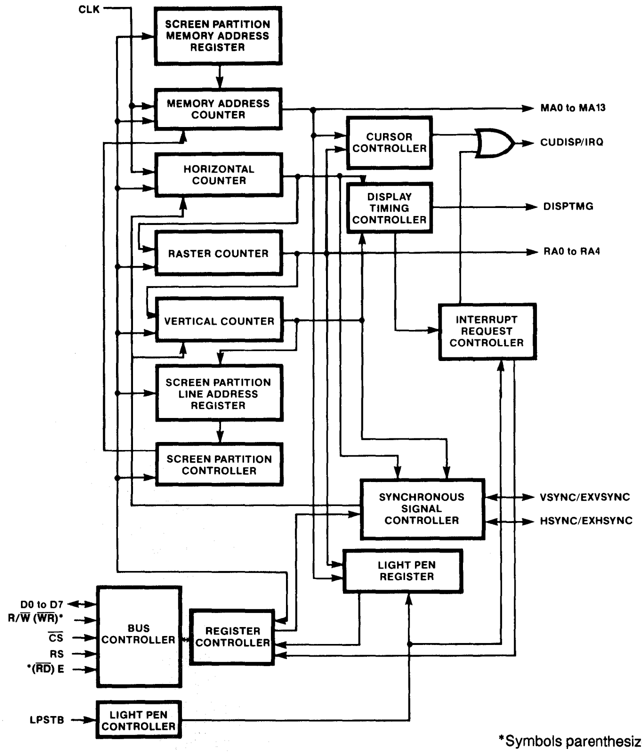


40-Lead Plastic DIP (DIP-40P-M01)

Features

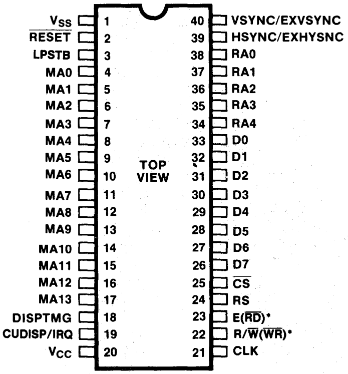
- **Programmable Screen and Character Formats**
- **Cursor Control (3 types)**
- **Selectable Scan Modes (3 types)**
- **Light Pen Detection**
- **Refresh Memory Address Function**
- **Screen Partitioning (up to 4 partitions)**
- **Independent Paging/Scrolling for Each Screen Partition**
- **Smooth Scrolling (up to 4 screens simultaneously)**
- **Status Generation and Processor Interrupt Generation by Vertical Blanking or Light Pen**
- **External Sync for TV Superimposition (synchronous mode) or Interface to Other CRT Controllers (master-slave mode)**
- **Double-Size Vertical Display using Raster Interpolation**
- **4.0 MHz Clock Rate**
- **Single +5 V Power Supply**
- **CMOS Process**
- **40-pin Plastic DIP**

Functional Block Diagram



*Symbols parenthesized are applied to MB89322A.

Pin Assignment



*Symbols parenthesized are applied to MB89322A.

Pin Descriptions

MB89321A(MB89322A)

Pin Number	Symbol	Pin Name	Function
1	V_{SS}	Ground	Ground
2	$\overline{\text{RESET}}$	Reset	Input used for device reset. When $\overline{\text{RESET}}$ goes low: • Internal counters are cleared and stopped; • All outputs go low, and; • Control registers and status register are cleared, other internal registers unaffected. Enabled only when LPSTB is low. $\overline{\text{RESET}}$ goes high, display is initiated immediately. Control registers R30 and R31 must be initialized by software after reset is released.
3	LPSTB	Light Pen Strobe	Character detection input. When high, the memory address is loaded in the light pen register, the raster address in the light pen raster register, and the status bit set.
4 to 17	MA0 to MA13	Memory Address	Refresh memory address output
18	DISPTMG	Display Timing	Display timing output. Set to high during display.
19	CUDISP/ IRQ	Cursor Display Timing/ Interrupt Request	Cursor display timing output/interrupt request output. Set to high during display. Setting the control register enables a high-level interrupt request signal to be output while the display timing signal is low.
20	V_{CC}	Power Supply	+5 V power supply.
21	CLK	Clock	Clock input. Goes low during EXHSYNC in TV sync mode.
22	R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)*	Read/Write (Write)	MPU read/write input. (MPU write input)
23	E ($\overline{\text{RD}}$)*	Enable (Read)	MPU enable input. (MPU read input)
24	RS	Register select	Internal register select input. Normally connected to the least significant bit (A0) of the address bus. When high, selects internal registers; when low, the address register.
25	$\overline{\text{CS}}$	Chip select	Chip select input. Goes low when the MPU accesses the CRTC.
26 to 33	D7 to D0	Data Bus	MPU data bus pins
34 to 38	RA4 to RA0	Raster Address	Raster address output
39	HSYNC/ EXHSYNC	Hsync Output/ Hsync Input	Horizontal sync output/external horizontal sync input. When reset, becomes the horizontal sync output.
40	VSYNC/ EXVSYNC	Vsync Output/ Vsync Input	Vertical sync output/external vertical sync input. When reset, becomes the vertical sync output.

*Symbols parenthesized are applied to MB89322A.

Internal Registers and Functions

		Address					Register		Read	Data Bit							
$\overline{CS}$	RS	4	3	2	1	0	Number	Register Name	Write	7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	—	Invalid	—	▨	▨	▨	▨	▨	▨	▨	▨
0	0	x	x	x	x	x	AR	Address Register	W	▨	▨	▨					
0	1	0	0	0	0	0	R0	Total Number of Characters in Line (*)	W								
0	1	0	0	0	0	1	R1	Number of Characters Displayed in Line	W								
0	1	0	0	0	1	0	R2	Horizontal Sync Position (*)	W								
0	1	0	0	0	1	1	R3	Sync Signal Pulse Width	W	V3	V2	V1	V0	H3	H2	H1	H0
0	1	0	0	1	0	0	R4	Total Number of Lines (*)	W	▨							
0	1	0	0	1	0	1	R5	Total Raster Adjust	W	▨	▨	▨					
0	1	0	0	1	1	0	R6	Number of Lines Displayed	W	▨							
0	1	0	0	1	1	1	R7	Vertical Sync Position (*)	W	▨							
0	1	0	1	0	0	0	R8	Scan Mode/Skew	W	C1	C0	D1	D0	▨	▨	I1	I0
0	1	0	1	0	0	1	R9	Maximum Raster Address	W	▨	▨	▨					
0	1	0	1	0	1	0	R10	Cursor Start Raster	W	▨	B1	B0					
0	1	0	1	0	1	1	R11	Cursor End Raster	W	▨	▨	▨					
0	1	0	1	1	0	0	R12	Start Address 1	R/W	▨	▨						
0	1	0	1	1	0	1	R13										
0	1	0	1	1	1	0	R14	Cursor	R/W	▨	▨						
0	1	0	1	1	1	1	R15										
0	1	1	0	0	0	0	R16	Light Pen	R	▨	▨						
0	1	1	0	0	0	1	R17										
0	1	1	0	0	1	0	R18	Screen 2 Display Start Position (*)	R/W	▨							
0	1	1	0	0	1	1	R19	Start Address 2	R/W	▨	▨						
0	1	1	0	1	0	0	R20										
0	1	1	0	1	0	1	R21	Screen 3 Display Start Position (*)	R/W	▨							
0	1	1	0	1	1	0	R22	Start Address 3	R/W	▨	▨						
0	1	1	0	1	1	1	R23										
0	1	1	1	0	0	0	R24	Screen 4 Display Start Position (*)	R/W	▨							
0	1	1	1	0	0	1	R25	Start Address 4	R/W	▨	▨						
0	1	1	1	0	1	0	R26										
0	1	1	1	0	1	1	R27	Vertical Sync Position Fine Adjust	W	▨	▨	▨					
0	1	1	1	1	0	0	R28	Light Pen Raster	R	DP	▨	▨					
0	1	1	1	1	0	1	R29	Smooth Scroll	R/W	▨	▨	▨					
0	1	1	1	1	1	0	R30	Control	W	VE	VS	IB	IL	SY	TV	P1	P0
0	1	1	1	1	1	1	R31	Control/Status	R/W	SS3	SS2	SS1	SS0	RI*	E	SB	SL

***Note:** Values written to these registers are one (1) less than the set values; refer to Notes on operation

Register Description

Address Register (AR)

Sets the number of the internal register. Unchanged until a new value is written.

Total Number of Characters in Line Register (RO)

Sets horizontal scan sync. Settings indicate number of characters, and are determined by the formula:

Total Number of Characters in Line x Character Period = Horizontal Scan Period

Values written to the register are 1 less than the set values.

Number of Characters Displayed in Line Register (R1)

Sets the horizontal display period. Settings indicate number of characters.

Horizontal Sync Position Register (R2)

Sets the horizontal sync signal position. Settings indicate number of characters. Values written to the register are 1 less than the set values.

Sync Signal Pulse Width Register (R3)

MSB							LSB
V3	V2	V1	V0	H3	H2	H1	H0

Sets the sync signal pulse width. The 4 high-order bits are used for the vertical sync signal, the 4 low-order bits for the horizontal sync signal. the TV sync mode, the 4 low-order bits are used as the horizontal back porch.

Total Number of Lines Register (R4)

Used the the total raster adjust register to set vertical sync (field sync is set by number of rasters). Setting is in number of lines. Values written to the register are 1 less than the set value.

Total Raster Adjust Register (R5)

Used to fine tune the vertical sync. Settings indicate number of rasters, and must be less than the maximum raster address. Vertical sync is determined by the formula:

Vertical Sync = Total Number of Lines x Maximum Raster Address + Total Raster Adjust

Number of Lines Displayed Register (R6)

Sets the vertical display period. Settings indicate number of lines.

Vertical Sync Position Register (R7)

Used with the vertical sync position fine adjust register (R27) to set vertical sync position using raster count. Settings indicate number of lines. Values written to the register are 1 less than the set values.

Scan Mode/Skew Register (R8)

MSB							LSB
C1	C0	D1	D0	▨	▨	I1	I0

Sets cursor display signal and display timing signal skew, and the scan mode. Bit functions are as shown below:

C1	C0	CUDISP Output
0	0	Output without skew
0	1	Skewed by 1 character
1	0	Skewed by 2 characters
1	1	No CUDISP output

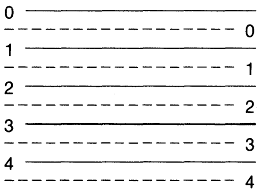
D1	D0	DISPTMG Output
0	0	Output without skew
0	1	Skewed by 1 character
1	0	Skewed by 2 characters
1	1	No DISPTMG output

I1	I0	Scan Mode
0	0	Non-interlace mode
0	1	Interlace mode
1	0	Non-interlace mode
1	1	Interlace and video mode

Maximum Raster Address Register (R9)

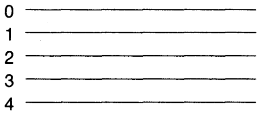
Sets the number of rasters in a line. In interlace and non-interlace modes, the value written is 1 less than the set value; in interlace and video mode, 2 less. Examples of settings in each mode are as follows:

Interlace mode



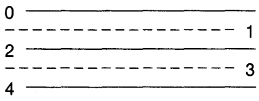
Raster count - 5
Value written - 4

Non-interlace mode



Raster count - 5
Value written - 4

Interlace & video modes



Raster count - 5
Value written - 3

Non-interlace mode and Interlace mode:
Written value = Setting value −1
Interlace mode & video mode:
Written value = Setting value −2

Register Description
(Continued)

Cursor Start Raster Register (R10)

MSB							LSB
▨	B1	B0					

Sets the cursor display mode and the display start raster. Settings indicate number of rasters. Cursor display mode bit function is as follows:

B1	B0	Cursor Display Mode
0	0	Displays without blinking
0	1	No display
1	0	Blinks in 16-field sync
1	1	Blinks in 32-field sync

Cursor End Raster Register (R11)

Sets the cursor display end raster. Settings indicate number of rasters.

Start Address Registers (R12, R13, R19, R20, R22, R23, R25, R26)

Four sets of 14-bit paired registers used to set the starting memory address for screen display that enable independent paging/scrolling when screen is partitioned. Registers are for Start Address 1 (R12, R13), Start Address 2 (R19, R20), Start Address 3 (R22, R23) and Start Address 4 (R25, R26).

Cursor Registers (R14, R15)

14-bit paired registers used to set the cursor display memory address.

Light Pen Registers (R16, R17)

14-bit paired registers to which the memory address is written when the light pen strobe signal goes high. Memory address value must be compensated in software for delay in the light pen detection circuit.

Light Pen Raster Register (R28)

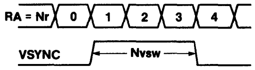
MSB							LSB
DP	▨	▨					

Register to which the raster address and display status bit are written when the light pen strobe signal goes high. When the light pen register or light pen raster register are written to during the display period, the display status bit is set to 1; during blank period, reset to 0.

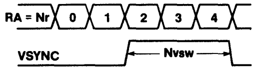
Vertical Sync Position Fine Adjust Register (R27)

Used to fine-tune the vertical sync signal within the line set by the vertical sync position register. Settings indicate number of rasters. Examples of settings are shown below:

Setting Value = 1



Setting Value = 2



Setting 0 must not be written as it will cause the control register to disable the vertical sync position adjust register, resulting in a vertical sync signal output of RA = 0. The set value must be less than the maximum raster address.

Display Start Position Registers (R18, R21, R24)

Sets the starting line numbers for display start addresses 2, 3, and 4 when screen is partitioned. See following figure. Values written to the register are 1 less than the line number; 0 must not be written. Examples of settings are shown below:

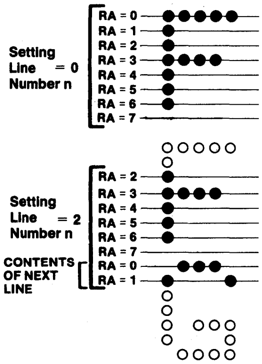
Line Number	Display Screen
0 1 2	Screen 1 (Start address 1)
3	Screen 2 (Start address 2, Register 18)
4 5 6 7	Screen 3 (Start address 3, Register 21)
8 9	Screen 4 (Start address 4, Register 24)

Value written for start position 2 = 2
Value written for start position 3 = 3
Value written for start position 4 = 7

Smooth Scroll Register (R29)

Sets the starting raster address within a line. Setting indicates number of rasters. Smooth scrolling can be used in interlace and non-interlace modes only.

Settings are valid for screens specified by SS3 to SS0 of the control/status register. Settings must be less than the maximum raster address. Examples of settings are shown below:



Register Description
(Continued)

Control Register (R30)

MSB LSB

VE	VS	IB	IL	SY	TV	P1	P0

Controls the external sync function, interrupt function, vertical sync position fine adjust function and screen partition function. This register must be initialized by software after reset is released. Bit functions are as shown below:

VE	VS	TV	External Sync Function
0	0	0	Both VSYNC and HSYNC are in output mode. DISPTMG is active. External sync operation is disabled.
0	1	0	Outputs VSYNC for odd-numbered fields only in interlace mode. No VSYNC output when the programmed values of max. raster address and vertical sync position are odd numbers in interlace & video mode.
1	0	0	EXVSYNC is in input mode but external sync signal ignored. DISPTMG is active.
1	1	0	EXVSYNC is in input mode and external sync signal is accepted. DISPTMG goes low (disabled).
0	0	1	Disallowed
0	1	1	Disallowed
1	0	1	Both EXVSYNC and EXHSYNC are in input mode and external sync signal is accepted. DISPTMG output is active.
1	1	1	Both EXVSYNC and EXHSYNC are in input mode and external sync signal is accepted. DISPTMG goes low (disabled).

Notes:
1. When VS = 1, DISPTMG goes low.
2. When TV = 0, indicates master-slave mode. When TV = 1, indicates TV sync mode.
3. In TV sync mode, the horizontal back porch must be set using the horizontal sync pulse width register.
4. In TV sync mode, the internal control is in non-interlace mode.

IB	IL	Interrupt Function
0	0	None
0	1	With light pen strobe
1	0	With vertical blanking
1	1	With light pen or vertical blanking

Note: Interrupt signal is output for CUDISP while DISPTMG is low.

SY	Vertical Sync Position Fine Adjust Function
0	Vertical sync position fine adjust register disabled
1	Vertical sync position fine adjust register enabled

P1	P0	Screen Partition Function
0	0	Start Address 1 enabled
0	1	Start addresses 1 and 2 enabled; screen partitioned into two sections
1	0	Start addresses 1, 2, and 3 enabled; screen partitioned into three sections
1	1	Start addresses 1, 2, 3, and 4 enabled; screen partitioned into four sections

Note: Screen address 1 is always displayed starting from line number 0.

Register Description
(Continued)

Control/Status Register (R31)

MSB … LSB

SS3	SS2	SS1	SS0	RI	0	0	0

Write

MSB … LSB

					E	SB	SL

Read

Controls the smooth scrolling and raster interpolation functions, and performs read/write of the status register. This register must be initialized by software after reset is released. Control bit functions are as follows:

Control Bits	Function

SS3 to SS0	Smooth scrolling control bits; when set to 1 the smooth scrolling register is enabled. Bits correspond to the screens as follows:
	SS3 = screen 4
	SS2 = screen 3
	SS1 = screen 2
	SS0 = screen 1

RI	Raster interpolation bit. Set to 1, raster interpolation is performed. The raster counter is incremented every two rasters, doubling the vertical sync rate. Therefore, in this case, registers related to vertical sync control must be reprogrammed. The raster interpolation function can't be used in external sync mode and interlace & video mode.

Notes:
1. "0s" must be written to lower 3 bits of the control register.
2. Refer to diagram of "Double-Size Vertical Display" and item 6 of Notes on Operation.

Status Bits

The functions of status bits are as follows:

E	Display Field Status
0	Odd-numbered screen display, or in non-interlace mode
1	Even-numbered screen display

SB	Vertical Blanking Status
0	During screen display
1	During vertical blanking

SL	Light Pen Strobe Status
0	Light pen strobe ignored
1	Light pen strobe accepted

Notes:
1. Light pen strobe status is cleared by reset or by read of the status register.
2. Vertical blanking status and light pen strobe status are set regardless of the setting of the control register interrupt function.
3. E bit is controlled by the vertical blank. Therefore, E bit status is different from normal field image, and it's update timing changes depending on number of lines displayed. To get correct status, E bit must be read immediately after the display period.

Restrictions on Values Written to Registers

Values which may be written to internal registers are as follows:

(1) 0 < number of characters displayed in line (R1) < total number of characters in line (R0) + 1 ≤ 256

(2) 0 < number of lines displayed (R6) < total number of lines (R4) + 1 ≤ 128

(3) 0 ≤ horizontal sync position (R2) ≤ total number of characters in line (R0)

(4) 0 ≤ vertical sync position (R7) ≤ total number of lines (R4)

(5) 0 ≤ cursor start raster (R10) ≤ cursor end raster (R11) ≤ maximum raster address (R9)
(interlace mode and non-interlace modes)
0 ≤ cursor start raster (R10) ≤ cursor end raster (R11) ≤ maximum raster address (R9) + 1
(interlace & video mode)

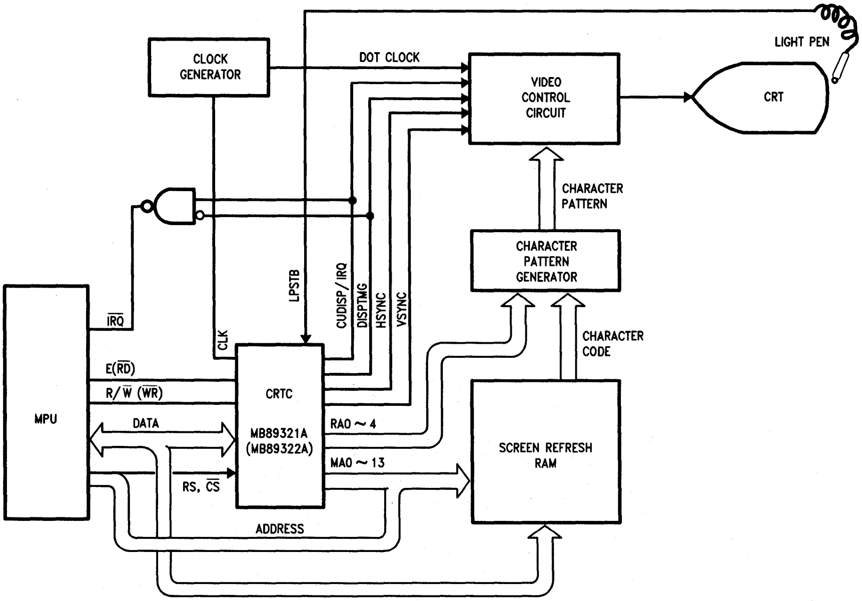
(6) 2 ≤ maximum raster address (R9) ≤ 30
(interlace & video mode only)

(7) 3 ≤ total number of characters in line (R0)
(except in non-interlace mode)
5 ≤ total number of characters in line (R0)
(non-interlace mode only)

(8) Vertical sync position fine adjust (R27) < maximum raster address (R9)

(9) Smooth scroll (R29) ≤ maximum raster address (R9)

System Block Diagram

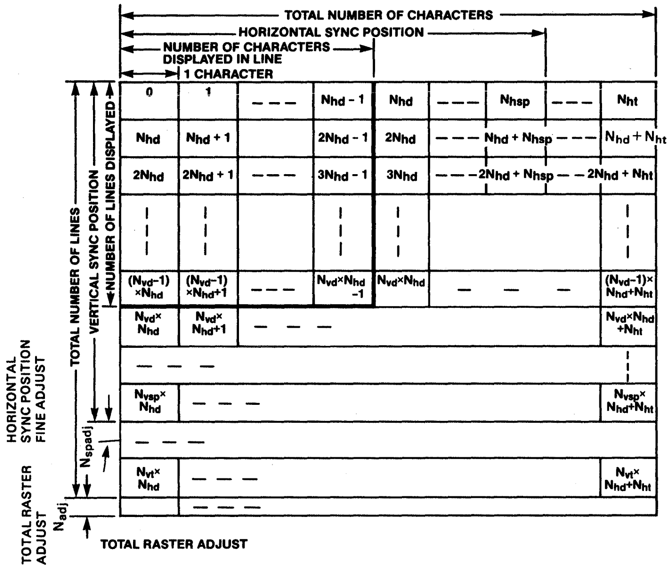


Programmable Values

Programmable values which can be written to registers and their respective symbols are as shown below:

Register Number	Register Name	Programmable Value	Symbol
R0	Total Number of Characters in Line	Characters	Nht
R1	Number of Characters Displayed in Line	Characters	Nhd
R2	Horizontal Sync Position	Characters	Nhsp
R3	Sync Signal Pulse Width	Rasters/Characters	Nvsw/Nhsw
R4	Total Number of Lines	Lines	Nvt
R5	Total Raster Adjust	Rasters	Nadj
R6	Number of Lines Displayed	Lines	Nvd
R7	Vertical Sync Position	Lines	Nvsp
R8	Scan Mode/Skew		
R9	Maximum Raster Address	Rasters	Nr
R10	Cursor Start Raster	Rasters	N_{CSTART}
R11	Cursor End Raster	Rasters	N_{CEND}
R12 R13	Start Address 1		N_{SI}
R14 R15	Cursor		
R16 R17	Light Pen		
R18	Screen 2 Display Start Position	Lines	N_{L2}
R19 R20	Start Address 2		N_{S2}
R21	Screen 3 Display Start Position	Lines	N_{L3}
R22 R23	Start Address 3		N_{S3}
R24	Screen 4 Display Start Position	Lines	N_{L4}
R25 R26	Start Address 4		N_{S4}
R27	Vertical Sync Position Fine Adjust	Rasters	Nspadj
R28	Light Pen Raster		
R29	Smooth Scroll	Rasters	Nradj
R30	Control		
R31	Control/Status		

Screen Format



Line numbers are counted starting at the following addresses:

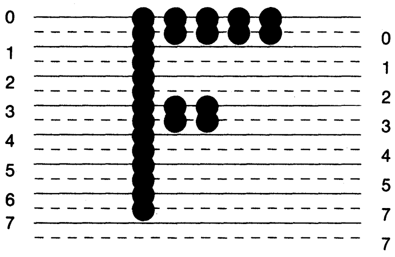
Line number 0 = starts from memory address 0
Line number 1 = starts from memory address Nhd
Line number 2 = starts from memory address 2Nhd

Line number n = starts from memory address (Nvd-1)Nhd

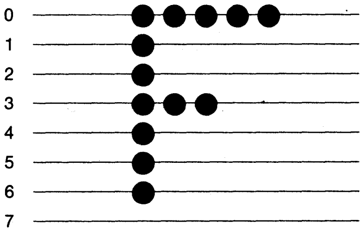
Scan Mode

Examples of format during scan mode:

Interlace Mode



Non-Interlace Mode

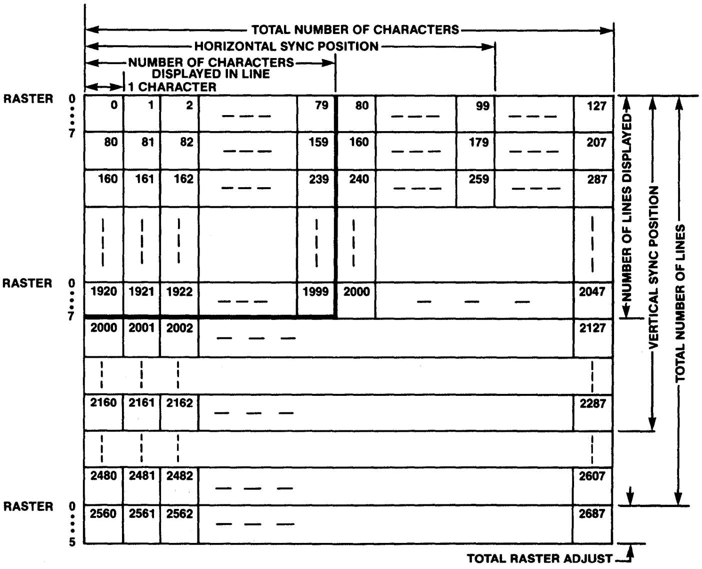


Example of Screen Format

Dot clock rate	16.128 MHz
Horizontal frequency	15.75 kHz
Vertical frequency	60.1145 Hz

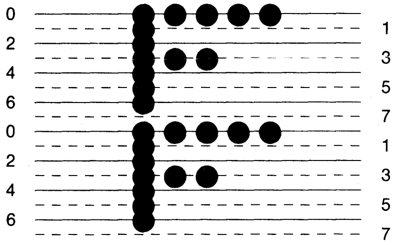
At the following clock rates and register settings, the screen format is as shown in the diagrams below:

Total number of characters in line, Register 0:	127
Number of characters displayed in line, Register 1:	80
Horizontal sync position, Register 2:	99
Sync signal pulse width, Register 3:	8
Total number of lines, Register 4:	31
Total raster adjust, Register 5:	6
Number of lines displayed, Register 6:	25
Vertical sync position, Register 7:	27
Maximum raster address, Register 9:	8

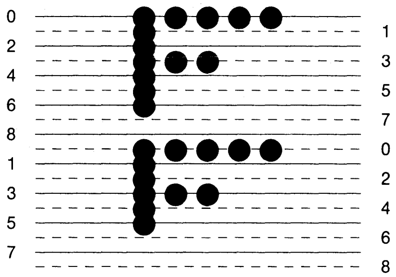


Scan Mode
(Continued)

Interlace & Video Modes



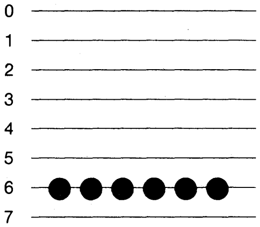
Even number of rasters in a line



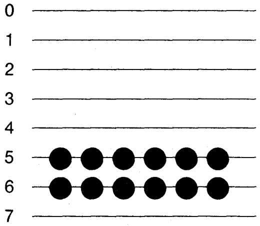
Odd number of rasters in a line

Cursor Control

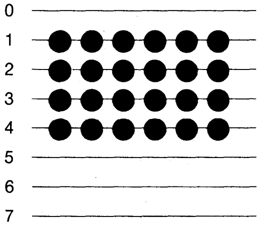
Examples of settings for the cursor start and end raster registers:



Start address = 6
End address = 6



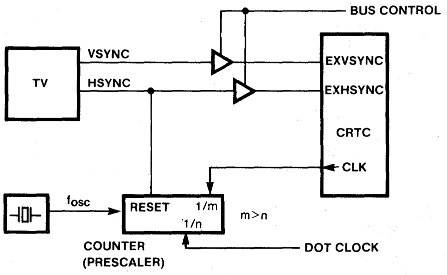
Start address = 5
End address = 6



Start address = 1
End address = 4

TV Sync Mode

Example of a TV Sync mode circuit:

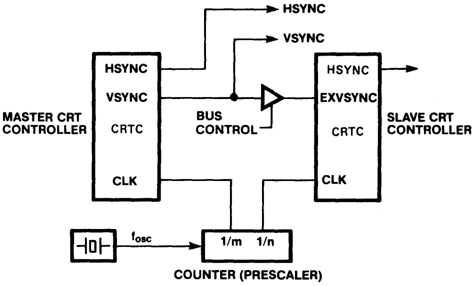


TV sync mode is used to superimpose displays on TV or video signals. In the above example a 1/n f_{OSC} dot shift will occur. Accordingly, an appropriate prescaler should be designed to avoid image resolution problems.

During HSYNC, CLK must be low (stopped).

Master-Slave Mode

Example of a master-slave mode circuit:

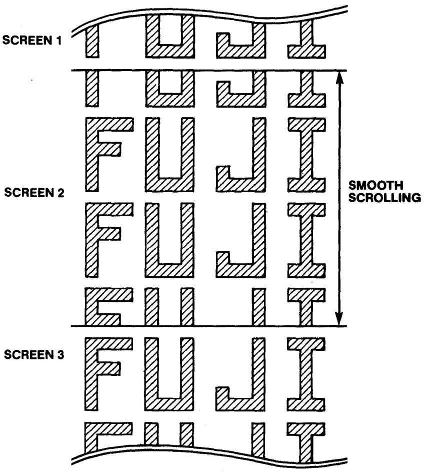


Master-slavemode is used to synchronize master and slave CRT controllers. The screen formats and clock phases of the two CRTCs must match.

Since HSYNC is output, PLL can be used.

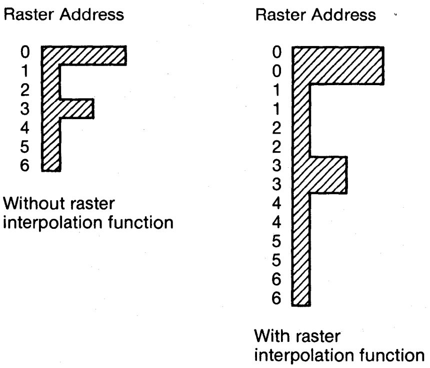
Smooth Scroll

Example of smooth scrolling display:



In the example, screen 2 is being smooth scrolled.

Double-Size Vertical Display


Raster Address
0
1
2
3
4
5
6
Without raster interpolation function
Raster Address
0
0
1
1
2
2
3
3
4
4
5
5
6
6
With raster interpolation function

The vertical size of the display can be doubled using the raster interpolation function as shown in the example.

In raster interpolation, the raster address is updated every second raster.

Refer to item 6 of Notes on Operation.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	−0.3 to +7.0	V
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	600	mW

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
		V_{SS}		0.0		V
Input High Voltage	LPSTB, CLK	V_{IH1}	2.2		V_{CC}	V
	Other Inputs	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	LPSTB, CLK	V_{IL1}	−0.3		0.6	V
	Other Inputs	V_{IL}	−0.3		0.8	V
Ambient Temperature		T_A	−20	25	+75	°C

DC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter		Symbol	Test Conditions	Value			Unit
				Min	Typ	Max	
Input High Voltage	LPSTB, CLK	V_{IH1}		2.2		V_{CC}	V
	Other Inputs	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	LPSTB,CLK	V_{IL1}		−0.3		0.6	V
	Other Inputs	V_{IL}		−0.3		0.8	V
Input Leakage Current	D0 to D7, EXHSYNC, EXVSYNC	I_{IL}	V_{IN} = 0.4 V to 2.4 V, V_{CC} = 5.5 V	−10		10	μA
	Other Inputs	I_{IL_1}	V_{IN} = 0 V to 5.5 V	−2.5		2.5	μA
Output High Voltage	D0 to D7	V_{OH}	I_{OH} = −205 μA	2.4			V
	Other Outputs	V_{OH1}	I_{OH} = −100 μA	2.4			V
Output Low	Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Capacitance	D0 to D7, EXHSYNC, EXVSYNC	C_{IN}	V_{IN} = 0 V			12.5	pF
	Other Outputs	C_{IN_1}	f = 1.0 MHz			10.0	pF
Ouput Capacitance		C_{OUT}				10.0	pF
Power Dissipation		P_D	V_{CC} = V_{max} f = 1.0 MHz		10	30	mW

AC Characteristics

Recommended operating conditions unless otherwise noted.

	Parameter	Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
CRT Controller	Clock Period	t_{CLK}	(1)	250			ns
	Clock High	t_{PWCH}		100			ns
	Clock Low	t_{PWCL}		100			ns
	Clock Rise	t_{CR}				20	ns
	Clock Fall	t_{CF}				20	ns
	Memory Address Delay	t_{MAD}				80	ns
	Raster Address Delay	t_{RAD}				100	ns
	Display Timing Delay	t_{DTD}				120	ns
	Cursor Timing Delay	t_{CDD}				120	ns
	Horizontal Synchronous Delay	t_{HSD}				100	ns
	Vertical Synchronous Delay	t_{VSD}				120	ns
External Synchronization	Clock Stop	t_{CLKST}	(2)	100			ns
	External Horizontal Synchronous Signal Width	t_{PWHS}		1000			ns
	External Horizontal Synchronous Rise	t_{HR}				20	ns
	External Horizontal Synchronous Fall	t_{HF}				20	ns
	External Vertical *1 Synchronous Signal Width	t_{PWVS}/ t_{PWVSS}		1220/ 1750			ns
	External Vertical Synchronous Rise	t_{VR}				20	ns
	External Vertical Synchronous Fall	t_{VF}				20	ns
	External Synchronous Setup (Master-slave mode)	t_{VSS}		50			ns
Light Pen	Light Pen Strobe Width	t_{PWLP}	(3)	60			ns
	Light Pen Strobe Maximum Period	t_{LPDR} t_{LPDF}				0 70	ns ns
CRT Interface 1	Enable Period	t_E	[(4) MB89321A only]	0.5			μs
	Enable High	t_{PWEH}		0.22			μs
	Enable Low	t_{PWEL}		0.21			μs
	Enable Rise	t_{ER}				20	ns
	Enable Fall	t_{EF}				20	ns
	Address Setup	t_{AS}		40			ns
	Data Delay	t_{DDR}				120	ns
	Data Access	t_{ACC}				160	ns
	Address Hold	t_{AH}		10			ns
	Data Hold	t_H		10			ns
	Data Setup	t_{DSW}		60			ns

AC Characteristics

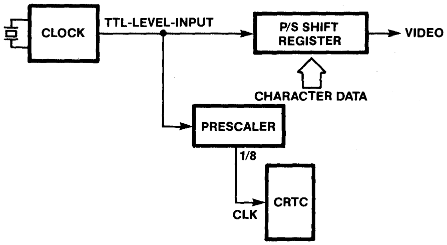
(Continued)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
CPU Interface 2	Read Address Setup	t_{AR}	[(5)MB89322A only]	0			ns
	Read Low	t_{RR}		160			ns
	Read Address Hold	t_{RA}		0			ns
	Write Address Setup	t_{AW}		0			ns
	Write Low	t_{WW}		190			ns
	Write Address Hold	t_{WA}		0			ns
	Data Delay	t_{RD}				120	ns
	Data Hold	t_{DF}		10			ns
	Data Setup	t_{DW}		60			ns
	Data Hold	t_{WD}		0			ns
	Access Inhibit	t_{DIS}		210			ns
IRQ	Interrupt Delay	t_{IRDF}	(6)			150	ns
	Interrupt Delay *2	t_{IRDR}				$1/2t_{clk}$ +150	ns

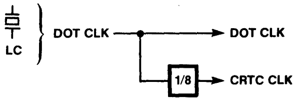
Note: *1. External vertical synchronous signal width t_{PWVS} = 1000 ns + t_{CLK} (TV sync mode)
t_{PWVSS} = 1000 ns + 3 t_{CLK} (Master slave mode)
*2. Rising delay time when light pen strobe input in non display time

Clock

A TTL-level input from DC to 4.5 MHz character clock should be used. An example of the clock circuit is shown below.

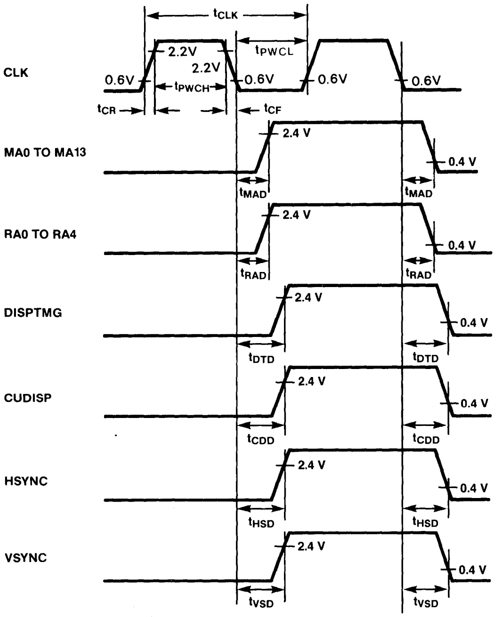


A circuit example for horizontal 8-dot character mode is as follows:

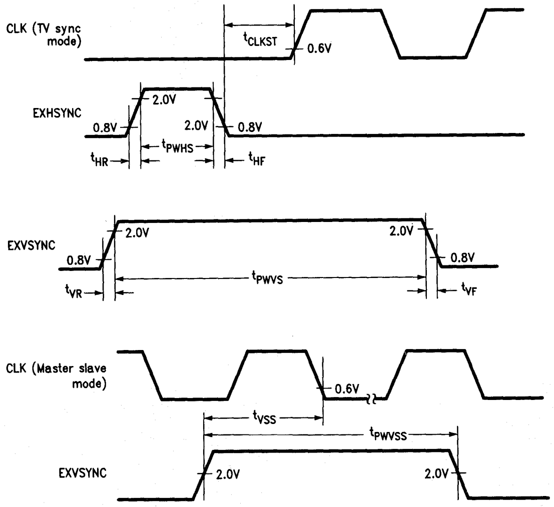


Timing Diagrams

(1) CRT Controller

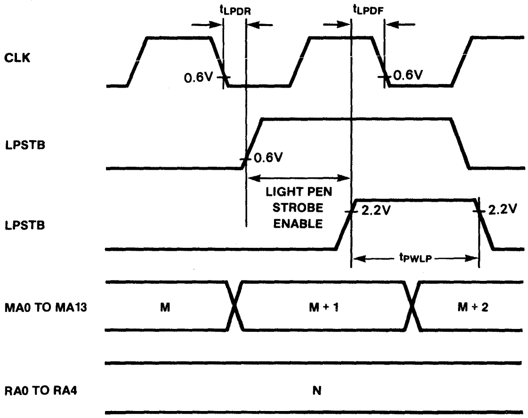


(2) External synchronization



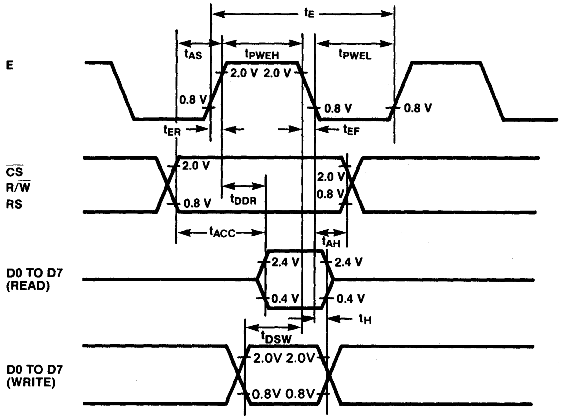
Timing Diagrams
(Continued)

(3) Light Pen



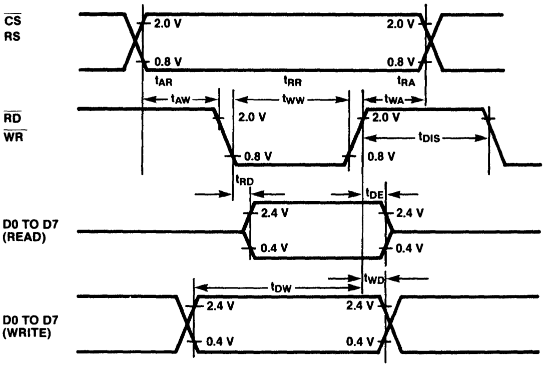
When the light pen strobe is enabled, LPSTB goes high, M+2 is loaded into the light pen register, N into the light pen raster register, and the display status bit is set.

(4) CPU Interface 1 (MB89321A only)

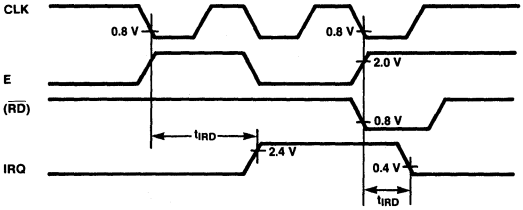


Timing Diagrams
(Continued)

(5) CPU Interface 2 (MB89322A only)

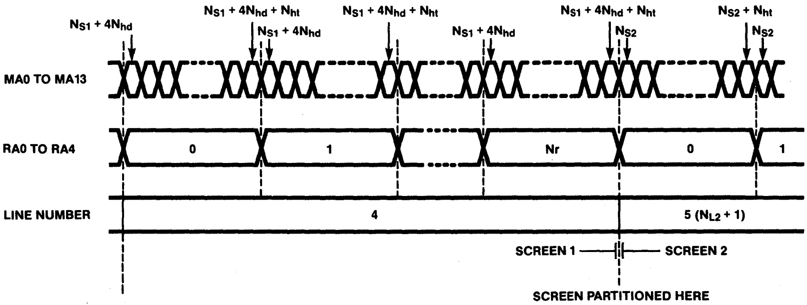


(6) IRQ Timing



Notes on Operation

(1) Screen Partition Timing

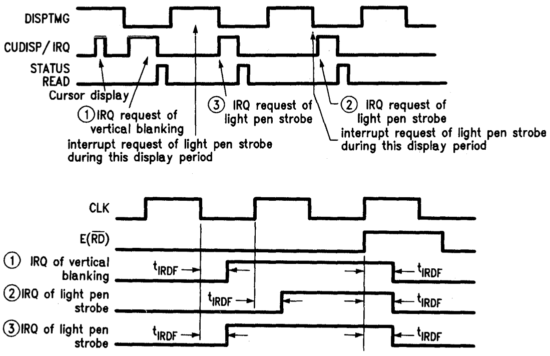


This example shows typical memory addresses and raster addresses of screens 1 and 2 during screen partitioning.

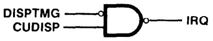
Nht: Total Number of Characters in Line (R0)
Nhd: Number of Characters Displayed in Line (R1)
Nr : Maximum Raster Address (R9)
Ns1: Start Address 1 (R12, R13)
NL2: Screen 2 Display Start Position (R18)
NS2: Start Address 2 (R19, R20)

Notes on Operation
(Continued)

(2) Interrupt Signal Generator Timing

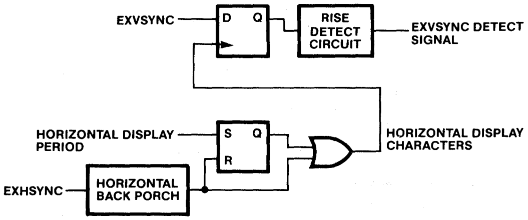

DISPTMG
CUDISP/IRQ
STATUS READ
Cursor display
① IRQ request of vertical blanking
interrupt request of light pen strobe during this display period
③ IRQ request of light pen strobe
② IRQ request of light pen strobe
interrupt request of light pen strobe during this display period
CLK
E(RD)
① IRQ of vertical blanking
② IRQ of light pen strobe
③ IRQ of light pen strobe
t_{IRDF}

The interrupt signal is output to the CUDISP pin during display blanking. The interrupt signal can be generated as shown in the diagram below.



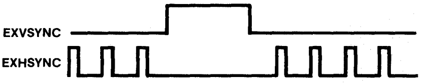
When the cursor is not enabled, the CUDISP pin functions as IRQ.

(3) TV Sync Timing

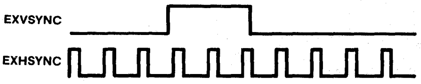


In TV sync mode, EXHSYNC is enabled when a pulse of 1,000 ns or more is applied. Also, during vertical blanking, EXVSYNC is enabled to sync the controller's internal horizontal display period signal. In order to use the TV sync function, a horizontal display period should be set. The basic circuit required to do this is shown to the left.

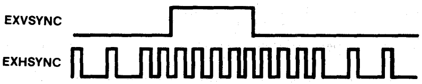
Note: Low (enabled) during the horizontal display period.



The TV sync function may not operate under the timing shown here at the immediate left.



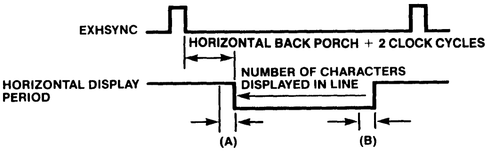
The TV sync function is activated using the timing as shown here.



Notes on Operation
(Continued)

(4) Horizontal Display Period Setting (TV Sync Mode)

The horizontal display period is determined by the timing diagrams below:


EXHSYNC
HORIZONTAL BACK PORCH + 2 CLOCK CYCLES
NUMBER OF CHARACTERS DISPLAYED IN LINE
HORIZONTAL DISPLAY PERIOD
(A)
(B)

(A) and (B) indicate points where EXVSYNC is detected.

EXVSYNC is normally detected at (B). However, when EXHSYNC is generated during the horizontal display period by an equivalent pulse, detection is at (A).

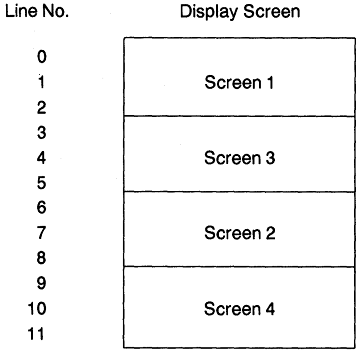
(A) and (B) require at least 1,000 ns + 1 clock cycle, during which period EXVSYNC must be maintained.

(5) Screen Partitioning

The display order of partitioned screens can be changed by programming the start position registers (R18, R21, and R24) for each partitioned screen, except screen 1, which is always displayed from line 0 on the screen. (See Figure A below.)

But, when the same values are programmed to the start position registers, the partitioned screens for those start position registers aren't displayed, even if those partitioned screens are enabled by P0 and P1 bits.

Figure A



Example of Register Setting

Screen 3 Start Position (R21)
≤ Screen 2 Start Position (R18)
≤ Screen 4 Start Position (R24)

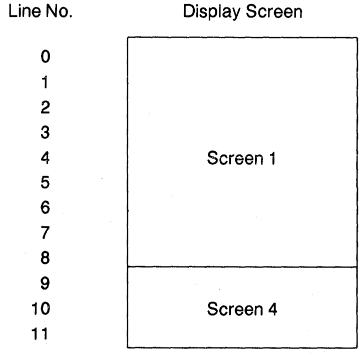
- Screen 2 Start Position Reg. (R18) = 5
- Screen 3 Start Position Reg. (R21) = 2
- Screen 4 Start Position Reg. (R24) = 8

Notes on Operation
(Continued)

(6) Raster Interpolation

At present, two versions of MB89321A/89322A are provided: One has the raster interpolation function, and another has no raster interpolation function. On MB89321A/89322A without the raster interpolation function, "0" must always be written to RI bit of the control/status register (R31).

Figure B



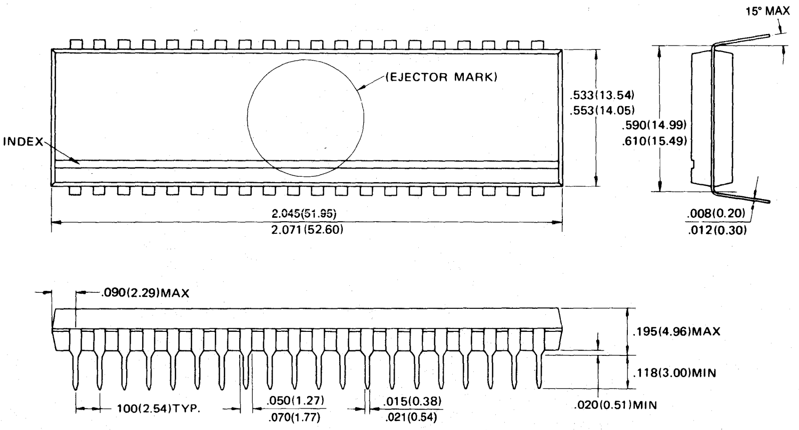
Example of Register Setting

Screen 2 Start Position (R18)
= Screen 3 Start Position (R21)
≤ Screen 4 Start Position (R24)

- Screen 4 Start Position Reg. (R24) = 8
- Screens 2 and 3 aren't displayed because the start position registers for these screens have the same value. In the display areas for Screens 2 and 3, Screen 1, which is displayed above those screens, is displayed.

Package Dimensions
Dimensions in inches (millimeters)

40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



FUJITSU

PROGRAMMABLE CRT CONTROLLER

MB89321B MB89322B

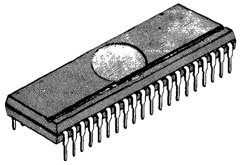
October 1986
Edition 1.0

DESCRIPTION

The Fujitsu MB89321B/MB89322B Programmable CRT Controllers are used to interface a CRT raster-scan display with a microcomputer system. The MB89321B is pin-for-pin compatible with the 6845 controller and is designed to interface with the 6800-series of microprocessors from Motorola. The MB89322B is designed to interface with the 8080-series of microprocessors from Intel; because the Intel bus requires separate read/write lines, the MB89322 is not a direct replacement for 6845.

Both devices refresh the CRT display by buffering information from main memory. Eighteen internal registers track the display position on the screen and provide a realtime presentation of the video data. The interface with most raster-scan CRT displays is simple and the hardware/software overhead is minimal.

Together, the MB89321A/MB89322A and MB89321B/MB89322B controllers provide design alternatives for the bus-interface requirements shown at the bottom of this page. The MB89321 and MB89322 can be ordered with or without enhancements. Non-enhanced versions (suffix B) contains all standard features of the 6845; enhanced versions (suffix A) provide all standard features of the 6845 plus smooth scroll, additional screen partitioning, independent scrolling of screen partitions, and other convenient features.

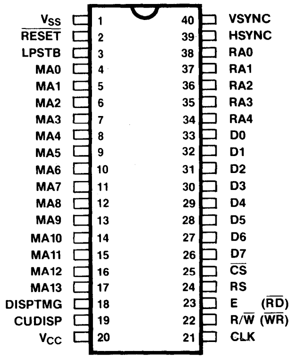


40-Pin Plastic DIP
(DIP-40P-M01)

FEATURES

- Programmable screen and character formats
- Cursor control display: Form, Position, and Blink
- Three selectable scan modes: Interlace, Non-interlace, and Interlace with Video
- 14-bit refresh memory address output: 16K word refresh memory addressing capability
- 5-bit raster address output: Up to 32 rasters per character
- Light pen detection: Refresh memory address capture
- Flexible bus interface: 6800 compatible bus for MB89321B, 8080 compatible bus for MB89322B
- Up to 4 MHz clock rate
- Silicon gate CMOS process/TTL compatible I/O
- Single +5V power supply/40-pin plastic DIP (Suffix P)

PIN ASSIGNMENTS



Legend:
( ) = MB89322B

Bus Interface	MB89321A	MB89322A	MB89321B	MB89322B	6845
8080 Bus Interface (Intel)		X		X	
6800 Bus Interface (Motorola)	X		X		X
Enhanced (Note)	X	X			
Non-Enhanced			X	X	X

Note:
The MB89321A and MB89322A provide all features of the 6845; however, both devices require that Registers 30 and 31 be cleared during initialization. The clearing command is not required for the 6845 or the non-enhanced (MB89321B/MB89322B) devices.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU HARD DISK CONTROLLER MB89341

October 1986
Edition 1.0

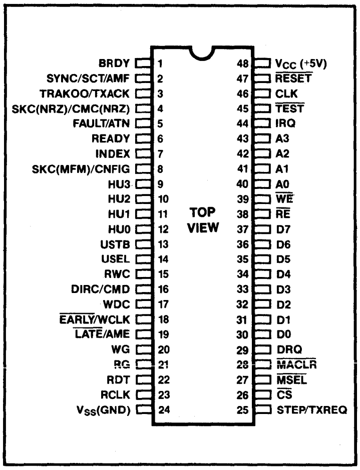
DESCRIPTION

The Fujitsu MB89341 Hard Disk Controller (HDC) interfaces with a host processor and a hard disk drive unit and provides data transfers between the two units in accordance with commands loaded from the host processor. The HDC is fabricated in CMOS and is housed in a 48-pin shrink DIP.

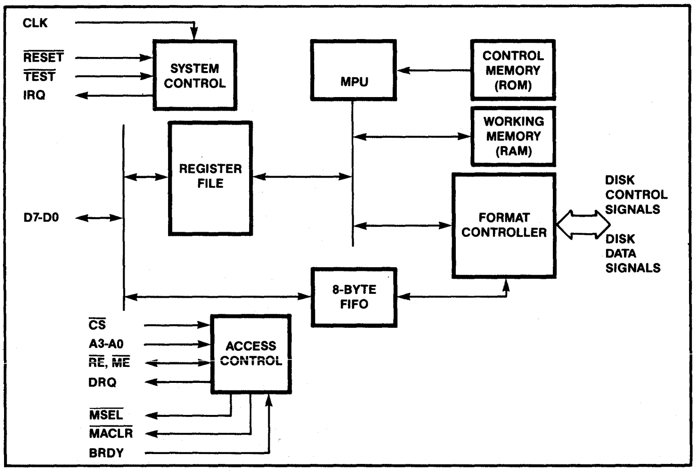
FEATURES

- Two programmable modulation modes: MFM and NRZ.
- High speed data transfers —
  MFM: Maximum of six megabits per second (typically 5 Mbps).
  NRZ: Maximum of 12 megabits per second (typically 10 Mbps).
- Programmable step rate —
  Fast: 1-to-8 μs in eight steps.
  Slow: 0.5-to-4 ms in eight steps.
- Multi-sector read/write and multi-track read/write.
- On-chip 8-byte FIFO for timing control of data transfers.
- On-chip memory buffer with arbitration logic.
- On-chip ECC with 32-bit fire code.
- Supports 16 drives and 16 head selections.
- Interface compatibility with Seagate ST506/412 specification and ESDI specification.
- CPU interface: Parallel data loading to register array.
- Silicon-gate CMOS process.
- Single +5V supply.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU
MICROELECTRONICS

MB8876A
MB8877A

October 1986
Edition 2.0

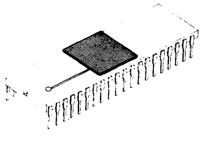
FLOPPY DISK FORMATTER/CONTROLLER (FDC)

DESCRIPTION

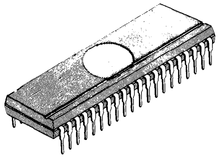
The Fujitsu MB8876A and MB8877A are one-chip Floppy Disk Formatter/Controllers (FDC) which are fabricated with N-channel E/D MOS technology. They can be applied to any single density floppy disk, double density floppy disk and mini floppy disk.

The IBM3740 format and the frequency modulation (FM) recording are used for the single density storage, and the IBM System-34 format and the modified frequency modulation (MFM) recording are used for the double density storage.

The MB8867A and MB8877A interface with an 8-bit parallel microprocessor to control data transfer and mechanical operation. They are packaged in a standard 40-pin dual in-line package.



CERAMIC DIP
DIP-40C-A01

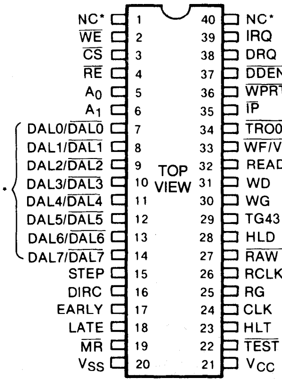


PLASTIC DIP
DIP-40P-M01

FEATURES

- **Interface to 8-bit Microprocessor**
  - **MB8876A: Negative-logic 8-bit Data Bus**
  - **MB8877A: Positive-logic 8-bit Data Bus**
- **IBM Compatible Sector Format**
- **Automatic Track Seeking and Verification**
- **Both Single and Double Density Formats**
  - **a) Single Density in IBM3740 Format and FM Recording**
  - **b) Double Density in IBM System-34 Format and MFM Recording**
- **Programmable Single Sector/ Multiple Sectors/Entire Track Read Operation**
- **Programmable Single Sector/ Multiple Sectors/Entire Track Write Operation**
- **Programmable Side Compare Function**
- **Programmable Sector Length**
- **Programmable Head Step Rate**
- **Applicable to Single Density, Double Density, and Mini Floppy Disks**
- **Programmable Head Engage/Head Settle Time**
- **Double Buffered Data I/O**
- **DMA Data Transfer Capability**
- **Write Precompensation Capability**
- **All TTL Compatible I/O**
- **Single +5V Power Supply**
- **N-Channel Silicon-gate E/D MOS Process**
- **MB8876A: Upward Compatible with Western Digital FD1791-02**
- **MB8877A: Upward Compatible with Western Digital FD1793-02**
- **Two Package Options**
  - **—40-pin Ceramic DIP (Suffix: -C)**
  - **—40-pin Plastic DIP (Suffix: -P)**

PIN ASSIGNMENT



PACKAGE
DIP-40C-A01
*: No Connection
.. { MB8876A: Negative Logic
MB8877A: Positive Logic

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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PIN DESCRIPTIONS

Pin No.	Symbol	Pin Name	I/O	Description
20	V_{SS}	Power Supply	I	Ground (GND)
21	V_{CC}			+5V DC supply
24	CLK	Clock	I	2-MHz fixed frequency clock signal (1-MHz for mini-floppy disk).
19	$\overline{MR}$	Master Reset	I	Signal for resetting the FDC.
22	$\overline{TEST}$	Test	I	Signal for setting the FDC into a test mode.
1, 40	NC	Non Connection	—	These pins are not used.

MPU INTERFACE PINS

37	$\overline{DDEN}$	Double Density	I	Signal for selecting a FDC operation mode: When $\overline{DDEN}$ = 0, the double density operation mode is selected. When $\overline{DDEN}$ = 1, the single density operation mode is selected. This input must be fixed while the FDC is in busy state.
3	$\overline{CS}$	Chip Select	I	Signal for controlling the DALs: When $\overline{CS}$ = 0, the DALs are activated and data transfer between the FDC and the MPU is enabled. When $\overline{CS}$ = 1, the DALs are in high impedance state and data transfer is inhibited. (i.e., $\overline{RE}$ and $\overline{WE}$ are ignored.)
4	$\overline{RE}$	Read Enable	I	Strobe signal provided when data is read from internal registers: When $\overline{CS}$ = $\overline{RE}$ = 0, data can be read from internal registers.
2	$\overline{WE}$	Write Enable	I	Strobe signal provided when data is written into internal registers: When $\overline{CS}$ = $\overline{WE}$ = 0, data can be written internal registers.
5, 6	A_0, A_1	Register Select Line	I	Signal for addressing an internal register among Command Register (CR), Status Register (STR), Track Register (TR), Sector Register (SCR) and Data Register (DR): Refer to table of REGISTER SELECTION (p. 6).
7 ~ 14	$\overline{DAL_0}$ ~ $\overline{DAL_7}$ DAL_0 ~ DAL_7	Data Access Line	I/O	8-bit bidirectional bus for transferring 8-bit data between the FDC and the MPU. MB8876A: negative logic/MB8877A: positive logic.
38	DRQ	Data Request	O	Signal for informing the MPU of a DR status: Read operation: DRQ = 1 shows the DR is filled with a 8-bit data from a disk, and the FDC is requesting for the MPU to read the data. Write operation: DRQ = 1 shows the DR is empty, and the FDC is requesting for the MPU to write the next data into the DR.
39	IRQ	Interrupt Request	O	Interrupt signal to the MPU: IRQ is set when a Command is completed or the TYPE IV Command is executed. IRQ is reset when the next Command is written or the STR is read.

FLOPPY DISK INTERFACE PINS

Disk Head Control Signal

15	STEP	Step Move	O	Step pulse signal for moving a disk head.
16	DIRC	Direction	O	Signal for indicating a direction of disk head moving to the FDD: DIRC = 0 shows the head moves toward outside. DIRC = 1 shows the head moves toward inside.
28	HLD	Head Load	O	Signal for loading a disk head: When HLD = 1, the head is engaged on the disk. When HLD = 0, the head is released from the disk.

Disk Head Control Signal (Continued)

Pin No.	Symbol	Pin Name	I/O	Description
23	HLT	Head Load Timing	I	Signal for informing a disk head status: HLT = 1 shows a disk head is in an enagaged state. HLT is set when a disk head has been settled or a head settle time pre-determined by one shot circuit has elapsed after HLD = 1.
34	$\overline{\text{TR00}}$	Track 00	I	Signal for informing whether a disk head is positioned on Track No. 00 or not: $\overline{\text{TR00}}$ = 0 shows Track No. 00 is detected during track seaking operation.
32	READY	Ready	I	Signal for informing the FDC of a disk drive status: READY = 1 shows the disk drive is ready for operation, and only when READY = 1, read/write operation for disk can be executed. READY = 0 shows the disk drive is not ready, and neither read/write operation cannot be executed. However, seek operation is executed regardless of this signal.
35	$\overline{\text{IP}}$	Index Pulse	I	Signal for informing the FDC of an index hole of disk being detected in the FDD.

Disk Read Operation Signal

25	RG	Read Gate	O	Signal for informing synchronization between RCLK and $\overline{\text{RAWREAD}}$ to an external VFO circuit: RG = 1 show the FDC has found out a SYNC byte during disk reading operation.
26	RCLK	Read Clock	I	A data window signal which is generated in an external VFO circuit out of Read Data.
27	$\overline{\text{RAWREAD}}$	Raw Read	I	A raw read data signal transferred from the FDD.

Disk Write Operation Signal

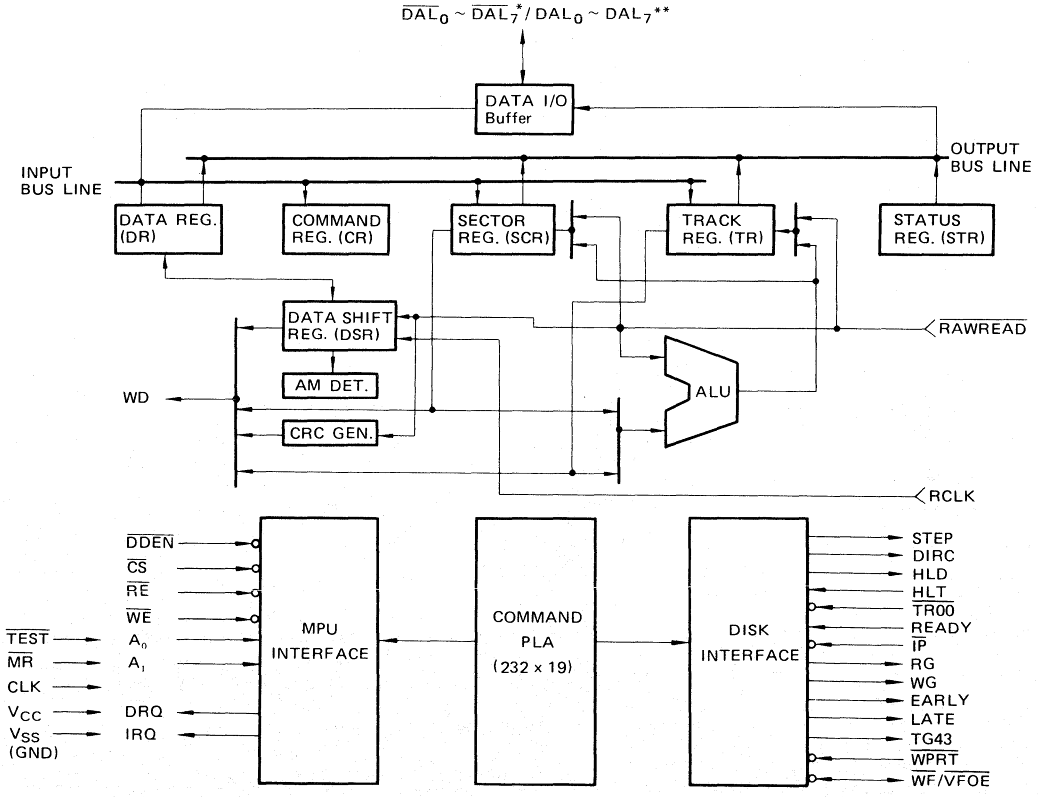
30	WG	Write Gate	O	Signal for indicating data is being written into a disk.
17	EARLY	Early Shift	O	Signal for indicating early pre-compensation of data write timing to a disk: EARLY = 1 shows a serial data to be transmitted via the WD pin to a disk must be shifted earlier.
18	LATE	Late Shift	O	Signal for indicating later pre-compensation of data write timing to a disk: LATE = 1 shows a serial data to be transmitted via the WD pin to a disk must be shifted later.
31	WD	Write Data	O	A write data signal transferred to the FDD.
29	TG43	Track Greater Than 43	O	Signal for indicating a head position of a disk: TG43 = 1 shows the head is located on any Track No. 44 thru 76. TG43 = 0 shows the head is located on any Track No. 0 thru 43.
33	$\overline{\text{WF}}/\overline{\text{VFOE}}$	Write Fault/Variable Frequency Oscillator Enable	I/O	Input signal for informing a fault is detected during write operation for a disk (during WG = 1). Output signal for informing the FDC is reading a disk (during WG = 0).
34	$\overline{\text{WPRT}}$	Write Protect	I	Signal for inhibiting write operation for disk.

REGISTER SELECTION

Chip Select	Address		Selected Register		Data Access Line Status
$\overline{CS}$	A_1	A_0	Read Mode ($\overline{RE}$ = 0)	Write Mode ($\overline{WE}$ = 0)	$\overline{DAL_7} \sim \overline{DAL_0}$ $DAL_7 \sim DAL_0$
1	*	*	Deselected	Deselected	High Impedance
0	0	0	Status Register (STR)	Command Register (CR)	Enabled
0	0	1	Track Register (TR)	Track Register (TR)	Enabled
0	1	0	Sector Register (SCR)	Sector Register (SCR)	Enabled
0	1	1	Data Register (DR)	Data Register (DR)	Enabled

*: Don't care

MB8876A/MB8877A BLOCK DIAGRAM



* MB 8876A: Negative Logic
** MB 8877A: Positive Logic

FUNCTIONAL BLOCK DESCRIPTION

INTERNAL REGISTERS

- **Command Register (CR)**
  An 8-bit write-only register, holds the command which is being executed. This register should not be loaded when the BUSY flag is set (BUSY = 1) unless the execution of the current command is to be overridden, using the Force Interrupt command.
- **Status Register (STR)**
  An 8-bit read-only register, holds the device status information. The contents of STR are automatically updated according to the status of the executing Command. After the STR is read, the IRQ output is usually reset (IRQ = 0) except for the Type IV Command.
- **Data Register (DR)**
  An 8-bit read/write used as a holding register during Disk Read and Write operations. In Disk Read operations, the serial data assembled in the Data Shift Register is transferred to the DR, where it is made available to the data bus. In Disk Write operations, parallel data from the data bus is written into the DR where it is transferred to Data Shift Register. In a Seek Command, the data written into the DR holds the address of the desired Track address.
- **Data Shift Register (DSR)**
  An 8-bit shift register which cannot be accessed directly through the data bus. The DSR assembles serial data from the RAW READ input during Read operations and transfers the data to the DR. In Write operations, the DSR receives data from the DR and serially transfers it out through the WRITE DATA output.
- **Track Register (TR)**
  An 8-bit read/write register, holds the track number of the current disk head position for Restore, Seek, Step, Step-In and Step-Out Commands (i.e. TYPE 1 Commands), and is updated during the Command execution. The TR contents are compared with the track number (recorded in the disk's ID field) during Read, Write, and Verify operations. The TR should not be written to when the device is busy (BUSY = 1).
- **Sector Register (SCR)**
  An 8-bit read/write register, holds the address of the desired sector number. The sector number is written into the SCR prior to the Read and Write Data Command execution. It should not be written to during busy (BUSY = 1). Executing the Read Address Command causes the SCR to be loaded with the track number from the ID field.

OTHER FUNCTIONAL BLOCKS

- **Cycle Redundancy Check (CRC) Logic**
  This logic is used for checking or generating the 16-bit Cycle Redundancy Check that is in the ID and Data fields used for error detection. The polynominal is: G(X) = X16 + X12 + X5 + 1.
- **Arithmetic/Logic Unit (ALU)**
  The ALU is a serial comparator, incrementer, and decrementer used for register comparisons and modifications with the disk record ID fields.
- **Address Mark (AM) Detection Circuit**
  A circuit to detect specific bit pattern data in the serial data from a disk (i.e. Index Mark, ID Address Mark, Data Address Mark).
- **Data Modulator**
  A circuit to modulate data to be written onto a disk in the specific recording format: Single density recording format: Frequency Modulation (FM) Double density recording format: Modified Frequency Modulation (MFM)
- **Programmable Logic Array (PLA) for Commands**
  A micro-program to generate control signals (Commands) which control the FDC operation: The size of micro-program is approximately 232 x 19 bits.

BIT STRUCTURES OF COMMANDS

MB8876A/MB8877A

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

NOTE: Bits shown in TRUE form.

TABLE 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{\text{DDEN}}$	0	1	0	1	X	X
R1 R0	$\overline{\text{TEST}}$ = 1	$\overline{\text{TEST}}$ = 1	$\overline{\text{TEST}}$ = 1	$\overline{\text{TEST}}$ = 1	$\overline{\text{TEST}}$ = 0	$\overline{\text{TEST}}$ = 0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

TYPE I COMMANDS

h = Head Load Flag (Bit 3)
h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)
V = 1, Verify on destination track
V = 0, No verify

$r_1 r_0$ = Stepping motor rate (Bits 1-0)
Refer to Table 1 for rate summary

u = Update flag (Bit 4)
u = 1, Update Track register
u = 0, No update

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)
m = 0, Single Record
m = 1, Multiple Records

a_0 f = Data Address Mark (Bit 0)
a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)
E = 1, 15 ms delay
E = 0, no 15 ms delay

S = Side Select Flag
S = 0, Compare for Side 0
S = 1, Compare for Side 1

C = Side Compare Flag
C = 0, diable side select compare
C = 1, enable side select compare

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)
I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to No-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
$I_3 - I_0$ = 0, Terminate with no Interrupt

STATUS REGISTER SUMMARY

Command	Status Bit							
	7	6	5	4	3	2	1	0
All Type I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
Read Sector	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
Write Sector	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
Read Address	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
Read Track	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
Write Track	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

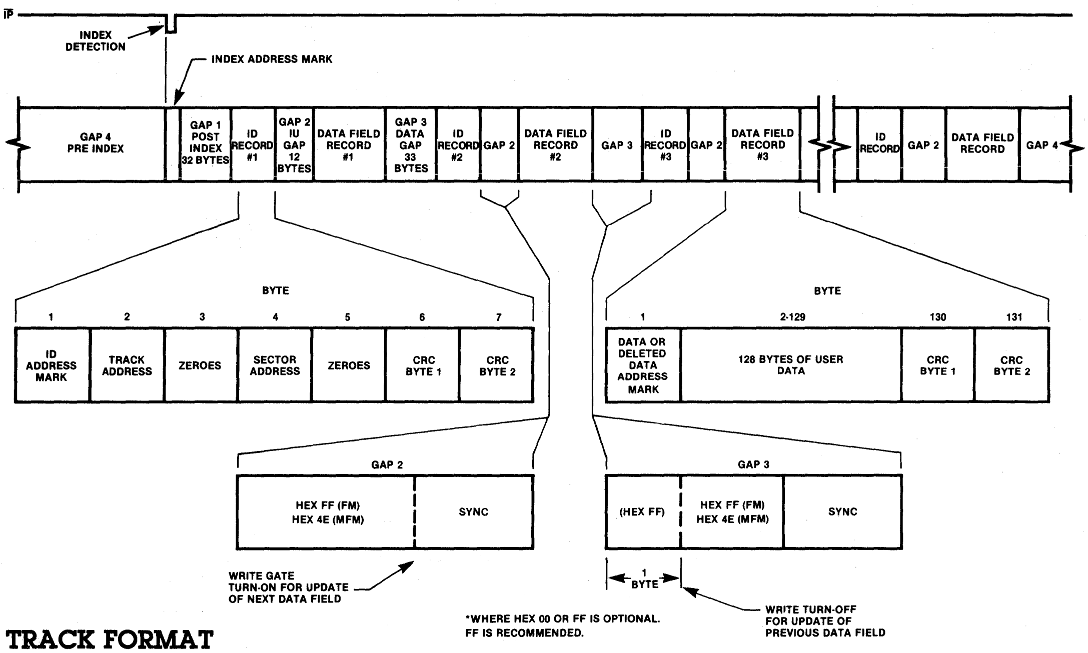
STATUS DESCRIPTION FOR TYPE I COMMANDS

Bit	Name	Meaning
S7	Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6	Protected	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5	Head Loaded	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	Seek Error	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC Error	CRC encountered in ID filed.
S2	Track 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1	Index	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	Busy	When set command is in progress. When reset no command is in progress.

STATUS DESCRIPTION FOR TYPE II AND III COMMANDS

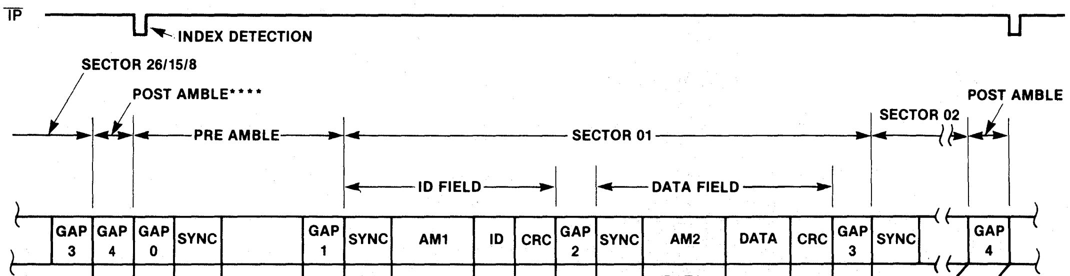
Bit	Name	Meaning
S7	Not Ready	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	Write Protect	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	Record Type/ Write Fault	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	Record Not Found (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC Error	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	Lost Data	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	Data Request	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	Busy	When set, command is under execution. When reset, no command is under execution.

TRACK FORMAT



*WHERE HEX 00 OR FF IS OPTIONAL. FF IS RECOMMENDED.

TRACK FORMAT



		GAP 0	SYNC	INDEX ADDRESS MARK		GAP 1	SYNC	ID ADDRESS MARK		ID	CRC	GAP 2	SYNC	DATA or DELETED DATA MARK		DATA	CRC	GAP 3	GAP 4	
SINGLE DENSITY (FM)	BYTE No's	40	6	1		26	6	1		4	2	11	6	1		128 256 512	2	27 42 58	247 170 311	26 15 8 (Sector/Track)
(FM)	DATA	FF	00	FC*		FF	00	FE*		**	***	FF	00	FB* or F8*		(DATA)	***	FF	FF	
DOUBLE DENSITY (MFM)	BYTE No's	80	12	3	1	50	12	3	1	4	2	22	12	3	1	256 512 1024	2	54 84 116	598 400 654	26 15 8 (Sector/Track)
(MFM)	DATA	4E	00	C2*	FC	4E	00	A1*	FE	**	***	4E	00	A1*	FB or F8	(DATA)	***	* 4E	4E	

NOTE: *: Shows to have missing clock.
**: Shows the ID field
***: Shows the cyclic Redundancy check polynomial $G(X) = X^{\circ} + X^{5} + X^{12} + X^{16}$
****: See the most right column for its byte numbers and data.

SECTOR FORMAT

SECTOR															
ID FIELD									DATA FIELD						
SYC	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP 2	SYNC	DATA AM	DATA	CRC 1	CRC 2	GAP 3	
6 bytes	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	11 bytes	6 bytes	1 byte	*	1 byte	1 byte	27/42/58 bytes	(FM) or
12 bytes	4 bytes	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	22 bytes	12 bytes	4 byte	*	1 byte	1 byte	54/84/116 bytes	(MFM)

SECTOR LENGTH:
(00)H** for 128 Bytes/Sector data
(01)H for 256 Bytes/Sector data
(02)H 412 Bytes/Sector data
(03)H for 1024 Bytes/Sector data

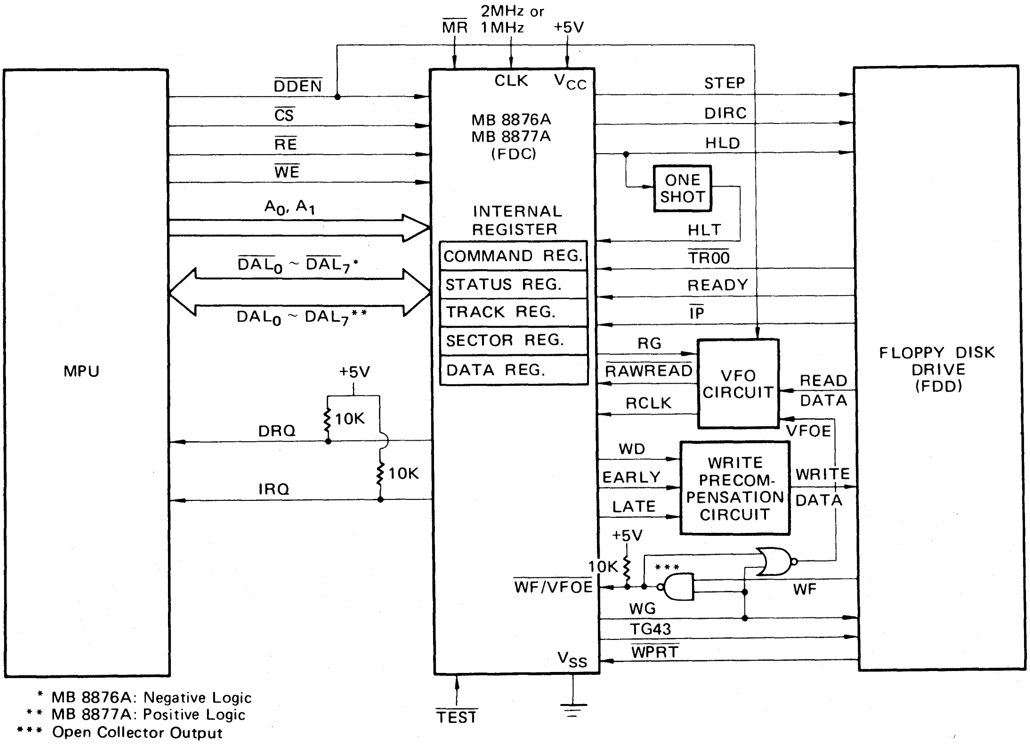
SECTOR NUMBER:
(01)H to (1A)H for 26 Sector/Track format
(01)H to (0F)H for 15 Sector/Track format
(01)H to (08)H for 8 Sector/Track format

SIDE NUMBER:
(00)H for Side 0 of single-side of double-side disk
(01)H for Side 1 of double-side disk

TRACK NUMBER:
(00)H to (4A)H for Track 0 thru Track 74***

NOTE *: Byte number of this column is defined in the SECTOR LENGTH column.
**: "H" after parentheses show that the parenthesized figures are hexa-decimal.
***: Track 75 and 76 are usually used for correction.

MB8876A/MB8877A TYPICAL SYSTEM CONSTRUCTION



* MB 8876A: Negative Logic
** MB 8877A: Positive Logic
*** Open Collector Output

IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown below.

ONE SECTOR [1]

Data Byte (hex)	No. of Bytes	Comments
FF	40	Gap 5 Post Index)
00	6	
FC	1	Index AM
FF	26	Gap 1
00	6	
FE	1	ID AM
XX	1	Track Number (00-4A)
0X	1	Side Number (00 or 01)
XX	1	Sector Number (01-1A)
00	1	Sector Length (128 bytes)
F7	1	Causes 2-Byte CRC to be Written
FF	11	Gap 2 (ID Gap)
00	6	
FB	1	Data AM
E5	128	Data Field
F7	1	Causes 2-Byte CRC to be Written
FF	27	Part of Gap 3 (Data Gap)
FF	247[2]	Gap 4 (Pre-Index)

Notes: 1. This pattern must be written 26 times per track.
2. Continue writing Hex FF until FDC completes sequence and generates INTRQ interrupt.

IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown below.

ONE SECTOR [1]

Data Byte (hex)	No. of Bytes	Comments
4E	80	Gap 5 (Post Index)
00	12	
F6	3	Writes C2
FC	1	Index AM
4E	50	Gap 1
00	12	
F5	3	Writes ID AM Sync Bytes
FE	1	ID AM
XX	1	Track Number (00-4C)
0X	1	Side Number (00 or 01)
XX	1	Sector Number (01-1A)
01	1	Sector Length (256 Bytes)
F7	1	Causes 2-Byte CRC to be Written
4E	22	Gap 2 (ID Gap)
00	12	
F5	3	Writes ID AM Sync Bytes
FB	1	Data AM
40	256	Data Field
F7	1	Causes 2-Byte CRC to be Written
4E	54	Part of Gap 3 (Data Gap)
4E	598[2]	Gap 4 (Pre Index)

Notes: 1. This pattern must be written 26 times per track.
2. Continue writing Hex 4E until FDC completes sequence and generates INTRQ interrupt.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin	V_{CC}, V_{IN}, V_{OUT}	V_{SS} −0.3 to V_{SS} +7.0	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.75	5.00	5.25	V	0°C to +70°C
	V_{SS}	—	0	—		
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	0.8	V	

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output High Voltage (I_{OH} = −200μA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 1.8mA)	V_{OL}	—	—	0.4	V
Three-State (Off-State) Input Current (V_{IN} = 0.4V to 2.4)	I_{TSI}	—	—	10	μA
Input Leakage Current (See Note 1)	I_{IN1}	—	—	2.5	μA
Input Leakage Current (See Note 2)	I_{IN2}	—	—	100	μA
Output Leakage Current for Off-State (V_{OH} = 2.4V)	I_{LOH}	—	—	10	μA
Power Consumption	P_D	—	—	350	mW

Note1) Except for HLT, $\overline{\text{TEST}}$, $\overline{\text{WF}}$, $\overline{\text{WPRT}}$, and $\overline{\text{DDEN}}$. (V_{IN} = 0 to 5.25V)
2) For HLT, $\overline{\text{TEST}}$, $\overline{\text{WF}}$, $\overline{\text{WPRT}}$, and $\overline{\text{DDEN}}$. (V_{IN} = 0 to 5.25V)

AC CHARACTERISTICS

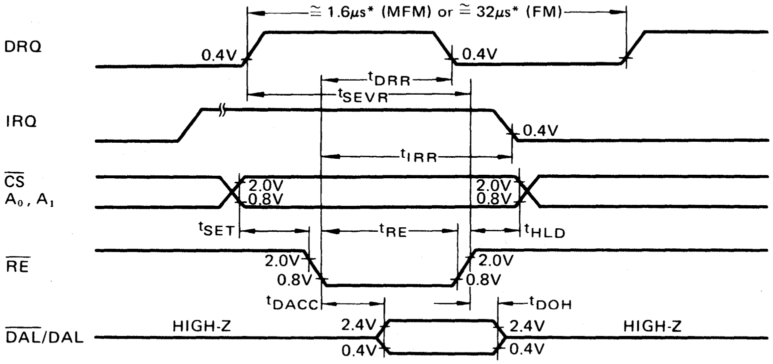
(Recommended Operating Conditions unless otherwise noted.)

MPU Read Timing (From FDC)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{SET}	50	—	—	ns
Address Hold Time	t_{HLD}	10	—	—	ns
$\overline{RE}$ Pulse Width	t_{RE}	280	—	—	ns
DRQ Reset Time	t_{DRR}	—	—	250	ns
IRQ Reset Time	t_{IRR}	—	—	500	ns
Data Delay Time (C_L = 25pF)	t_{DACC}	—	—	250	ns
Data Hold Time (C_L = 25pF)	t_{DOH}	50	—	150	ns
DRQ Service Time (RCLK·Cycle = 2μs)	t_{SEVR}	—	—	13.5*	μs

*: These values are doubled when CLK = 1MHz.

READ TIMING

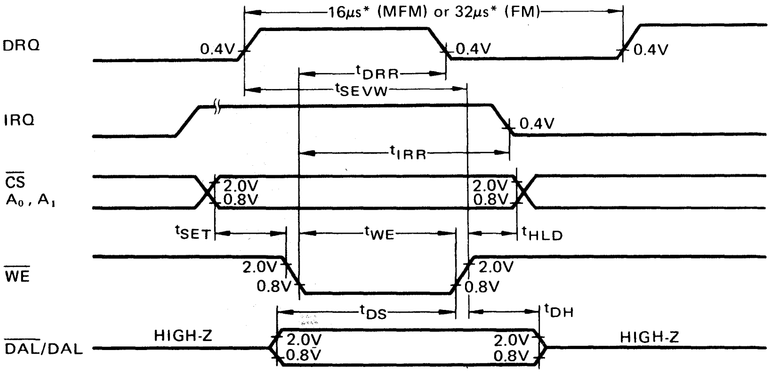


MPU Write Timing (To FDC)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{SET}	50	—	—	ns
Address Hold Time	t_{HLD}	10	—	—	ns
$\overline{WE}$ Pulse Width	t_{WE}	200	—	—	ns
DRQ Reset Time	t_{DRR}	—	—	250	ns
INTRQ Reset Time	t_{IRR}	—	—	500	ns
Data Setup Time	t_{DS}	250	—	—	ns
Data Hold Time	t_{DH}	0	—	—	ns
DRQ Service Time ($\overline{DDEN}$ = "L")	t_{SEVW}	—	—	11.5*	μs

*: These values are doubled when CLK = 1MHz.

WRITE TIMING



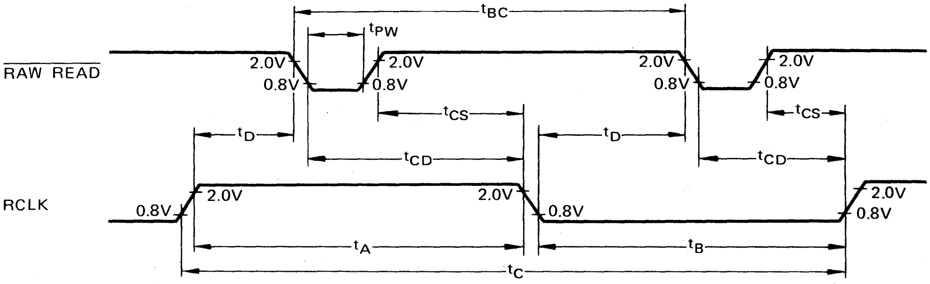
*: These values are doubled when CLK = 1MHz.

FDC Read Data Timing (From Disk)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
$\overline{\text{RAWREAD}}$ Pulse Width		t_{PW}	100	—	250*	ns
Clock Setup Time		t_D	40	—	—	ns
Clock Hold Time for MFM		t_{CD}	40	—	—	ns
Clock Hold Time for FM		t_{CS}	40	—	—	ns
$\overline{\text{RAWREAD}}$ Cycle Time	MFM	t_{BC}	—	2*, 3* or 4*	—	μs
	FM		—	2* or 4*	—	μs
RCLK High Pulse Width	MFM	t_A	0.8	1*	20	μs
	FM		0.8	2*	20	μs
RCLK Low Pulse Width	MFM	t_B	0.8	1*	20	μs
	FM		0.8	2*	20	μs
RCLK Cycle Time	MFM	t_C	—	2*	—	μs
	FM		—	4*	—	μs

*: These values are double when CLK = 1MHz.

READ DATA TIMING



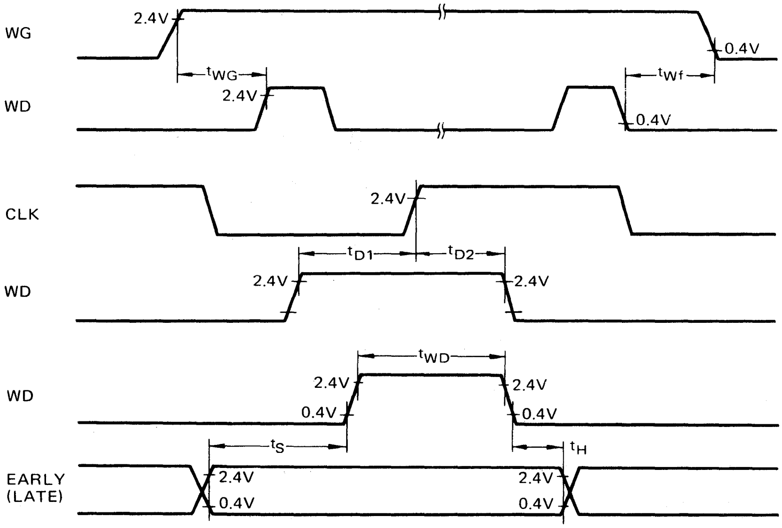
FDC Write Data Timing (To Disk)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Write Data Pulse Width	t_{WD}**	CLK = 2 MHz	FM	450	500	550	ns
			MFM	150	200	250	
Write Gate To Write Data	t_{WG}**	CLK = 2 MHz	FM	—	2	—	μs
			MFM	—	1	—	
Write Gate off from WD	t_{WF}**	CLK = 2 MHz	FM	—	2	—	μs
			MFM	1	—	2	
Early (Late) to Write Data	t_S	CLK = 2 MHz	MFM	125	—	—	ns
Early (Late) from Write Data	t_H	CLK = 2 MHz	MFM	−50*	—	—	ns
WD Valid to CLK	t_{D1}	CLK = 1 MHz	MFM	200	—	—	ns
		CLK = 2 MHz	MFM	30	—	—	
WD Valid after CLK	t_{D2}	CLK = 1 MHz	MFM	50	—	—	ns
		CLK = 2 MHz	MFM	50	—	—	

*: This value, −50ns (min) indicated that Early (Late) signal changes 50ns (min) before WD falls down in worst case. See DISK DATA OUTPUT TIMING.

**: All times are doubled when CLK = 1 MHz.

WRITE DATA TIMING

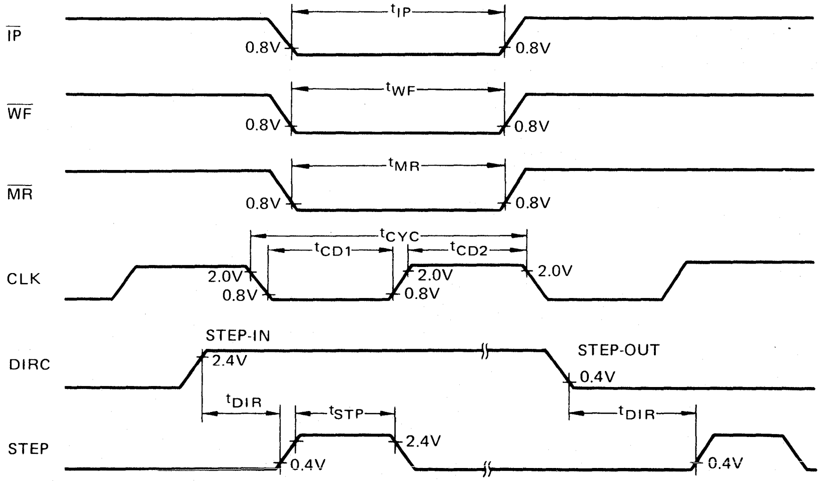


OTHER TIMINGS

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
CLK Low Pulse Width		t_{CD1}	230	—	20000	ns
CLK High Pulse Width		t_{CD2}	200	—	20000	ns
STEP Pulse Width	MFM	t_{STP}	2*	—	—	μs
	FM		4*	—	—	μs
DIRC Setup Time		t_{DIR}	12*	—	—	μs
$\overline{\text{MR}}$ Pulse Width**		t_{MR}	50*	—	—	μs
$\overline{\text{IP}}$ Pulse Width		t_{IP}	10*	—	—	μs
$\overline{\text{WF}}$ Pulse Width		t_{WF}	10*	—	—	μs
CLK Cycle Time		t_{CYC}	—	0.5*	—	μs

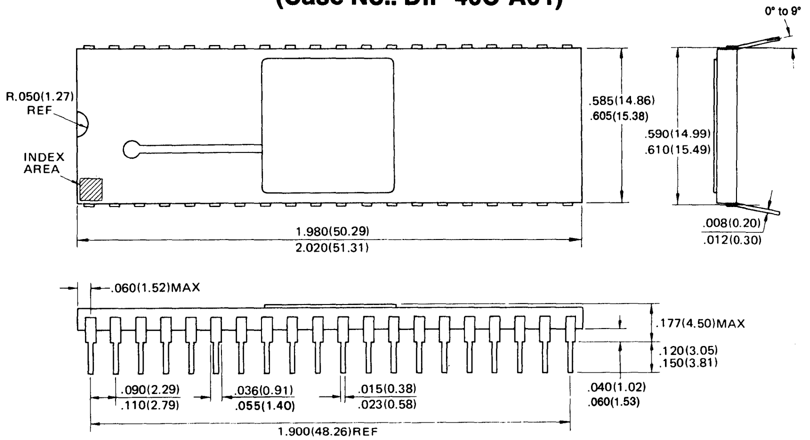
*: These Values are doubled when CLK = 1MHz.
**: During Master Reset, CLK of more than 10 cycles are required.

OTHER TIMINGS

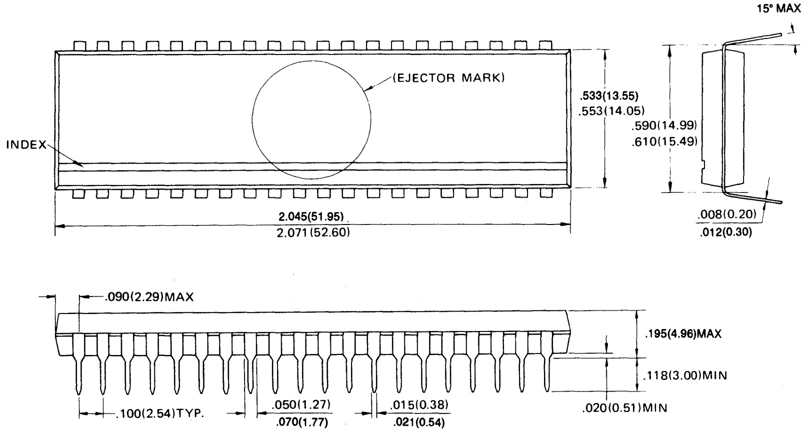


PACKAGE DIMENSIONS Dimensions in inches (millimeters)

40-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE (Case No.: DIP-40C-A01)



40-LEAD PLASTIC DUAL IN-LINE PACKAGE (Case No.: DIP-40P-M01)



Preliminary

Advanced Products

FUJITSU

MB89311
CMOS Floppy Disk Controller/Formatter

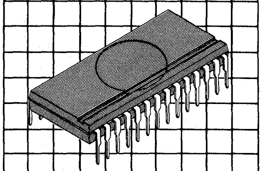
October 1986
Edition 1.0

Description

The Fujitsu MB89311 is a floppy disk controller/formatter (FDC) designed as an enhanced version of the conventional MB8877A.

The MB89311 is designed based on the MB8877A architecture. Some inconveniences of the MB8877A are eliminated on the MB89311, and several new commands are added. It can support micro- (3" or 3.5" double-density), mini- (5.25" double-density), and standard (8" single- or double-density), floppy disk drives. When combined with the MB4107 variable frequency oscillator (VFO), an economical floppy disk drive interface can be created with a minimum of parts.

The MB89311 is fabricated by the silicon-gate CMOS process, and packaged in a 28-pin plastic DIP. It has TTL compatible inputs/outputs. Operation is with a single +5V power supply with low power consumption.



Plastic DIP
(DIP-28P-M02)

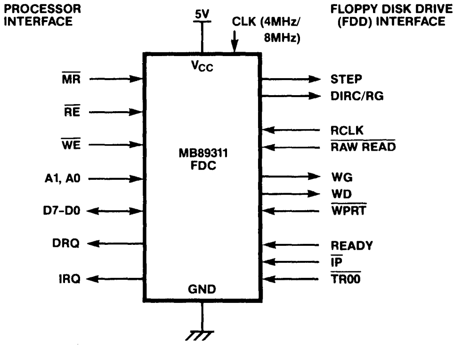
Features

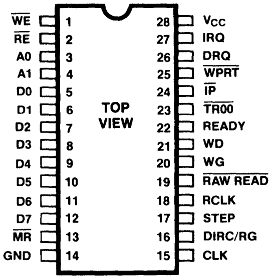
- **Single +5V power supply**
- **TTL compatible I/O**
- **IBM & ISO compatible disk formats**
- **Track seeking with automatic verification**
- **Multiple-sector read/write operation**
- **Track read/write/initialize operation**
- **Program/DMA data transfer**
- **Single density/double density**

Enhancements

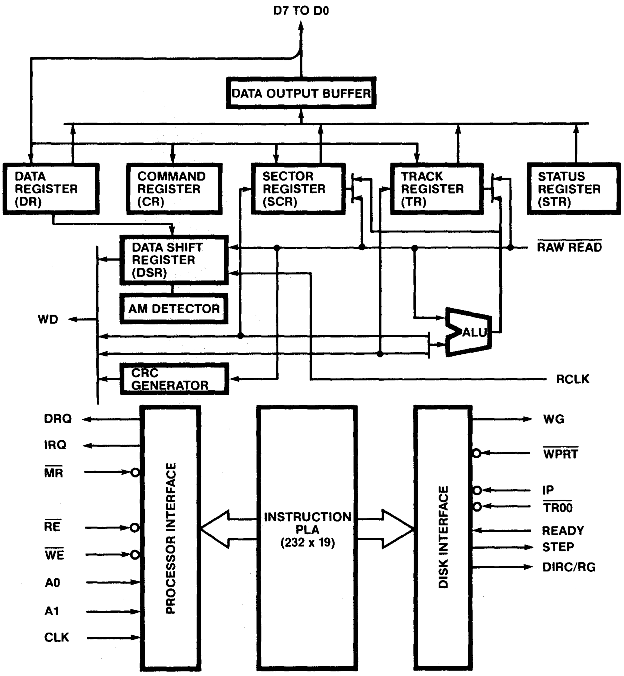
- **Silicon-gate CMOS process**
- **28-pin plastic DIP (Suffix -P)**
- **Built-in programmable write precompensation (125ns/250ns for all tracks at CLK = 8MHz, 250ns/500ns at CLK = 4MHz)**
- **For lost data error, abnormal termination after sector read or write completion**
- **Extended mode commands: Read-after-seek, write-after-seek, delay, and format commands are added.**
- **No restrictions on the RCLK frequency in gap between ID and data fields.**
- **Step rate: 1ms to 30ms, Settling time: 15ms to 60ms**
- **Record length: 128, 256, 512, 1024, 2048, 4096, and 8192 bytes/sector**

Logic Symbol and Pin Assignment





Block Diagram



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Pin Descriptions

The MB89311 FDC has two interfaces: One is the processor interface; $\overline{\text{MR}}$, $\overline{\text{RE}}$, $\overline{\text{WE}}$, and A1 & A0 inputs, D7-D0 inputs/outputs, and DRQ & IRQ outputs which are used for the processor to control the FDC. The other is the floppy disk drive (FDD) interface; STEP, DIREC/RG, WG, and $\overline{\text{WD}}$ outputs, and RCLK, $\overline{\text{RAW READ}}$, WPRT, READY, $\overline{\text{TR00}}$, $\overline{\text{IP}}$ inputs, which are used for the FDC to control the FDD.

	Symbol	Number	Type	Name & Function
Power Supply & Clock	V_{CC}	28	—	+5Vdc power supply pin.
	V_{SS}	14	—	Power supply ground pin.
	CLK	15	I	Clock input: Basic timing clock for internal circuits. 8MHz and 4MHz frequencies are required for 500K bits/s data transfer rate in MFM (250K bits/s in FM) and 250K bits/s in MFM (125K bits/s in FM). The CLK signal is required also during a reset.
Processor Interface	$\overline{\text{MR}}$	13	I	Master Reset: A low level on this pin stops FDC operation, and initializes its internal state. The CLK signal is required also during a reset.
	$\overline{\text{RE}}$	2	I	Read Enable: Strobe signal for reading data from the internal register addressed by A1 and A0.
	$\overline{\text{WE}}$	1	I	Write Enable: Strobe signal for writing data into the internal register addressed by A1 and A0.
	A1, A0	4, 3	I	Register Select Line: Signal for addressing an internal register (CR, STR, TR, SCR, or DR).
	D7-D0	12-5	I/O	Data Access Line: 8-bit bidirectional three-state data bus. These lines go to a high impedance state when $\overline{\text{RE}}$ and $\overline{\text{WE}}$ are high.
	DRQ	26	O	Data Request: Notifies the processor when new data must be read from or written into the data register. This pin is an open-drain output and must be pulled up by an external 10kΩ resistor.
	IRQ	27	O	Interupt Request: Set when a command completes, terminates, or a force interrupt command is specified. This pin is an open-drain output and must be pulled up by an external 10kΩ resistor. Undefined at power-on.
Floppy Disk Drive Interface	STEP	17	O	Step: Signal for moving disk head. One pulse is generated to move the head by one track.
	DIRC/RG	16	O	Direction/Read Gate: During disk head operations, when this signal is low, the head moves to the outside, and when high, to the inside. During read operations, when this signal is high, it indicates that read data has been synchronized.
	RCLK	18	I	Read Clock: A data window signal for the raw read data from disk. This signal is generated by an external VFO circuit.
	$\overline{\text{RAW READ}}$	19	I	Raw Read Data: Serial raw data read from disk, containing clock and data bits.
	WG	20	O	Write Gate: This signal is high when valid data is being written to disk.
	WD	21	O	Write Data: Serial write data pulses to be written to disk.
	$\overline{\text{WPRT}}$	25	I	Write Protect: Signal for inhibiting write operation to disk. When this signal is low, write operation is disabled.
	READY	22	I	Ready: When this signal is high, the disk drive is ready for operation. Commands except for Type I commands can be executed if this signal is high.
	$\overline{\text{TR00}}$	23	I	Track 00: When this signal is low, it indicates that the disk head is positioned at track 00.
	$\overline{\text{IP}}$	24	I	Index Pulse: Pulsed low each time the index hole of the floppy disk is detected.

Functional Description

Register Set

The MB89311 FDC contains the following five registers to execute commands and indicate status:

- Command register (CR)
- Status register (STR)
- Track register (TR)
- Sector register (SR)
- Data register (DR)

Register Selection

A1	A0	Read Mode ($\overline{\text{RE}}$ = 0)	Write Mode ($\overline{\text{WE}}$ = 0)
0	0	Status register	Command register
0	1	Track register	Track register
1	0	Sector register	Sector register
1	1	Data register	Data register

These registers are addressed by register select lines A1 and A0 under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control.

Command Words

The FDC's operations are defined by commands, that are divided into four groups: Types I, II, III, and IV. Each group contains one to five command(s). Each command has flags that define detailed operation of the command.

The FDC has two command modes, the 8877 mode (which emulates the MB8877 command set) and the extended mode (in which additional commands can be used). Either of these two modes can be selected by the assign command.

Command Summary (1): 8877 Mode Command Set

Type	Name	Code								Function
		MSB							LSB	
I	Restore	0	0	0	0	X	V	r1	r0	Moves head to track 0.
	Seek	0	0	0	1	X	V	r1	r0	Moves head to a desired track.
	Step	0	0	1	u	X	V	r1	r0	Moves head one track.
	Step-in	0	1	0	u	X	V	r1	r0	Moves head one track to inside.
	Step-out	0	1	1	u	X	V	r1	r0	Moves head one track to outside.
II	Read data	1	0	0	m	S	E	C	L	Reads data (data field) from disk.
	Write data	1	0	1	m	S	E	C	a0	Writes data (data field) to disk.
III	Read address	1	1	0	0	0	E	0	0	Reads ID field from disk.
	Read track	1	1	1	0	0	E	0	0	Reads all data from one track.
	Write track	1	1	1	1	0	E	0	0	Writes all data to one track.
IV	Assign parameter	1	1	1	1	1	1	0	1	Selects operation timing.
	Assign mode	1	1	1	1	1	1	1	0	Selects operation mode.
	Force interrupt	1	1	0	1	I3	I2	I1	I0	Generates interrupt (IRQ).

Functional Description
(Continued)

Command Summary (2): Extended Mode Command Set

Type	Name	Code MSB							LSB	Function
I	Restore	0	0	0	0	0	V	0	0	Moves head to track 0.
	Seek	0	0	0	1	0	V	0	0	Moves head to a desired track.
	Step	0	0	1	u	0	V	0	0	Moves head one track.
	Step-in	0	0	1	u	0	V	0	1	Moves head one track to inside.
	Step-out	0	0	1	u	0	V	1	0	Moves head one track to outside.
II	Read-after-seek	0	1	0	0	S	1	C	L	Reads one sector data after seek.
	Write-after-seek	0	1	1	0	S	1	C	a0	Writes one sector data after seek.
	Read data	1	0	0	m	S	E	C	L	Reads data (data field) from disk.
	Write data	1	0	1	m	S	E	C	a0	Writes data (data field) to disk.
III	Read address	1	1	0	0	0	E	0	0	Reads ID field from disk.
	Read track	1	1	1	0	0	E	0	0	Reads all data from one track.
	Write track	1	1	1	1	0	E	0	0	Writes all data to one track.
	Format	1	1	1	1	0	E	0	1	Formats disk.
IV	Delay	1	1	1	1	1	1	0	0	Generates interrupt after a set time.
	Assign parameter	1	1	1	1	1	1	0	1	Selects operation timing.
	Assign mode	1	1	1	1	1	1	1	0	Selects operation mode.
	Reset	1	1	1	1	1	1	1	1	Resets FDC.
	Force interrupt	1	1	0	1	I3	I2	I1	I0	Generates interrupt (IRQ).

Flag Summary

Type	Symbol	Function
I	u	Update of track register
	V	Verify at destination track
	r1, r0	Step rate of STEP pulse
II	m	Multiple sectors
	S	Side number
	a0	Data address mark
III	C	Side compare
	L	Long read (CRC read)
IV	I3–I0	Interrupt

Functional Description

Status Words

Status words, which are automatically held in the status register, show the status of the executing command, executed command, and conditions of the FDD. The system processor can monitor the FDC operations and FDD conditions, reading the status register.

When the FDC receives a command, the status register is automatically preset at the start of the command execution. Each status bit is internally updated (set or reset) during the command execution, and the status word is established at the completion of the command.

Status Word Summary

		Status Bit							
Command		**STR7**	**STR6**	**STR5**	**STR4**	**STR3**	**STR2**	**STR1**	**STR0**
Type I	All commands	Not Ready	Write Protect	1	Seek Error	CRC Error	Track 00	Index	Busy
Type II	Read data & Read-after-seek	Not Ready	D/M N/F	Rec. Type	Rec. N/F	CRC Error	Lost Data	Data Request	Busy
	Write data & Write-after-seek	Not Ready	0	0	Rec. N/F	CRC Error	Lost Data	Data Request	Busy
Type III	Read address	Not Ready	0	0	Rec. N/F	CRC Error	Lost Data	Data Request	Busy
	Read track	Not Ready	Write Protect	0	0	0	Lost Data	Data Request	Busy
	Write track	Not Ready	Write Protect	0	0	0	Lost Data	Data Request	Busy
	Format	Not Ready	Write Protect	0	0	Illegal Length	Lost Data	Data Request	Busy
Type IV	Force Interrupt	In accordance with the executing commands.							0
		Not Ready	Write Protect	0	0	0	Track 00	Index	0
	Reset command & Master reset	In accordance with Type I commands.							
	Delay, Assign Parameter & Mode	Not Ready	0	0	0	0	0	0	Busy

Notes: Rec. = Record, N/F = Not Found
D/M N/F = Data Mark Not Found. This status bit is valid in extended mode only. In 8877 mode, this bit is "0".

Functional Description (Continued)

Status Bit Function Summary

Command	Status	Status Bit	Function
Type I	Not Ready	STR7	1 = FDD is not ready: Not Ready = $\overline{\text{READY}}$ + MR.
	Write Protect	STR6	1 = Write operation is inhibited: Write Protect = WPRT.
	Seek Error	STR4	1 = Verify operation was unsuccessful.
	CRC Error	STR3	1 = CRC check error occurred.
	Track 00	STR2	1 = Disk head is positioned at track 0: Track 00 = TR00.
	Index	STR1	1 = Index hole was detected. Index = INP
	Busy	STR0	1 = FDC is executing a command.
Type II & Type III	Not Ready	STR7	1 = FDD is not ready. Not Ready = $\overline{\text{READY}}$ + MR.
	Write Protect	STR6	1 = Write operation is inhibited. Write Protect = WPRT.
	Data Mark Not Found*		1 = Data mark was not found within required byte interval after ID mark detection.
	Record Type	STR5	1 = Data address mark was deleted data mark.
	Record Not Found	STR4	1 = Desired track and sector were not found.
	CRC Error	STR3	1 = CRC check error occurred.
	Lost Data	STR2	1 = Data was not read from or written to data register within required time interval.
	Data Request	STR1	1 = DRQ is currently active. Data Request = DRQ.
	Busy	STR0	1 = FDC is executing a command.

*For read data and read-after-seek commands in extended mode only.

Absolute Maximum Ratings (Note)

		Rating			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Note**
Supply Voltage	V_{CC}	V_{SS}-0.3	V_{SS}+7.0	V	
	V_{SS}		0	V	
Input Voltage	V_{IN}	V_{SS}-0.3	V_{SS}+7.0	V	Should not exceed V_{CC}+0.5V
Output Voltage	V_{OUT}	V_{SS}-0.3	V_{SS}+7.0	V	Should not exceed V_{CC}+0.5V
Operating Temperature	T_A	-40	+85	°C	
Storage Temperature	T_{STG}	-55	+150	°C	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		Value				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}		0		V	
Operating Temperature	T_A	-40		+85	°C	

DC Characteristics

(Recommended operating conditions unless otherwise noted).
(V_{CC} = +5V ± 10%, GND = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	Value		Unit	Test Condition
		Min	Max		
Input Low Voltage	V_{IL}	-0.3	0.8	V	
Input High Voltage	V_{IH}	2.2	V_{CC}	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.5mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400μA
		V_{CC}-0.4		V	I_{OH} = -100μA
Input Leakage Current	I_{IL}	-10	+10	μA	0V ≤ V_{IN} ≤ V_{CC}
Output Leakage Current	I_{OFL}	-10	+10	μA	0V ≤ V_{OUT} ≤ V_{CC}
Standby Current	I_{CC}		10	mA	
Input Capacitance	C_{IN}		10	pF	V_{CC} = GND = 0V T_A = 25°C All pins except measured pin are 0V
Output Capacitance	C_{OUT}		20	pF	
I/O Capacitance	$C_{I/O}$		20	pF	

AC Characteristics

(Recommended operating conditions unless otherwise noted).
(V_{CC} = +5V ± 10%, GND = 0V, T_A = -40°C to +85°C)

CPU Read Timing (from FDC)

Parameter	Symbol	Value		Unit	Test Condition
		Min	Max		
Address Setup Time (to $\overline{RE}$↓)	t_{SET}	50		ns	
Address Hold Time (from($\overline{RE}$↑)	t_{HLD}	15		ns	
$\overline{RE}$ Pulse Width	t_{RE}	150		ns	
Data Delay Time (from $\overline{RE}$↓)	t_{DACC}		120	ns	C_L = 150pF
Data Hold Time (from $\overline{RE}$↑)	t_{DOH}	10	75	ns	C_L = 150pF
DRQ Service Time (from DRQ to $\overline{RE}$↑)	t_{SEVR}		13.5	μs	t_C = 2μs
DRQ Release Time (from $\overline{RE}$↓ to DQR↓)	t_{DRR}		150	ns	
IRQ Release Time (from $\overline{RE}$↓ to IRQ↓)	t_{IRR}		500	ns	

CPU Write Timing (to FDC)

Parameter	Symbol	Value		Unit	Test Condition
		Min	Max		
Address Setup Time (to $\overline{WE}$↓)	t_{SET}	50		ns	
Address Hold Time (from $\overline{WE}$↑)	t_{HLD}	10		ns	
$\overline{WE}$ Pulse Width	t_{WE}	100		ns	
Data Setup Time (to $\overline{WE}$↑)	t_{DS}	100		ns	
Data Hold Time (from $\overline{WE}$↑)	t_{DH}	0		ns	
DRQ Service Time (from DRQ to $\overline{WE}$↑)	t_{SEVW}		9.5*	μs	
DRQ Release Time (from $\overline{WE}$↓ to DQR↓)	t_{DRR}		150	ns	
IRQ Release Time (from $\overline{WE}$↓ to IRQ↓)	t_{IRR}		500	ns	

* This value is doubled when CLK = 4MHz.

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)
(V_{CC} = +5V ± 10%, GND = 0V, T_A = -40°C to +85°C)

FDC Read Timing (from FDD)

		Value				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
$\overline{\text{RAW READ}}$ Pulse Width	t_{PW}	100			ns	
$\overline{\text{RAW READ}}$ Cycle Time	t_{BC}		*2,*3,*4		μs	MFM
			*2, *4			FM
RCLK Setup Time (from RCLK Change to to $\overline{\text{RAW READ}}$↓)	t_D	40			ns	
RCLK Hold Time (from $\overline{\text{RAW READ}}$↓ to RCLK Change)	t_{CD}	40			ns	
RCLK High Time	t_A	0.8	1*	8	μs	MFM
		0.8	2*	8		FM
RCLK Low Time	t_B	0.8	1*	8	μs	MFM
		0.8	2*	8		FM
RCLK Cycle Time	t_C		2*		μs	MFM
			4*			FM

* These values are doubled when the CLK = 4MHz.

FDC Write Timing (to FDD)

		Value				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
WD Pulse Width	t_{WD}	450	500	550	ns	CLK=8MHz, FM
		200	250	300		CLK=8MHz, MFM
WG Setup Time (from WG↑ to WD↑)	t_{WG}		2		μs	CLK=8MHz, FM
			1			CLK=8MHz, MFM
WG Hold Time (from WD↓ to WG↓)	t_{WF}		2		μs	CLK=8MHz, FM
		1		2		CLK=8MHz, MFM
WD Output Delay	t_{CWD}	20		100	ns	

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)
(V_{CC} = +5V ± 10%, GND = 0V, T_A = -40° C to +85° C)

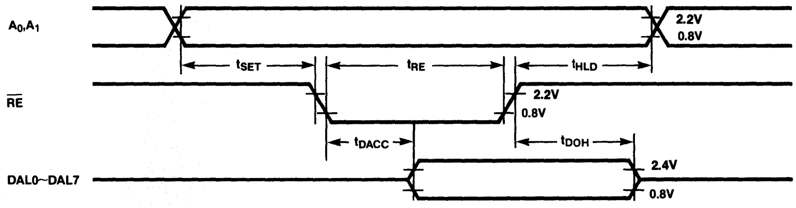
Other Timing

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Test Condition
CLK Cycle Time	t_{CYC}	125		500	ns	
CLK Low Time	t_{CD1}	55		250	ns	
CLK High Time	t_{CD2}	55		250	ns	
STEP Pulse Width	t_{STP}	6*			μs	MFM
		12*				FM
DIRC Setup Time	t_{DIRS}	12*			μs	
DIRC Hold Time	t_{DIRH}	6*			μs	
$\overline{MR}$ Pulse Width	t_{MR}	50*			μs	
$\overline{IP}$ Pulse Width	t_{IP}	10*			μs	

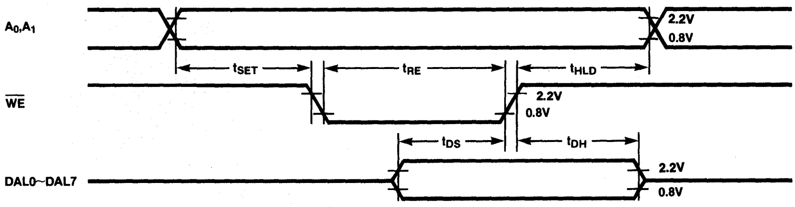
* These values are doubled when CLK = 4MHz.

Timing Diagrams

CPU Read Timing Diagram

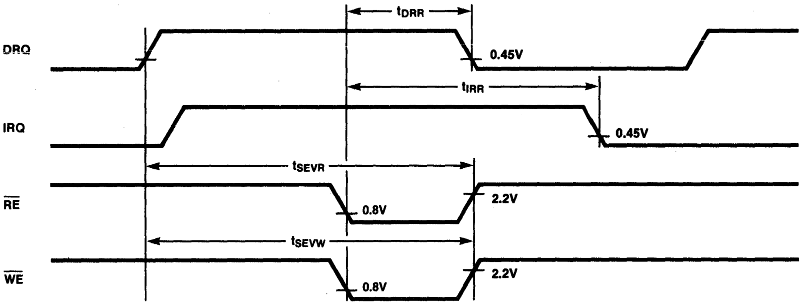


CPU Write Timing Diagram

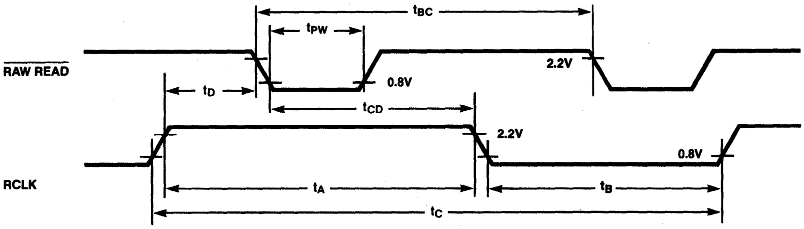


Timing Diagrams
(Continued)

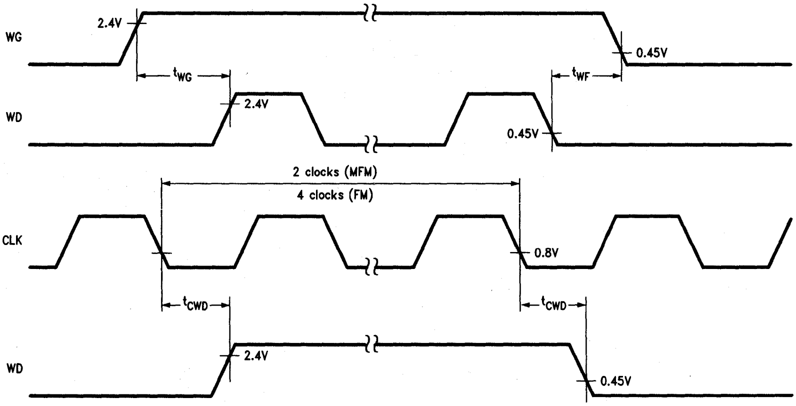
DRQ, IRQ Service and Release Timing Diagram



FDC Read Timing Diagram

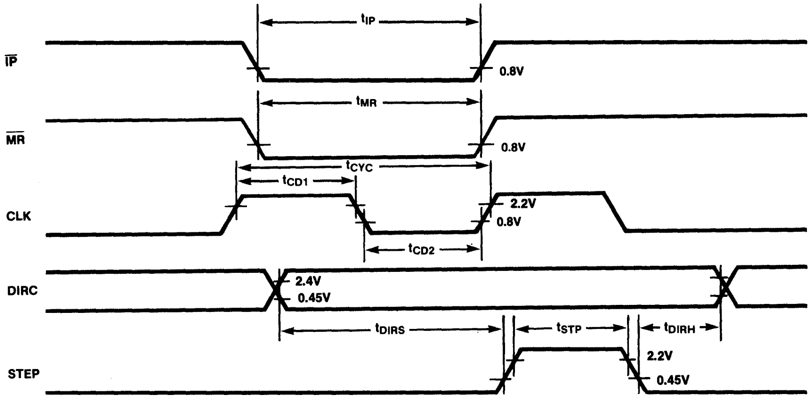


FDC Write Timing Diagram



Timing Diagrams
(Continued)

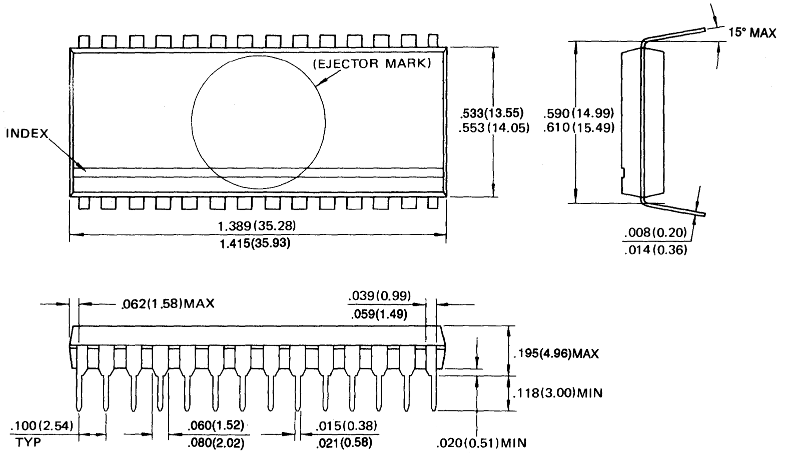
Other Timing Diagram



Package Dimensions

Dimensions in Inches (millimeters)

28-Lead Plastic Dual In-Line Package (Case No.: DIP-28P-M02)



Dimensions in inches (millimeters)

FUJITSU

FLOPPY DISK VFO

MB 4107

October 1984
Edition 1.0

FLOPPY DISK VFO

The Fujitsu MB 4107 is a variable-frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting, and produces a stable read signal for the controller. It also produces a window signal, which can be used to differentiate the clock and data pulses in the read signal.

The MB 4107 includes functions for sync field detection, automatic loop filter gain switching, and address and index mark detection.

- **The analog VFO (PLL) circuitry allows a wide read margin for the data separator.**
- **Can be connected to both 8-inch and 5-inch floppy disk drives using the same external components.**
- **Handless both double-density (MFM) and single-density (FM) disks.**
- **Can be used with various floppy disk controllers such as the MB 8876A, MB 8877A, FD1791, and μPD 765.**
- **The discrimination function for gap and sync fields prevents incorrect locking on the gap field.**
- **The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain).**
- **Because the sync pattern detector (data: 00_H, clock: FF_H) and the IBM format mark detector control PLL gain, the index, ID, and data fields can be locked onto without special control signals.**
- **A master clock is generated for the floppy disk controller, to prevent spikes when switching between 8- and 5-inch floppy disks.**
- **External circuitry requires very few components, and no adjustments.**
  Internal clock: 7 resistors, 5 capacitor, 1 crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitors

Fig. 1 — BLOCK DIAGRAM

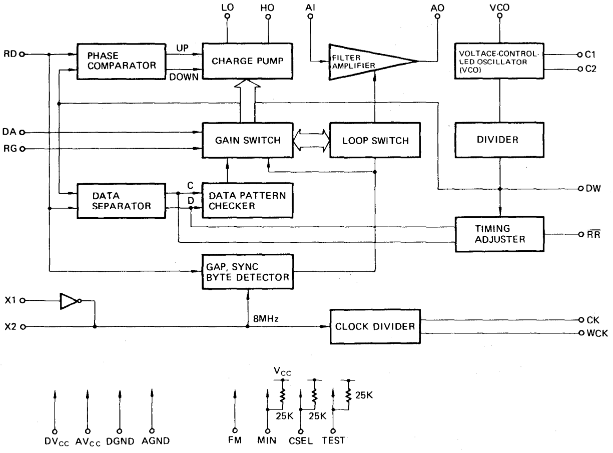


Fig. 2 — PIN ASSIGNMENT

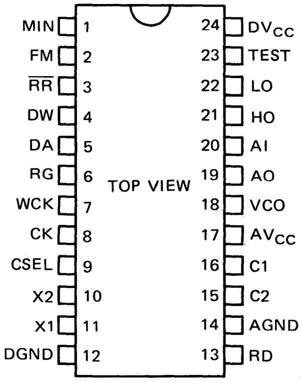


TABLE 1 – PIN FUNCTION

Pin No.	Symbol	Function
1	MIN	Selects type of floppy disk as follows: – 5-inch floppy disk (MIN) High – 8-inch floppy disk (STD) Low
2	FM	Selects the disk density as follows: – Single density (FM system) High – Double density (MFM system) Low
3	$\overline{RR}$	Read data signal for the FDC, including both clock and data pulses.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field. When DA goes high, the PLL is kept as a low gain. Either RG or DA is used, but not both, and the unused pin is kept low.
6	RG	Read Gate (MB 8877A system) or VCO Sync (μPD765 system) input. When a high signal is applied to this pin, PLL is kept at a low gain.
7	WCK	The μPD 765 system FDC write clock pulse is output from this pin as follow: – 8-inch/MFM T = 1 μs – 8-inch/FM T = 2 μs – 5-inch/MFM T = 2 μs – 5-inch/FM T = 4 μs
8	CK	The FDC clock pulse is output from this pin as follows: – MB 8877A system/8-inch 2 MHz – MB 8877A system/5-inch 1 MHz – μPD 765 system/8-inch 8 MHz – μPD 765 system/5-inch 4 MHz
9	CSEL	Selects the FDC type shown below (an internal pull-up resistor is provided): – MB 8877A, FD 1791 system High – μPD 765 system Low
10	X2	(1) Inverter output for the quartz oscillator (2) This pin is open when a 8-MHz external clock is used.
11	X1	(1) Inverter input for the quartz oscillator (2) Input pin when an 8-MHz external clock is used.
12	DGND	Ground for digital circuits
13	RD	Input for the source read data from the FDD
14	AGND	Ground for analog circuits such as VCO and filter amplifier
15 16	C1 C2	An external capacitor for setting VCO oscillating frequency is connected to these pins.

TABLE 1 – PIN FUNCTION (cont'd)

Pin No.	Symbol	Function
17	AV_{CC}	Power supply for analog circuits such as the VCO and filter amplifier.
18	VCO	VCO control current input.
19	AO	Output pin for the low pass filter (LPF) amplifier in the VFO (PLL) circuit.
20	AI	Input pin for the LPF amplifier in the VFO (PLL) circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. A high signal decreases the VCO frequency and a low signal increases it. (High gain)
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock, for phase synchronization. A high signal delays the VCO phase, and a low signal advances it. (Low gain)
23	TEST	Used for the LSI function test. It is normally open or pulled up.
24	DV_{CC}	Power supply pin for digital circuits.

TABLE 2 – MAXIMUM RATINGS (T_A = 25°C)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{CC}		7	V
Logic input voltage	V_{IN}		7	V
Power dissipation	P_D	$T \leqq 75°C$	550	mW
Storage temperature	T_{STG}		–55 ~ +125	°C

TABLE 3 – RECOMMENDED OPERATING CONDITIONS

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature range	T_{OP}	-20	25	75	°C

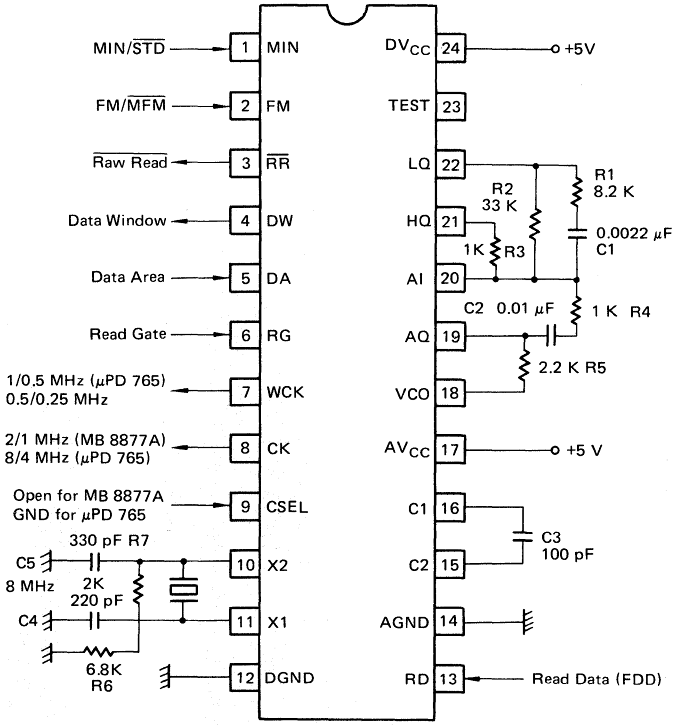
TABLE 4 – ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

(Recommended operating conditions unless otherwise noted)

Item	Symbol	Condition		Value			Unit	Applicable pin	Note
				Min	Typ	Max			
Supply current	I_{CC}	V_{CC} = 5.25 V		–	70	100	mA	V_{CC}	–
High level input voltage	V_{IH}	V_{CC} = 4.75 – 5.25 V		2.0	–	–	V	MIN, FM DA, RG CS, X1 RD	*3
Low level input voltage	V_{IL}			–	–	0.8	V		*3
High level input current	I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V		–	–	20	μA	FM, DA RG, X1 RD	–
Current at maximum input voltage	I_I	V_{CC} = 5.25 V, V_I = 7.0 V		–	–	0.1	mA		–
Low level input current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V		–400	-20	–	μA		–
Open-circuit input voltage	V_{IP}			4.85	5.0	–	V	MIN, CS	–
Low level input current	I_{ILP}	V_I = 0 V		-1.1	-0.6	–	mA		–
High level output voltage 1	V_{OH1}	V_{CC} = 4.75 V, I_{OH} = –1.2 mA		2.7	3.3	–	V	$\overline{RR}$, DW	*1 *3
Low level output voltage 1	V_{OL1}	V_{CC} = 4.75 V	I_{OL} = 12 mA	–	0.28	0.4	V		*2 *3
			I_{OL} = 24 mA	–	0.35	0.5	V		
Short-circuit output current 1	I_{OS1}	V_{CC} = 5.25 V		-30	–	-160	mA		*1 *3
High level output voltage 2	V_{OH2}	V_{CC} = 4.75 V, I_{OH} = –0.4 mA		2.7	3.3	–	V	WCK, CK	*1 *3
Low level output voltage 2	V_{OL2}	V_{CC} = 4.75 V	I_{OL} = 4 mA	–	0.28	0.4	V		*2 *3
			I_{OL} = 8 mA	–	0.35	0.5	V		
Short-circuit output current 2	I_{OS2}	V_{CC} = 5.25 V		-20	–	-110	mA		*1 *3
High level output voltage 3	V_{OH3}	V_{CC} = 4.75 V, I_{OH} = –0.4 mA		2.7	3.3	–	V	X2	*1 *3
Low level output voltage 3	V_{OL3}	V_{CC} = 4.75 V, I_{OL} = 1 mA		–	0.28	0.4	V		*2 *3
High output voltage	V_{HH}	I_{OH} = –1 mA		3.3	3.7	–	V	HO	*1
Low output voltage	V_{LH}	I_{OL} = 1 mA		–	2.0	2.4	V		*2
High output voltage	V_{HL}	I_{OH} = –0.2 mA		3.8	4.2	–	V	LO	*1
Low output voltage	V_{LL}	I_{OL} = 0.2 mA		–	1.5	1.9	V		*2
VCO free run frequency	f_{FR}			1.6	2.0	2.4	MHz		–

NOTE: *1 The output stage is set high. *2 The output stage is set low. *3 T_A = –20°C to 75°C

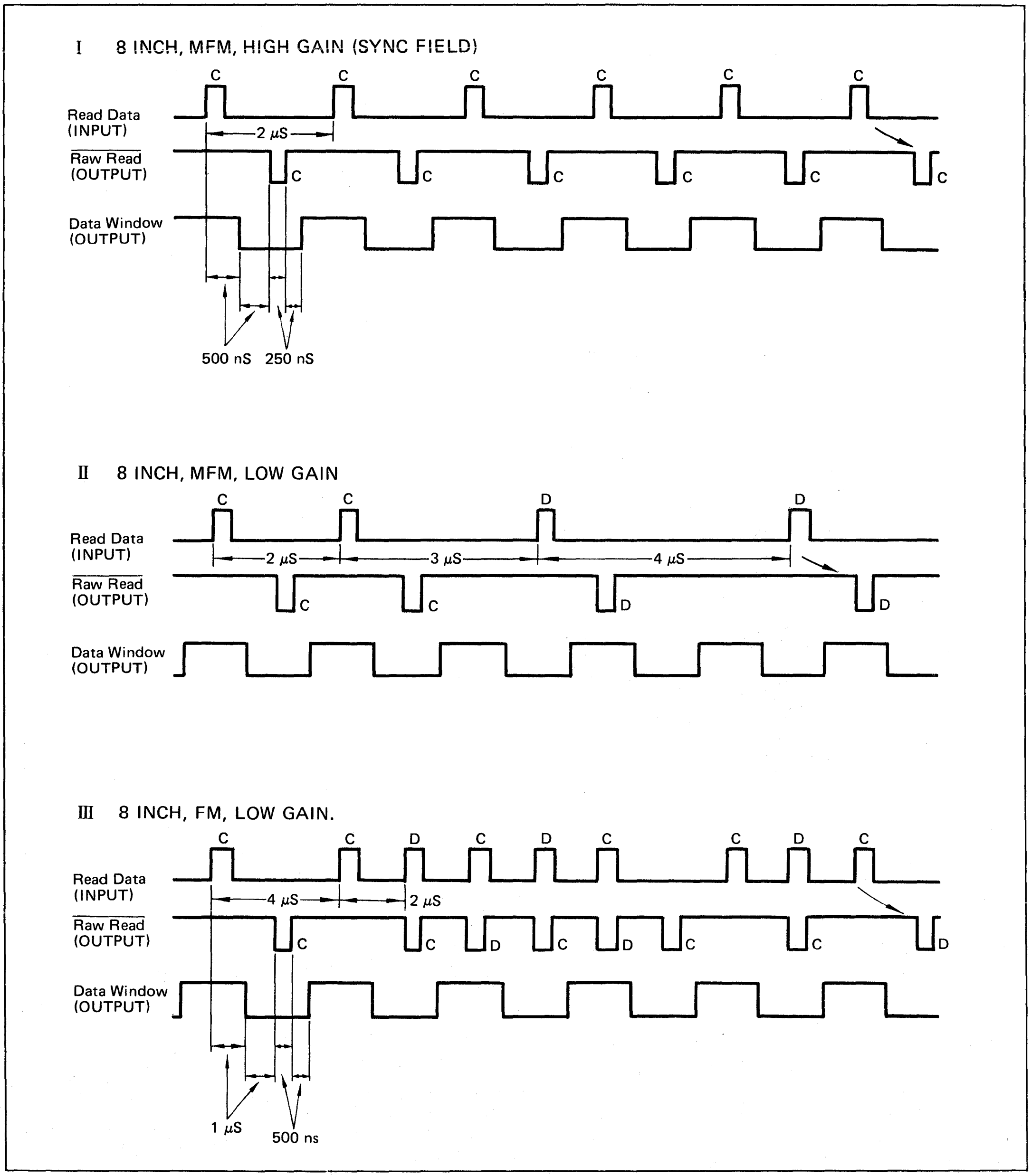
Fig. 3 – STANDARD EXTERNAL CIRCUITS (MB 4107)



NOTE: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)

2. Since the 8-MHz internal and 8-MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not require a high precision.

TIMING CHARTS



I 8 INCH, MFM, HIGH GAIN (SYNC FIELD)

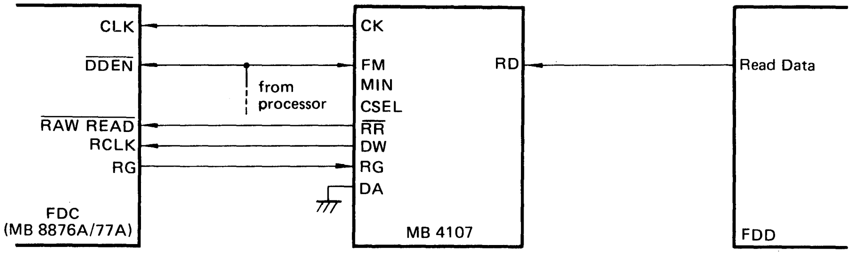
II 8 INCH, MFM, LOW GAIN

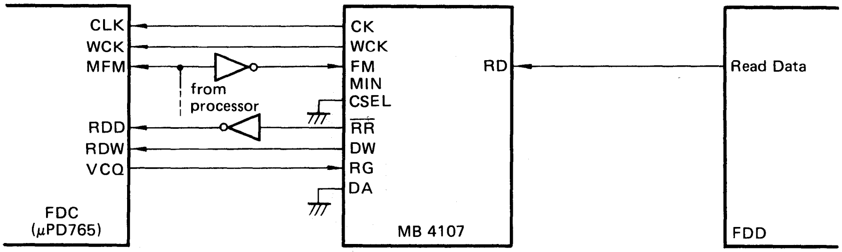
III 8 INCH, FM, LOW GAIN.

NOTES: 1. The above times are doubled for 5-inch floppy disks.
2. C = clock pulse, D = data pulse

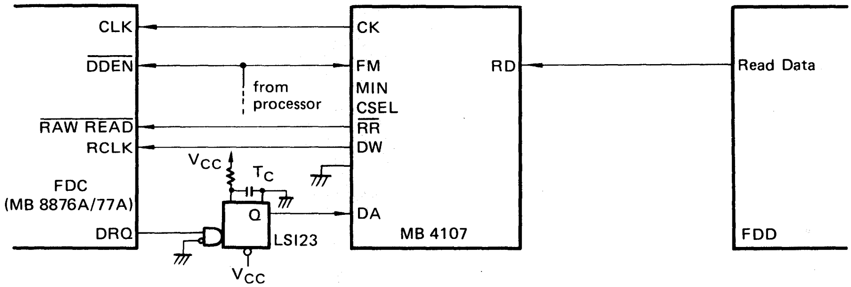
STANDARD CONNECTIONS FDD AND FDC

I READ GATE, VCO SYNC USED

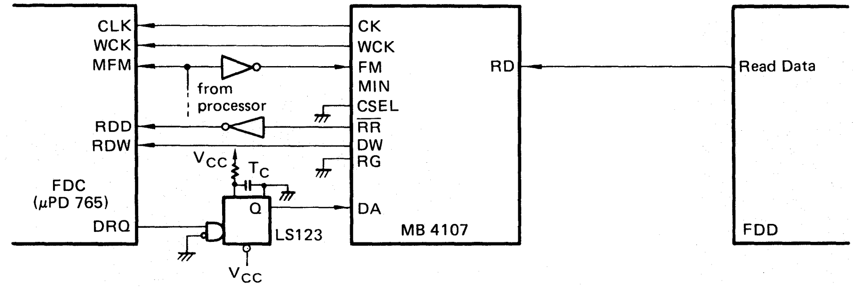




II DATA REQUEST USED



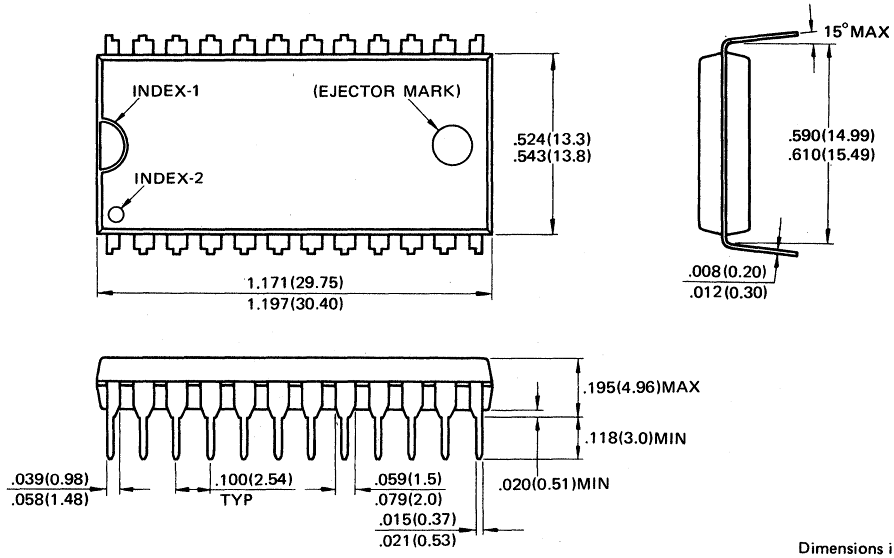
8 inch: T_C = 100 μs ±20% 5 inch: T_C = 200 μs ±20%



8 inch: T_C = 100 μs ±20% 5 inch: T_C = 200 μs ±20%

PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



Dimensions in
inches (millimeters)

FUJITSU

MAGNETIC DISK HEAD AMPLIFIER

MB 4111
MB 4112
MB 4113

March 1984
Edition 2.0

MAGNETIC DISK HEAD AMPLIFIER

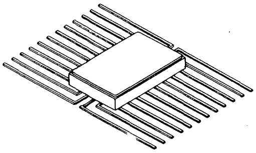
The Fujitsu MB 4111/MB 4112/MB 4113 is a monolithic bipolar integrated circuit optimized for high performance application to disk head systems.

The MB 4111/MB 4112/MB 4113 is featured with the following four major functions to interface with four magnetic heads.

- * Write Amplifier Circuit
- * Read Amplifier Circuit
- * $\overline{\text{RAS}}$ (safety) Circuit
- * Selection Decode Circuit

Also, the MB 4111/MB 4112/MB 4113 has three modes, Read, Write and Idle.

The MB 4111/MB 4113 is suitable for mounting directly on the arm of movable disk head.
The MB 4112 is suitable for mounting on the PC board interfacing the fixed disk head.



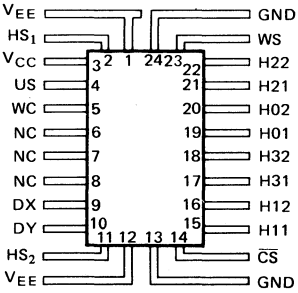
CERAMIC PACKAGE
FPT-24C-F01

ABSOLUTE MAXIMUM RATINGS (*: Referenced to ground)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	7.0	V
Supply Voltage	V_{EE}*	-5.5	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage (Read/Write/Idle)	V_{CC}	5.7	6.0	6.3	V
Supply Voltage (Read/Write/Idle)	V_{EE}	-4.2	-4.0	-3.8	V

Ambient temperature: 0°C to +70°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN NAMES

No.	Symbol	Name
1	V_{EE}	Supply Voltage
2	HS_1	Head Select 1
3	V_{CC}	Supply Voltage
4	US	Unsafe
5	WC	Write Current
6	NC	Non-connection*
7	NC	Non-connection*
8	NC	Non-connection*

No.	Symbol	Name
9	DX	Data X
10	DY	Data Y
11	HS_2	Head Select 2
12	V_{EE}	Supply Voltage
13	GND	Ground
14	WS	Write Select
15	H11	Head 1
16	H12	

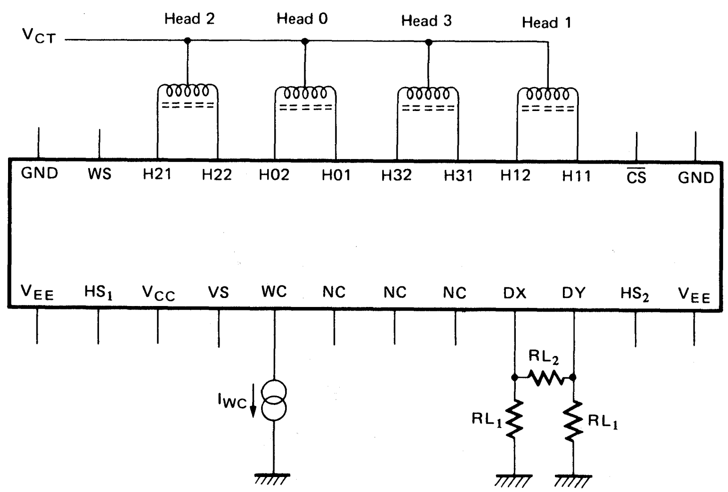
No.	Symbol	Name
17	H31	Head 3
18	H32	
19	H01	Head 0
20	H02	
21	H21	Head 2
22	H22	
23	$\overline{CS}$	Chip Select
24	GND	Ground

Note: NCs should be left open any time.

TEST CONDITIONS

Parameter	Symbol	Mode		Value	Unit
Supply Voltage	V_{CC}	Read/Write/Idle		6.0 ± 1.0%	V
	V_{EE}			-4.0 ± 1.0%	
Head Inductance	L_h	Read/Write	DC	0 (short)	μH
			AC	9.0	
Write Select Voltage	V_{WS}	Write		3.5 ± 1.0%	V
		Read		0.0 ± 0.01	
Chip Select Voltage	V_{CS}	Read/Write		0.0 ± 0.01	V
		Idle		6.0 ± 1.0%	
Unsafe Voltage	V_{US}	Read/Write/Idle		6.0 ± 1.0%	V
Termination Resistor	R_{L1}	Read/Write/Idle		200 ± 1.0%	Ω
	R_{L2}			100 ± 1.0%	
Write Current	I_{WC}	Write		40.0 ± 1.0%	mA
		Read		0.0 ± 0.2	
Ambient Temperature	T_A	Read/Write/Idle		25.0 ± 2.0	°C

Fig. 1 — TEST CIRCUIT



Note: NCs should be left open.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Supply Current	I_{CC}	12	16	20	mA	Selected
				100	µA	Non Selected
Supply Current	I_{EE}	-70			mA	Selected
		-45				Non Selected

MODE SELECT

Parameter	Sybmol	Mode	Value			Unit	Note
			Min	Typ	Max		
$\overline{CS}$ Input High Voltage	V_{IHC}	Idle	5.7	6.0	6.3	V	$-50\mu A < I_{CS} < 0\mu A$
$\overline{CS}$ Input Low Voltage	V_{ILC}	Read/Write	0.0	0.35	0.7	V	
$\overline{CS}$ Input High Current	I_{IHC}	Idle	-70			μA	
$\overline{CS}$ Input Low Current	I_{ILC}	Read/Write	-1.3	-1.0	-0.6	mA	V_{CS} = 0V
WS Input High Voltage	V_{IHW}	Write/Idle	3.2	3.5	3.8	V	
WS Input Low Voltage	V_{ILW}	Read/Idle	0	0.1	0.2	V	
WS Input High Current	I_{IHW1}	Write/Idle	0.7		2.8	mA	Transition Unsafe OFF
	I_{IHW2}	Write/Idle	0.7		3.5	mA	Transition Unsafe ON
WS Input Low Current	I_{ILW}	Read/Idle			0.1	mA	
Switching Delay	t_{SD}	All Modes			500	ns	

TOTAL HEAD INPUT CURRENT

Parameter	Symbol	Mode	Value			Unit	Note
			Min	Typ	Max		
Input Current	I_{I1}	Write			3.0	mA	V_{CT} = 3.5V
Input Current	I_{I2}	Read			0.16	mA	V_{CT} = 0V
Input Current	I_{I3}	Idle			0.5	mA	V_{CT} High or Low

HEAD SELECT

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HS Input High Voltage	V_{IHH}	T_A = 0°C to +70°C	-0.96		-0.81	V
HS Input Low Voltage	V_{ILH}	T_A = 0°C to +70°C	-1.85		-1.65	V
HS Input High Current	I_{IHH}				240	μA
HS Input Low Current	I_{ILH}				30	μA
Switching Delay	t_{SDH}				100	ns

HEAD SELECTION TABLE

Head No.	$\overline{CS}$	HS1	HS2
–	High	–	–
0	Low	High	High
1	Low	Low	High
2	Low	High	Low
3	Low	Low	Low

READ MODE

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Differential Gain	MB 4111 MB 4113	A_V	V_{IN} = 1mVp-p, 0V DC, f = 300KHz	22.0	35.0	46.0	V/V
	MB 4112			5.0	9.0	12.5	
Common Mode Rejection Ratio		CMRR	V_{IN} = 5mVp-p, 0V DC, f ≦ 5MHz	45			dB
Power Supply Rejection Ratio		SV_{RR}	V_{IN} = 0V, f ≦ 5MHz	45			dB
Band Width		BW	Z_{IN} = 0Ω (-3dB)	35			MHz
Channel Noise	MB 4111 MB 4113	V_n	V_{IN} = 0V, Z_{IN} = 0Ω, 10MHz Power Band Width			5.4	µV RMS
	MB 4112					20	
Input Current		I_{IN}	V_{IN} = 0V			40	µA
Input Capacitance	MB 4111 MB 4113	C_I				18.8	pF
	MB 4112					16.0	
Differential Input Resistance	MB 4111 MB 4112	R_D		585	750	915	Ω
	MB 4113			380	480	580	
Output Offset Voltage	MB 4111 MB 4113	V_{OFF}		-100		100	mV
	MB 4112			-50		50	
Unsafe Current		I_U	V_{US} = 6.0V, I_{WC} = 45mA	40		45	mA
Dynamic Range	MB 4111 MB 4113	D	DC input voltage where gain is 90% of gain with 0.5 mVp-p input signal	6			mVp-p
	MB 4112			30			
Channel Separation		S_I	See Note	40			dB
Common Mode Output Voltage		V_O		-0.75	-0.60	-0.45	V

Note: V_{IN} = 1mVp-p, f = 300KHz, 3 Channel driven.

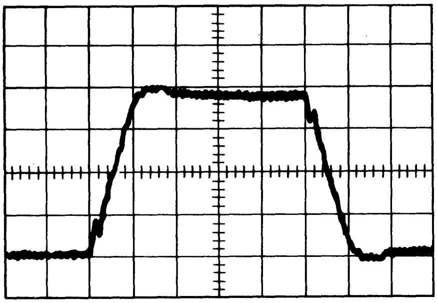
WRITE MODE

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Write Current		I_{WC}				50	mA
Current Gain		A_I	I_{WC} = 50mA	0.95			
Write Current Voltage		V_{WC}	I_{WC} = 45mA	V_{EE}+0.3		V_{EE}+1	V
Differential Input Voltage		V_{IN}		0.225			V
DX DY Input Current		I_{IN}	-0.75V ≦ V_{DX} ≦ -0.45V -0.75V ≦ V_{DY} ≦ -0.45V	-2.0		2.0	mA
Unsafe Current		I_{US}	L = 7μH, f = 1.2MHz, I_{WC} = 20mA			0.1	mA
			L = 9μH, f = 0MHz, I_{WC} = 30mA	20			
Head Current Transition Time		t_T	L = 0μH, f = 5MHz I_{WC} = 50mA		5	10	ns
Head Current Hysterisis		t_{HY}	L = 0μH, f = 5MHz I_{WC} = 50mA			2.0	ns
Unselected Head Current		I_{OP}	L = 9μH, f = 2MHz, I_{WC} = 50mA			1.5	mA
Unsafe Switching Delay Time	MB 4111 MB 4112	t_{USD}	L = 9μH, f = 6.0MHz to 0MHz	0.5		4.0	μs
			L = 7μH, f = 0MHz to 1.2MHz			1.0	
	MB 4113		L = 5μH, I_{WC} = 30mA f = 7.5MHz to 0MHz	0.3		4.0	
			L = 3.5μH, I_{WC} = 15mA f = 0MHz to 3.0MHz			1.0	
Differential Head Voltage	MB 4111 MB 4113	V_{DIF}	I_{WC} = 45mA L = 9μH	6.2		7.2	V
	MB 4112		I_{WC} = 45mA L = 9μH	8.0		9.0	

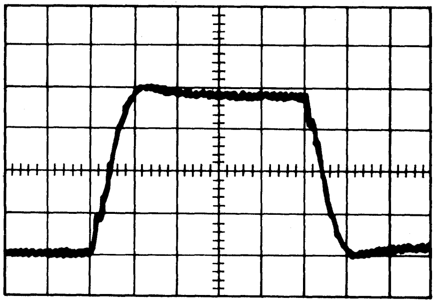
WRITE CURRENT WAVEFORMS

Conditions: L = 9μH, I_{WC} = 40mA

MB 4111

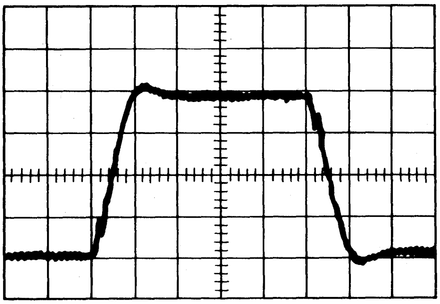


MB 4112

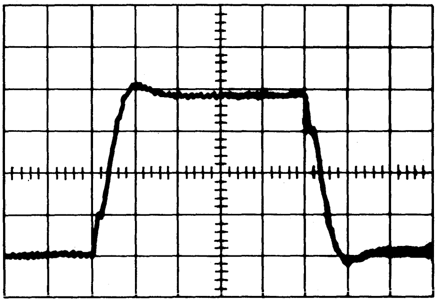


Conditions: L = 7μH, I_{WC} = 40mA

MB 4111

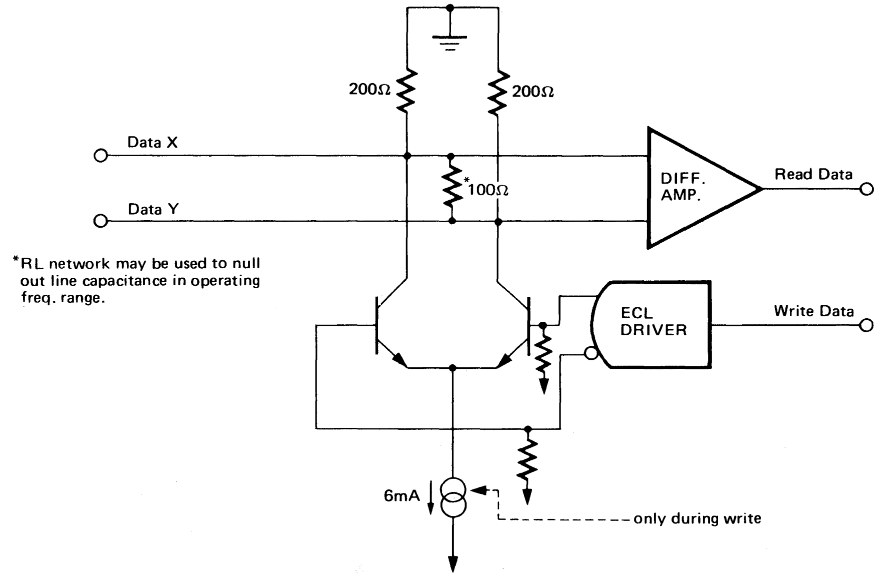


MB 4112



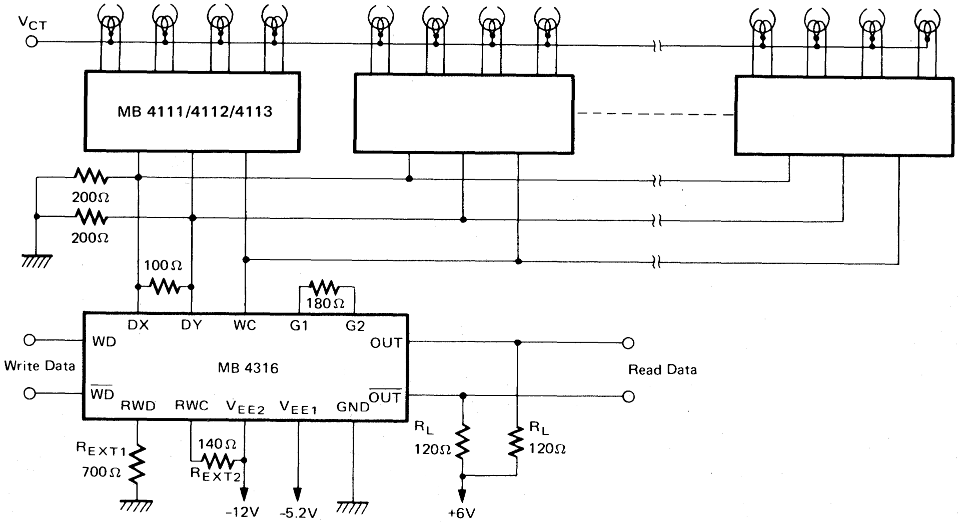
DISK HEAD APPLICATION NOTES

*BIDIRECTIONAL DATA BUS DRIVER



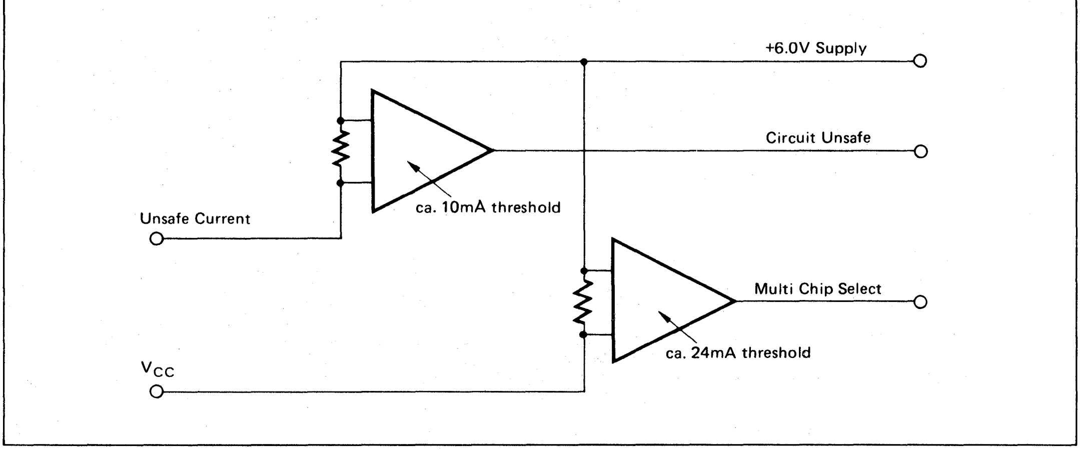
*RL network may be used to null out line capacitance in operating freq. range.

*USAGE IN COMBINATION WITH MB 4316 (BUS SWITCHING CIRCUIT)

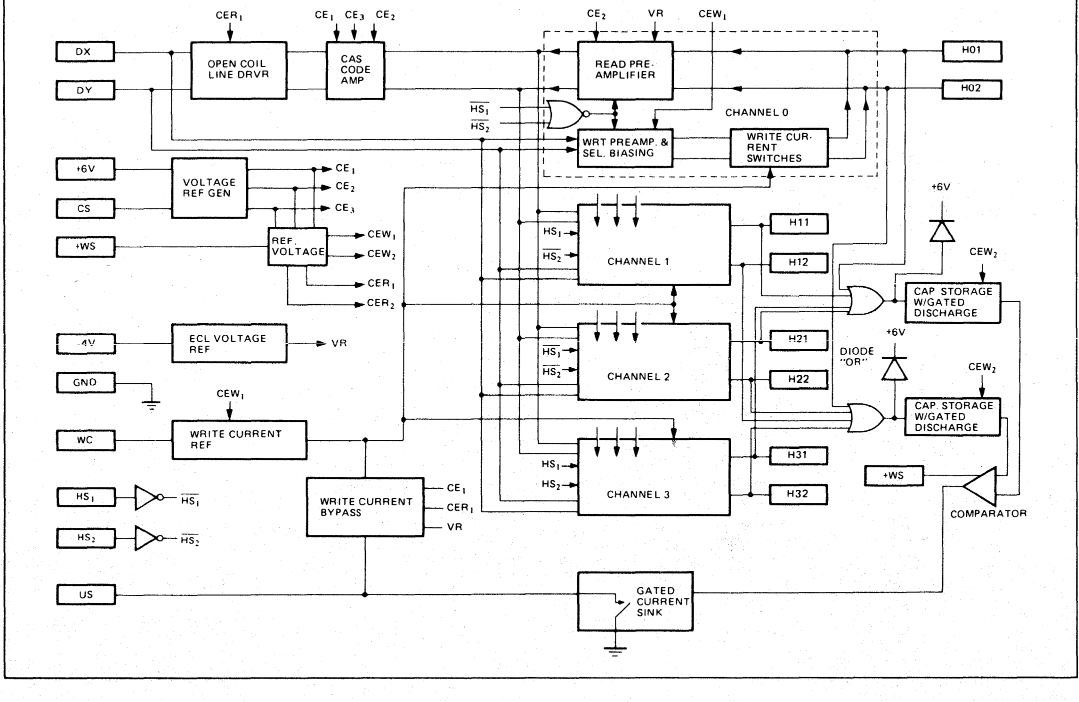


Note: NCs should be left open.

*FAULT DETECTION CIRCUITRY

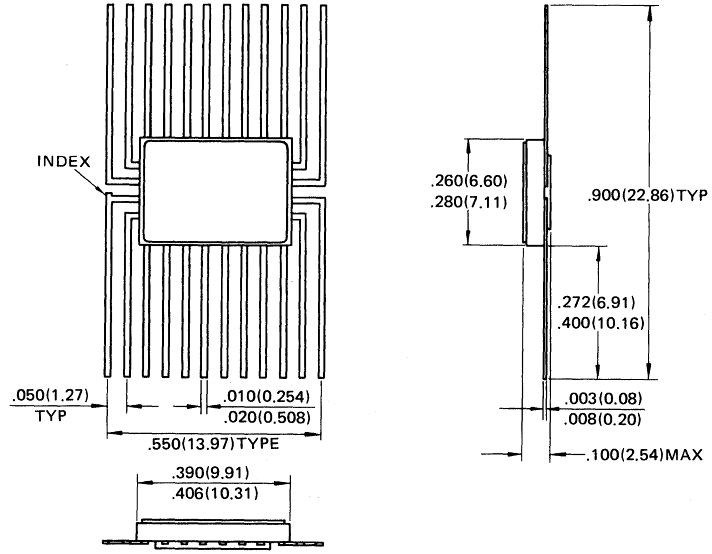


MB 4111/4112/4113 BLOCK DIAGRAM



PACKAGE DIMENSIONS

24-PAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No. : FPT-24C-F01)



Dimensions in
inches (millimeters)

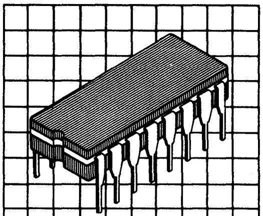
MB4316
Driver/Receiver
for Disk Head Amp.

Description

The Fujitsu MB4316 is designed for the MB4111/MB4112 Disk Head Amplifier's Driver/Receiver.

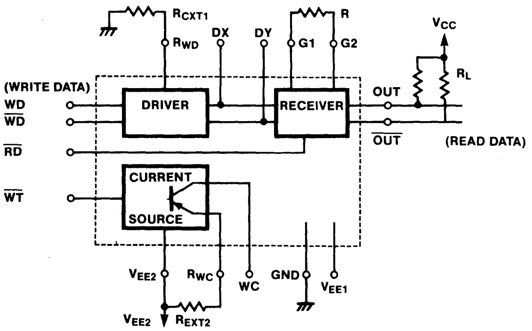
Features

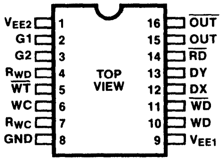
- **Data inputs and Control inputs are CML level inputs.**
- **On-chip Write Current Source which is adjustable by changing an external resister.**



Ceramic Package
DIP-16C-C02

Block Diagram and Pin Assignment





Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{EE1}	−7.0 - 0	V
	V_{EE2}	−15.0 - 0	V
Output Terminal Voltage	V_{CC}	0 - 9.0	V
Input Voltage	V_{IN}	−5.0 - 0	V
Write Current	I_{WG}	0 - 60	mA
Power Dissipation	P_D	580	mW
Operating Temperature	Ta	0 - 70	°C
Storage Temperature	Tstg	−55 - 150	°C

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply voltage	V_{EE1}	−5.2±5%	V
	V_{EE2}	−12.0±5%	V
Output Terminal Voltage	V_{CC}	−6.0±5%	V
External Resistance	R_{EXT1}	700±2%	Ω

Pin Function Table

Pin No.	Symbol	Functions
1	V_{EE2}	Power Supply (−12 V)
2	G1	Gain of output Amplifier (Receiver) is specified with an External resister between G1 and G2.
3	G2	
4	R_{WD}	This input specifies Data level in write mode.
5	$\overline{WT}$	WC switch. When it is at CML low level, WC is active.
6	WC	Write Current Source Output
7	R_{WC}	Write Current is specified with resister between R_{WC} and V_{EE2} (See Block Diagram). (I_{WC}=5.4V/R_{EXT2})
8	GND	Ground
9	V_{EE1}	Power Supply (−5.2V)
10	WD	Write Data, driven by complementary signal of CML level.
11	$\overline{WD}$	
12	DX	Data Bus
13	DY	
14	$\overline{RD}$	Read/Write mode Switch. When it is at CML low level, read mode is selected, and at high level, write mode is selected.
15	OUT	Output for read data
16	$\overline{OUT}$	

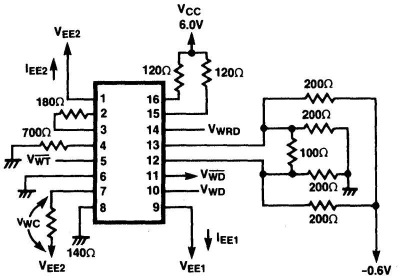
Electrical Characteristics

(V_{EE1} = -5.2V, V_{EE2} = -12.0V, T_A = 25° C)

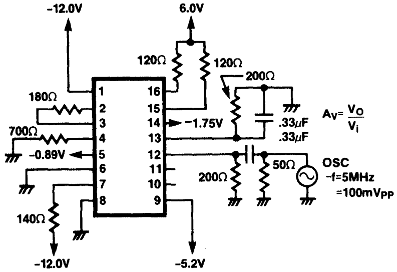
Parameters	Symbol	Conditions	Measurement Diagram	Min.	Typ.	Max.	Unit
Power Supply Current	I_{EE1}	V_{EE1} = -5.46V, V_{EE2} = -12.6V	1	—	—	65	mA
	I_{EE2R}		1	—	—	15	mA
	I_{EE2W}		1	—	—	10	mA
Input Current	$I_{I\overline{RD}}$	V_{EE1} = -5.46V, $V_{\overline{RD}}$ = -0.81V, $V_{\overline{WT}}$ = -1.71V	1	—	—	0.2	mA
	I_{IWD}	V_{WD} = -0.81V	1	—	—	0.9	mA
	$I_{I\overline{WD}}$	V_{EE2} = -12.6V, $V_{\overline{WD}}$ = -0.81V	1	—	—	0.9	mA
	$I_{I\overline{WT}}$	$V_{\overline{RD}}$ = -1.71V, $V_{\overline{WT}}$ = -0.81V	1	—	—	0.15	mA
Output Voltage	V_{WC}	$V_{\overline{RD}}$ = -0.89V, $V_{\overline{WT}}$ = -1.75V	1	4.9	5.4	5.9	V
	V_{DXH}	$V_{\overline{RD}}$ = 0.96V, $V_{\overline{WT}}$ = 1.65V, $V_{\overline{WD}}$ = -0.96V	1	-0.59	—	-0.45	V
	V_{DXL}	V_{WD} = -0.96V	1	-0.75	—	-0.61	V
	V_{DYH}		1	-0.59	—	-0.45	V
	V_{DYL}	$V_{\overline{WD}}$ = -0.96V	1	-0.75	—	-0.61	V
DxDy Differential Output Voltage	$\vert V_{XY}\vert$	$\vert V_{DX} - V_{DY}\vert$	1	160	—	—	mV
Voltage Gain	A_V	V_1 = 100mV_{PP}, f = 5MHz	2	0.95	1.1	1.25	V/V
Band Width	BW		2	30	—	—	MHz
Delay Time	t_{PLH1}	$\overline{WT}$ → RWC	3	—	—	350	ns
	t_{PLH1}		3	—	—	100	ns
	t_{PLH2}	RD → DX, DY	4	—	—	200	ns
	t_{PLH2}		4	—	—	100	ns

Measurement Diagram

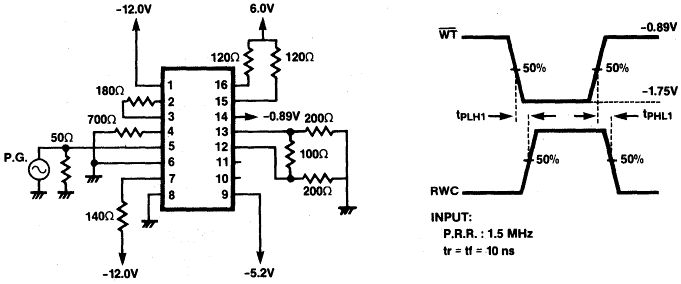
1.



2.

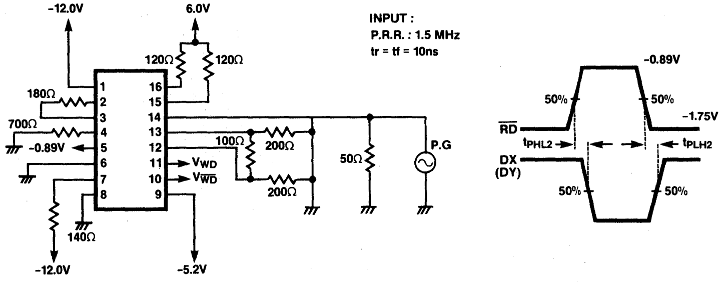


3.



INPUT:
P.R.R. : 1.5 MHz
tr = tf = 10 ns

4.



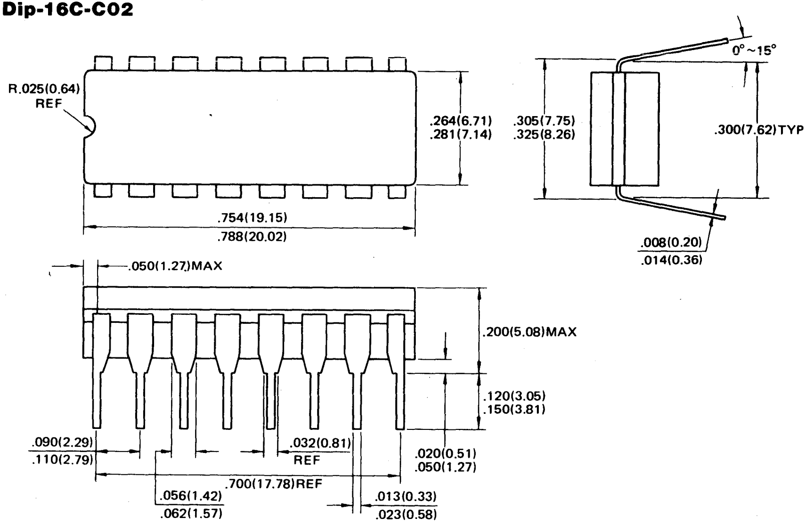
INPUT :
P.R.R. : 1.5 MHz
tr = tf = 10ns

Output	Bias V_{WD}	$V_{\overline{WD}}$
DX	−0.89V	-1.75V
DY	−1.75V	-0.89V

Package Dimensions

Dimensions in inches (millimeters)

16-Lead Ceramic (Cerdip) Dual In-Line Package Dip-16C-C02



FUJITSU

MB88303
NMOS Television Display Controller (TVDC)

October 1986
Edition 2.0

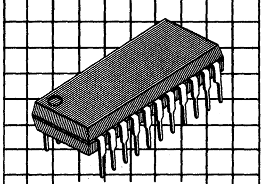
Description

The Fujitsu MB88303 NMOS Television Display Controller (TVDC) is an interface LSI that displays 180 alphanumeric characters (20 characters x 9 lines) in white on a TV screen. The characters overlay the picture on the TV screen.

While designed to operate in conjunction with the Fujitsu MB8840/8850 and MB88400/88500 single-chip 4-bit microcomputers, the MB88303 TVDC can also be interfaced to a wide range of 4- and 8-bit microprocessors.

The MB88303 allows simple interface to almost any TV display (raster scan CRT with horizontal and vertical scanning) regardless of interlace or non-interlace scan.

The MB88303 is fabricated with N-channel silicon-gate E/D MOS process, and packaged in a 22-pin plastic DIP. Also, it is powered by a single +5V power supply, and operates over a temperature range of -30°C to +70°C.

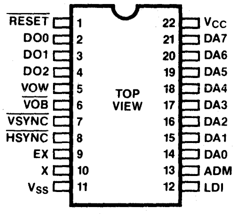


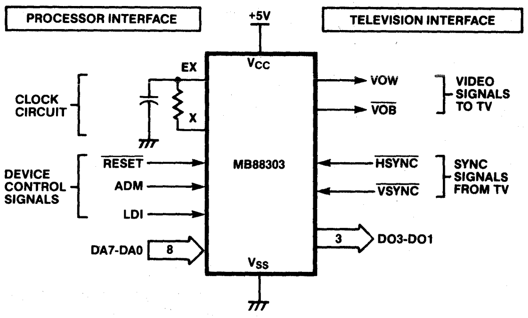
Plastic DIP
DIP-22P-M02

Features

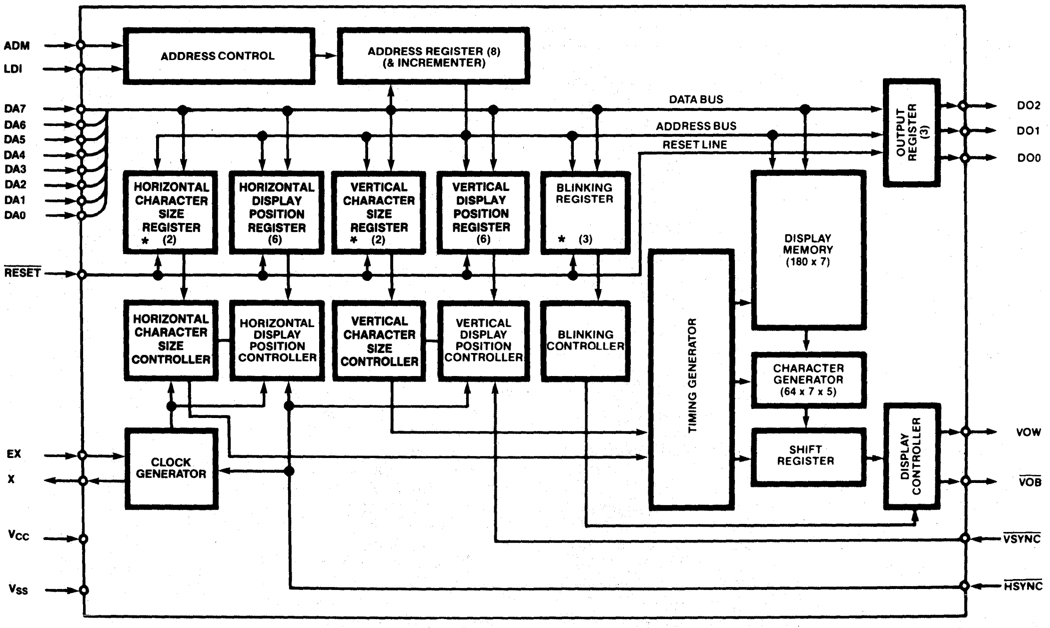
- **Character display controller available for NTSC, PAL and SECAN TV sets**
- **20 character x 9-line screen format (Max. 180 characters/screen)**
- **5x7-dot matrix character format (1-dot horizontal and 2-dot vertical spacings)**
- **64-character set**
- **Programmable character size: 4 widths and 4 heights**
- **Programmable display start position: 57 horizontal and 64 vertical positions**
- **Programmable character blinking control**
- **Automatic inter-dot filling function for improved smoothness**
- **Black-level background output for improved clarity**
- **180 x 7-bit display data RAM**
- **448 x 5-bit character generator ROM**
- **Four control registers**
- **3-bit general-purpose open-drain latched output**
- **On-chip clock generator for external RC-network**
- **Single +5V power supply**
- **Wide operating temperature range: -30° C to +70° C**
- **N-channel silicon-gate E/D MOS process**
- **22-pin plastic DIP (Suffix -P)**

Pin Assignment And Logic Symbol





Block Diagram


ADM
LDI
DA7
DA6
DA5
DA4
DA3
DA2
DA1
DA0
RESET
EX
X
Vcc
Vss
ADDRESS CONTROL
ADDRESS REGISTER (8) (& INCREMENTER)
DATA BUS
ADDRESS BUS
RESET LINE
OUTPUT REGISTER (3)
DO2
DO1
DO0
HORIZONTAL CHARACTER SIZE REGISTER * (2)
HORIZONTAL DISPLAY POSITION REGISTER (6)
VERTICAL CHARACTER SIZE REGISTER * (2)
VERTICAL DISPLAY POSITION REGISTER (6)
BLINKING REGISTER * (3)
DISPLAY MEMORY (180 x 7)
HORIZONTAL CHARACTER SIZE CONTROLLER
HORIZONTAL DISPLAY POSITION CONTROLLER
VERTICAL CHARACTER SIZE CONTROLLER
VERTICAL DISPLAY POSITION CONTROLLER
BLINKING CONTROLLER
TIMING GENERATOR
CHARACTER GENERATOR (64 x 7 x 5)
SHIFT REGISTER
DISPLAY CONTROLLER
CLOCK GENERATOR
VOW
VOB
VSYNC
HSYNC

* THESE REGISTERS ARE DESIGNATED BY ONE ADDRESS AS THE DISPLAY CONTROL REGISTER.

Pin Description

	Symbol	Pin No.	Type	Function
Power Supply	V_{CC}	22	—	+5V power supply pin.
	V_{SS}	11	—	Ground pin.
Clock	EX	9	I	RC-network externally connected to these pins from On-chip oscillator 6MHz clock generator.
	X	10	O	
Processor Interface	$\overline{\text{RESET}}$	1	I	Reset input: A low level on $\overline{\text{RESET}}$ stops the TVDC and initializes its internal control registers to the following states: Horizontal Display Position Register : Cleared. Vertical Display Position Register : Cleared. Display/Character Control Register : Cleared. (consisting of Horizontal Character Size, Vertical Character Size, and Blinking Registers) General-Purpose Output Register : Set. As a result, the output pins are clamped in the following states: VOW = "L", VOB = "H", DO2 = DO1 = DO0 ="H" The address register and display memory are not affected by $\overline{\text{RESET}}$. This pin is a non-TTL compatible hysteresis input with an internal pull up.
	ADM	13	I	Address mode select input for writing data to the internal registers and the display memory: A low level on ADM activates the Direct Address mode. A high level on ADM activates the Address Increment mode. This pin is a TTL compatible input with an internal pull up.
	LDI	12	I	Write strobe input for multiplexed address/data: Direct Address Mode: At the leading edge of LDI, an 8-bit address on DA7-DA0 is automatically latched into the internal address register. At the trailing edge of LDI, a 7-bit data on DA6-DA0 is written into an internal control register or an internal display memory location that is designated by the address latched at the leading edge. Address Increment Mode: At the leading edge of LDI, the address register is automatically incremented. At the trailing edge of LDI, a 7-bit data on DA6-DA0 is written into an internal control register or a display memory location that is indicated by the address register. This is a non-TTL compatible input with an internal pull up.
	DA7-DA0	21-14	I	8-bit parallel multiplexed address/data input: An address/data on DA7-DA0 is written into the internal registers or the display memory at the LDI transition. The address/data input format is DA7: the most significant bit (MSB) DA0: the least significant bit (LSB) These pins are TTL compatible with internal pull up.

Pin Description

(Continued)

Television Interface

Symbol	Pin No.	Type	Function
$\overline{\text{HSYNC}}$	8	I	Horizontal synchronization input: $\overline{\text{HSYNC}}$ pulses are supplied by the TV set connected. This signal is the same as the horizontal sync signal of the TV display, which controls display start position. The MB88303 starts to output character bit patterns on the VOW output, triggered by $\overline{\text{HYSNC}}$ pulse. This pin is a non-TTL compatible hysteresis input with an internal pull up.
$\overline{\text{VSYNC}}$	7	I	Vertical synchronization input: $\overline{\text{VSYNC}}$ pulses are supplied by the TV set connected. This signal is the same as the vertical sync signal of TV display, which controls display starts position. The MB88303 starts to output character bit patterns on the VOW output, triggered by $\overline{\text{VSYNC}}$ pulse. This pin is a non-TTL compatible hysteresis input with an internal pull up.
VOW	5	O	White-level video signal output: The device serially outputs character dot patterns on VOW synchronously with HYSNC pulses. This signal is used for brightness modulation of the TV display. This signal is superimposed on the normal TV video signal. This pin is a TTL compatible output.
$\overline{\text{VOB}}$	6	O	Black-level video signal output: This signal is supplied to the TV to improve clarity of displayed characters when BLK and BLKB bits of the blinking register are set. This pin is a TTL compatible output.
DO2-DO0	4-2	O	3-bit parallel output port: Data written into the general output register appears on pins DO_2-DO_0 These signals are used for other attribute control to TV. These are latched open-drain outputs.

Functional Description

Screen Format and Character Format

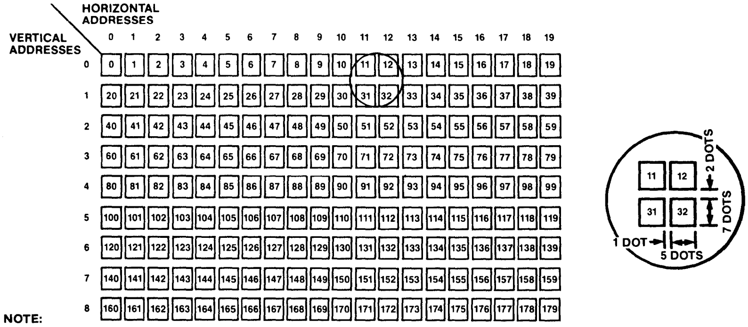
The MB88303 TVDC supports the display of 9 lines of 20 characters per line, or a total of up to 180 alphanumeric characters, as shown in Figure 1.

The characters are formed in a 5 x 7-dot matrix, with a 1-dot space between characters and a 2-dot space between lines. Screen Format also shows the relative on-screen size of the displayed elements. Figure 2 shows the character format.

Character Patterns and Codes

The MB88303 has a built-in 5 x 7-dot matrix character generator ROM. Fig. 6(a) shows internal character patterns in the character generator, which are automatically modifed by "filling" function and displayed on the screen as shown in Figure 3(b). The character patterns are encoded as shown in Table 1.

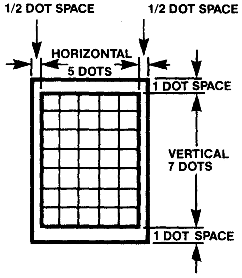
Figure 1. Screen Format



VERTICAL ADDRESSES \ HORIZONTAL ADDRESSES	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
2	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59
3	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
4	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99
5	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
6	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139
7	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
8	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179

NOTE:
NUMBERS 0 to 179 INDICATE DISPLAY MEMORY ADDRESSES.

Figure 2. Character Format



Note:
Refer to Page 10 for an explanation of the difference between blanks and background.

Table 1. Character Codes

CH3-0 \ CH5-4	0	1	2	3
0	A	N	0	↑
1	B	O	1	↓
2	C	P	2	←
3	D	Q	3	→
4	E	R	4	+
5	F	S	5	–
6	G	T	6	*
7	H	U	7	/
8	I	V	8	=
9	J	W	9	&
A	K	X	?	年 (kanji)
B	L	Y	!	月 (kanji)
C	M	Z	' (apostrophe)	日 (kanji)
D	• (raised dot)	:	. (period)	, (comma)
E	⊔	■	□ (background)	~
F	⬚ (blank)	[	]	☎ (Telephone)

Functional Description
(Continued)

Figure 3(a). Internal Character Dot Patterns
(Character Generator ROM Patterns)

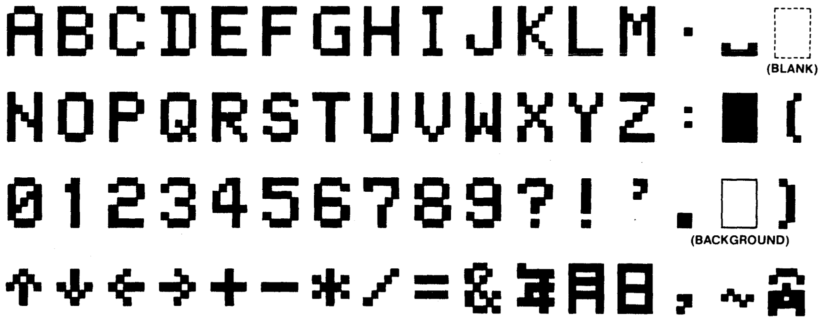
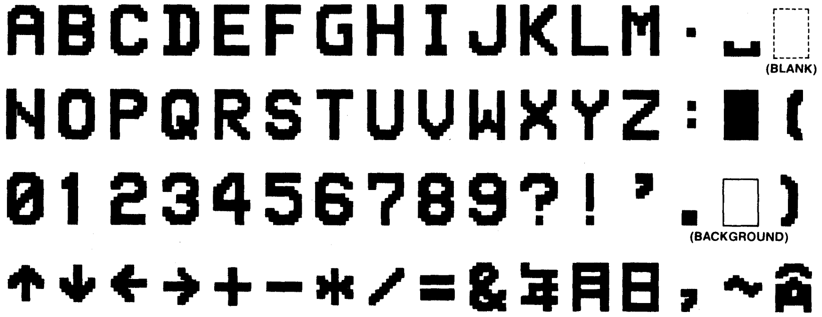


Figure 3(b). Displayed Character Dot Patterns
(Format with "Filling" Function)

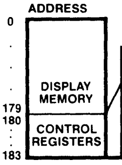


Functional Description
(Continued)

Address Structure

All addresses are 8-bit words. Addresses from 0 [00000000] to 179 [10110011] indicate the display memory locations. Addresses from 180 [10110100] to 183 [10110111] are used for the control registers. Figure 4 shows the memory map. Selected addresses are input through pins DA7 to DA0. Addresses 184 above cannot be used.

Figure 4. Display Memory & Control Register Map



ADDRESS \ BIT	6	5	4	3	2	1	0
180	—	HP5	HP4	HP3	HP2	HP1	HP0
181	—	VP5	VP4	VP3	VP2	VP1	VP0
182	BLINK	BLKB	BLK	VSZ1	VSZ0	HSZ1	HSZ0
183	—	—	—	—	DO2	DO1	DO0

- HP5 TO 0 : HORIZONTAL DISPLAY POSITION REGISTER
- VP5 TO 0 : VERTICAL DISPLAY POSITION REGISTER
- HSZ1 TO 0 : HORIZONTAL CHARACTER SIZE REGISTER
- VSZ1 TO 0 : VERTICAL CHARACTER SIZE REGISTER
- BLK : DISPLAY BLANKING BIT
- BLKB : BACKGROUND BLANKING BIT
- BLINK : BLINKING ENABLE BIT
- DO2 TO 0 : GENERAL OUTPUT REGISTER

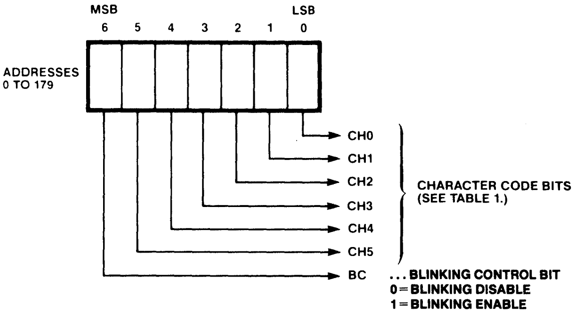
BLK, BLKB, BLINK: BLINKING REGISTER
HSZ1 TO 0 through BLINK: DISPLAY CONTROL REGISTER

Display Memory

The display memory is a 180 x 7-bit RAM. Bits 5 to 0 (CH5-CH0) are character code storage; Bit 6 (BC) can be set to "1" to enable blinking, and reset to zero to disable blinking.

Figure 5 shows the word structure; refer to Character Codes table for character codes (see page 5). Selected character codes and blinking control bit are input through pins DA6 to DA0.

Figure 5. Display Memory Word Format

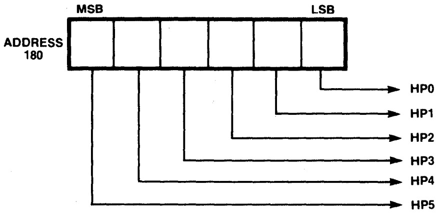


Control Registers

Horizontal Display Position Register [HP5 to HP0]

This register (address 180) stores the horizontal position of the start of the diplay on the TV screen. The values (000000) to (000110) cannot be used for the horizontal display position register. Since the RESET input clears this register, a value must be set after every RESET input. Figure 6 shows the horizontal display position register. For the display starting position control, see page 9.

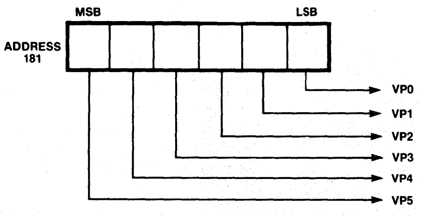
Figure 6. Horizontal Display Position Register Format



Vertical Display Position Register [VP5 to VP0]

This register (address 181) stores vertical position of the start of the display on the TV screen. Since the RESET input clears this register, a value must be set after every RESET input. Figure 7 shows the vertical display position register. For the display starting position control see page 9.

Figure 7. Vertical Display Position Register Format



4

Functional Description
(Continued)

Display Control Register

(1) Horizontal Character Size Register [HSZ1 and HSZ0]

These bits indicate the width of the characters. Character width is selectable from 4 values determined by setting HSZ1 and HSZ0 as shown in Table 2. The reset input rests both bits to zero.

Note: T is the period of oscillation frequency Q. When the oscillation frequency is Q [Hz], the period at that time T[s] is 1/Q.

(2) Vertical Character Size Register [VSZ1 and VSZ0]

These bits indicate the height of the characters. Character height is selectable from 4 values by setting VSZ1 and VSZ0 as shown in Table 3. The reset input rests both bits to zero.

Note: 1H (horizontal line) = 63.5μs. One screen at non-interlace scan is 262.5H.

(3) Blinking Register [BLK, BLKB and BLINK]

— Display Blanking Bit [BLK]

This bit indicates the status of the characters display. When BLK is zero, no data is displayed; to enable display, set BLK to "1". The reset input resets BLK to zero.

— Background Blanking Bit [BLKB]

This bit indicates the status of the background display. When BLKB is zero, background is not displayed regardless of data content; to enable background display, set BLKB to 1. The reset input resets BLKB to zero.

— Blinking Enable Bit [BLINK]

This bit turns blinking on and off. When BLINK is zero, blinking is disabled regardless of blink control bit value of the display memory input; when BLINK is "1", blinking is enabled, provided that the blink control bit of the display memory is set to "1". The reset input resets BLINK to zero.

Figure 8. Display Control Register Format

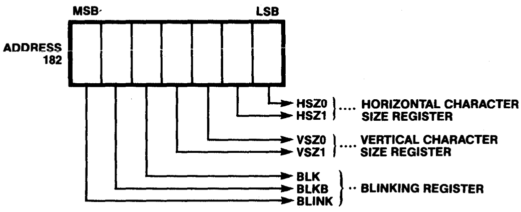

MSB
LSB
ADDRESS 182
HSZ0
HSZ1
.... HORIZONTAL CHARACTER SIZE REGISTER
VSZ0
VSZ1
.... VERTICAL CHARACTER SIZE REGISTER
BLK
BLKB
BLINK
.. BLINKING REGISTER

Table 2. Horizontal Character Size

Code		Size		Size	
HSZ1	HSZ0	Character	Dot	Character (when Q = 6MHz, T = 167ns)	Dot
0	0	10T	2T	1.67μs	0.33μs
0	1	20T	4T	3.34μs	0.67μs
1	0	30T	6T	5.01μs	1.0μs
1	1	40T	8T	6.68μs	1.34μs

Table 3. Vertical Character Size

Code		Size	
VSZ1	VSZ0	Character	Dot
0	0	14H	2H
0	1	28H	4H
1	0	42H	6H
1	1	56H	8H

Figure 9. General Output Register Format

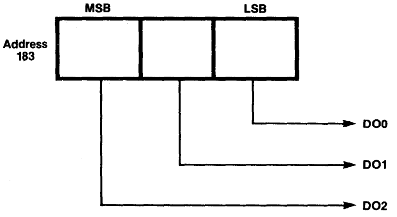
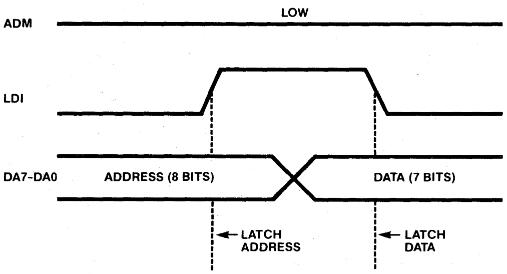


Figure 10(a). Direct Address Mode Timing



Functional Description (Continued)

General Output Register

This is a 3-bit latched output; data written to DO2 to DO0 is output to the open drain terminals DO2 to DO0. The reset input sets DO2 to DO0 lines to "1".

Data Input

MB88303 has two modes for writing data to the control registers and display memory. The modes are switched by the ADM input.

Direct Address Mode

This mode is enabled when input to the ADM terminal is low. When the input signal to the LDI terminal goes high, data on DA7 to DA0 are latched to the address register. When the LDI terminal signal goes low, 7 bits of data, DA6 to DA0, are written to the memory specified by the memory address register. Fig. 10(a) is the timing diagram.

Address Increment Mode

This mode is enabled when input to the ADM terminal is high. When the input signal to the LDI terminal goes high, the data currently latched to the address register are incremented. When the LDI terminal signal goes low, 7 bits of data, DA6 to DA0, are written to the memory specified by the address register after incrementing. Fig. 10(b) is the timing diagram.

Figure 10(b). Address Increment Mode Timing

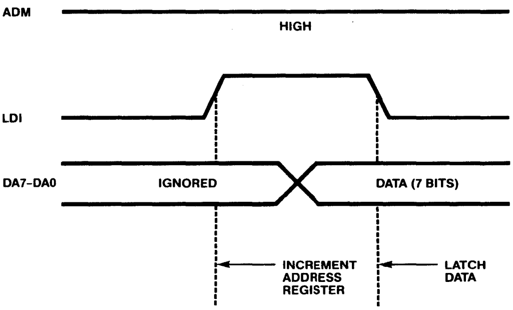
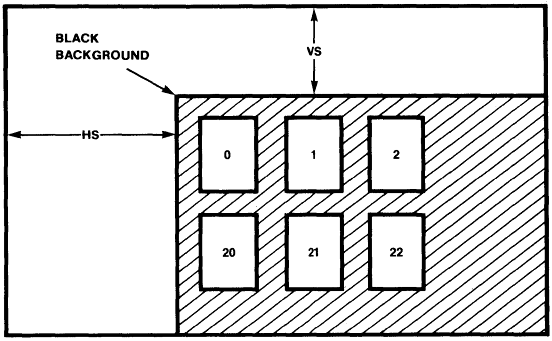


Figure 11. Display Start Position



Note: If T(s) is the period when the oscillating frequency is fc (Hz), H will be equal to one period of the horizontal synchronization signal.

Reset

1. The following internal registers are cleared by $\overline{\text{RESET}}$.

Horizontal character size register: HSZ1 = HSZ0 = "0"

Horizontal display position register: HP5 to HP0 = "0"

Vertical character size register: VSZ1 = VSZ0 = "0"

Vertical display position register: VP5 to VP0 = "0"

Blinking register: BLINK = BLKB = BLK = "0"

2. General output register (DO outputs) is set by $\overline{\text{RESET}}$. DO2 = DO1 = DO0 = "1" ("H")

3. VOW and $\overline{\text{VOB}}$ outputs are initialized by $\overline{\text{RESET}}$ as follows:

VOW = "L", $\overline{\text{VOB}}$ = "H" (Blanks are displayed on the screen.)

No character is displayed on the TV screen until "BLK" bit (Bit 4 of Blinking Register) is set to "1".

4. Address register and Display data memory are not affected by $\overline{\text{RESET}}$.

Functional Description
(Continued)

Display Starting Position Control

The horizontal and vertical display starting points on the TV screen are determined by specifying the position at which the black background display begins. This is done with the values of addresses HP5 to HP0 and VP5 to VP0 as shown in Fig. 6 and Fig. 7.

The horizontal starting position HS and the vertical start position VS may be found using the following equations:

$$HS = T \times 4 [2^5 \times HP5 + 2^4 \times HP4 + 2^3 \times HP3 + 2^2 \times HP2^2 + 2 \times HP1 + HP0) + P]$$

$$VS = H \times 4 (2^5 \times VP5 + 2^4 \times VP4 + 2^3 \times VP3 + 2^2 \times VP2 + 2 \times VP1 + VP0)$$

where: P = width of character, from Table 4;
T = 1/fc [fc = oscillating frequency; 6MHz typ.]
H = period of horizontal synchronization signal [63.5μs typ.]

Blinking Control

The MB88303 supports blinking of any desired character(s) on the screen. Blinking affects only those characters for which the blinking bit is set to 1. Display is on for approximately 0.5s and off for the same period (vertical synchronization pulse x 64).

Table 4. P Values

HSZ1	HSZ0	P
0	0	9
0	1	10
1	0	11
1	1	12

Figure 12(a). Dot Filling Examples

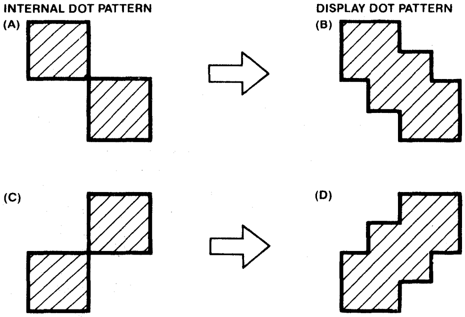
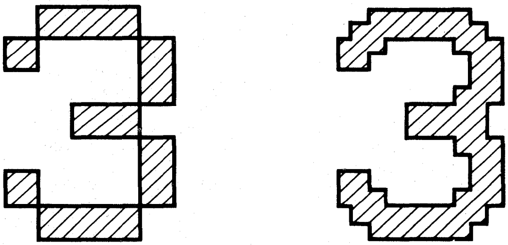


Figure 12(b). Simple 5×7 Matrix [Left] & with "Filling" Function [Right]



Blinking can be set as follows:

1. Set the blinking enable bit of the display control register to 1.

2. Set the blink control bit to 1 for the position of the display memory corresponding to the character for which blinking is desired.

"Filling" Function

"Filling" is the process whereby dot matrix displays like those in (A) of Fig. 12(a) 'a, are filled out to the form shown in (B) by the display of an intermediate dot. As can be seen from Fig. 12(b) "filling" results in a smoother and more pleasing shape than can be attained with an ordinary 5 x 7-dot matrix.

Functional Description (Continued)

Display Output Timing

Fig 13. shows the timing for VOW and $\overline{\text{VOB}}$ for the overlayed portion of a display consisting of the letter "A", a "blank" (character code 0F), "background" (character code 2E), and the letter "B", with the display blinking and background blanking set to 1.

Note that the display of the background changes during the "BLANK" character when the $\overline{\text{VOB}}$ line goes high.

Difference Between Blanks and Background

Note: In Fig. 14(b) which shows a screen of characters overlaying the picture of a woman, a blank (character code 0F) displays differently from background (character code 2E), depending on whether $\overline{\text{VOB}}$ is used or not.

In Fig. 14(b) both pictures display the letter "A", a "blank", a "background", the letter "B", and a "blank".

In the right picture of Fig. 14(b), where $\overline{\text{VOB}}$ is on, the character displays are bounded by a black frame, so that the spaces between characters display as black. Where a blank is displayed, a 5 x 7-dot portion of the TV picture is visible. The background display is black.

In the left picture of Fig. 14(b), were VOB is off, the TV picture is visible everywhere on the screen except where the characters display in white. Here, blanks and background are displayed identically. Note that the broken lines have been drawn in to indicate where the frames would be displayed if they were displayed on the screen.

Figure 13. Display Output Timing

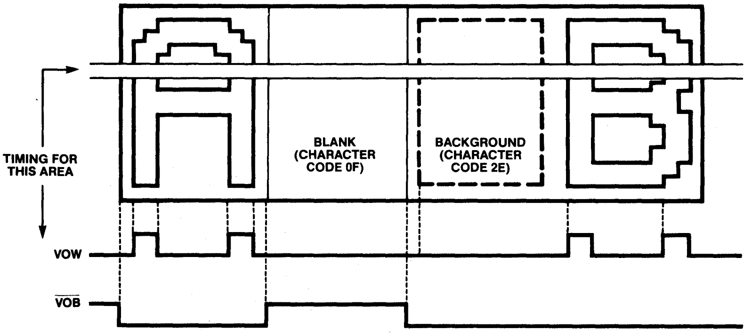
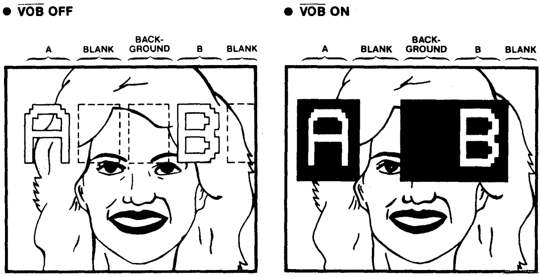


Fig 14(a). Display of TV Picture

Fig 14(b). Display of Character on TV Picture

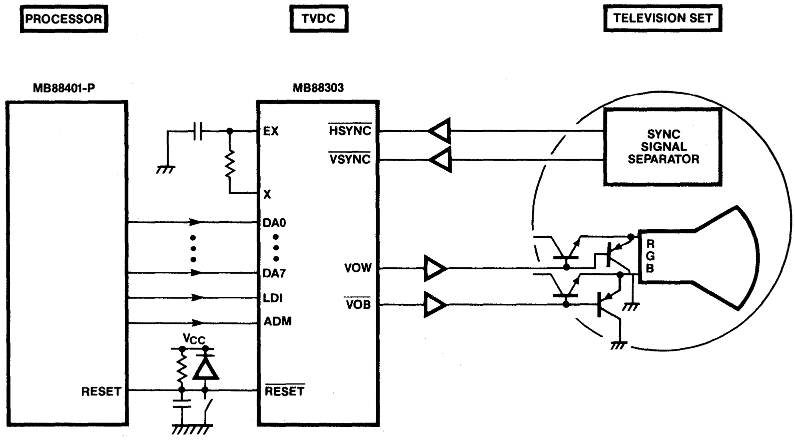


Notes:

1. For $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ input signals, both cycle and rise/fall times must be constant.
2. Character output during the blanking period of TV should be inhibited. If not, character shapes may change. So, blanks should be written for memory addresses which cannot be displayed on the screen.

Functional Description
(Continued)

Figure 15. Application Example



Absolute Maximum Ratings

Parameter	Symbol	Pin	Rating	Unit
Supply Voltage	V_{CC}	V_{CC}	V_{SS} -0.3 to V_{SS} +7.0	V
Input Voltage	V_{IN}	EX, $\overline{\text{RESET}}$, ADM, LDI, DA7-DA0	V_{SS} -0.3 to V_{SS} +7.0	V
Output Voltage	V_{OUT}	VOW, $\overline{\text{VOB}}$	V_{SS} -0.3 to V_{SS} +7.0	V
		DO0-DO2	V_{SS} -0.3 to V_{SS} +15	
Operating Temperature	T_A		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +150	°C
Power Dissipation	P_D		600	mW

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Pin	Value Min.	Value Typ.	Value Max.	Unit
Supply Voltage	V_{CC}	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	V_{SS}	—	0		
Input High Voltage	V_{IH}	DA7-DA0, ADM	2.0		V_{CC}	V
	V_{IHS}	$\overline{\text{RESET}}$, LDI VSYNC, HSYNC	3.0		V_{CC}	V
Input Low Voltage	V_{IL}	DA7-DA0, ADM $\overline{\text{RESET}}$, LDI VSYNC, HSYNC, EX	-0.3		0.8	V
Operating Temperature	T_A		-30		+70	°C
Operating Clock Frequency	f_c	EX, X			6.7	MHz

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value Min.	Value Typ.	Value Max.	Unit	Condition
Output High Voltage	V_{OH}	VOW, $\overline{\text{VOB}}$	2.4	—	—	V	V_{CC} = 4.5V, I_{OH} = -200μA
		DO2-DO0	Open Drain				
Output Low Voltage	V_{OL}	VOW, $\overline{\text{VOB}}$	—	—	0.4	V	V_{CC} = 4.5V, I_{OL} = 1.8mA
		DO2-DO0	—	—	0.4		V_{CC} = 4.5V, I_{OL} = 1.8mA, with 5kΩ external pull-up resistor
Output Leakage Current	I_{leak}	DO2-DO0	—	—	50	μA	V_{CC} = 5.5V, V_{OH} = 13.2V, at OFF state with with 5KΩ external pull-up resistor
Input Leakage Current	I_{IL}	$\overline{\text{RESET}}$, LDI, ADM, VSYNC, HSYNC, DA7-DA0	—	—	-60	μA	V_{CC} = 5.5V, V_{IL} = 0.4V
Supply Current	I_{CC}	V_{CC}	—	80	120	mA	V_{CC} = 5.5V, All outputs open, f_c = 6.7MHz, reset state

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value		Unit	Condition
			Min.	Max.		
LDI Pulse Width	t_{WLDI}	LDI	5		μs	Fig. 15, Fig. 18
LDI Rise/Fall Time	t_{rLDI} t_{fLDI}	LDI		1	μs	Fig. 15, Fig. 18
ADM Setup Time	t_{AS}	ADM	0.5		μs	Fig. 15, Fig. 18
ADM Hold Time	t_{AH}	ADM	2		μs	Fig. 15, Fig. 18
Address/Data Setup Time	t_S	DA0 to DA7	0.5		μs	Fig. 15, Fig. 18
Address/Data Hold Time	t_H	DA0 to DA7	2		μs	Fig. 15, Fig. 18
DO Output Delay Time	t_{DD}	DO0 to DO2		0.6	μs	Fig. 16, Fig. 18
$\overline{\text{RESET}}$ Pulse Width	t_{RST}	$\overline{\text{RESET}}$	4		μs	Fig. 17, Fig. 18
$\overline{\text{RESET}}$ Setup Time	t_{RSTS}	$\overline{\text{RESET}}$	1		μs	Fig. 17, Fig. 18
$\overline{\text{RESET}}$ Hold Time	t_{RSTH}	$\overline{\text{RESET}}$	3		μs	Fig. 17, Fig. 18

Figure 15. Address/Data Input Timing

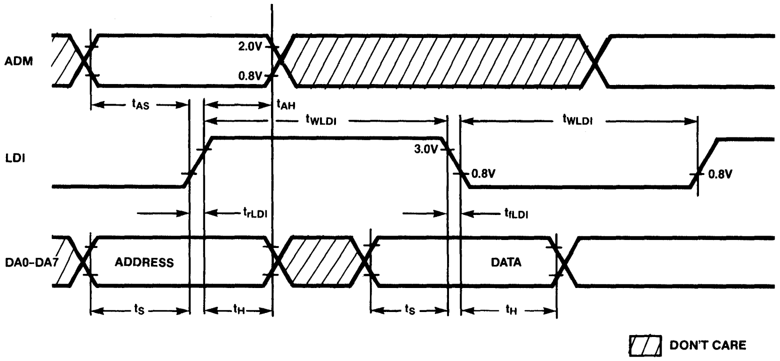


Figure 16. DO Output Timing

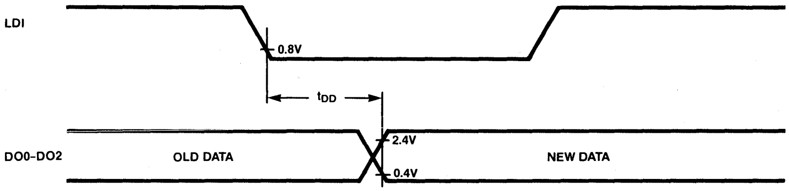
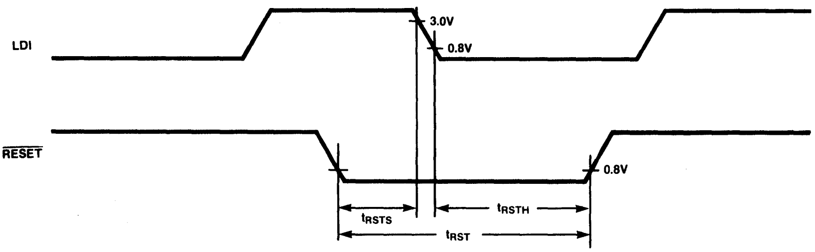
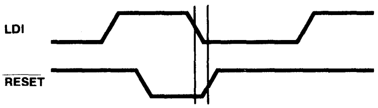


Figure 17. RESET Input Timing



Notes:

1. If t_{RSTS} spec. (1μs min.) is not met, the MB88303 cannot be reset.
2. If t_{RSTH} spec. (3μs min.) is not met, then the TV screen will be disturbed. This is caused by the undefined data on the DA line written into internal registers and display memory at LDI's high-to-low transition during RESET = "L". This case occurs, for example, when RESET goes high just after LDI goes low, shown at top, right diagram. This unacceptable RESET timing is caused when the device is reset separately from the processor connected to the device. However, when LDI level is fixed high or low during reset (i.e. RESET = "L") shown at bottom right diagram, the TV screen is not disturbed.



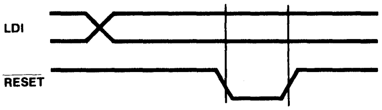
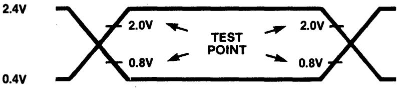


Figure 18. AC Test Conditions

Input Conditions

Timing Reference Levels:

3.0V for a logic "1" (RESET, LDI)
2.0V for a logic "1" (ADM, DA7-DA0)
0.8V for a logic "0"



Output Conditions

Timing Reference Levels:

2.4V for a logic "1"
0.4V for a logic "0"

Output Load Circuit:

R_L = 4kΩ
C_L = 50pF
(including scope and jig capacitances)
*with external 5kΩ pull-up resistor at DO2-DO0 for t_{DD}

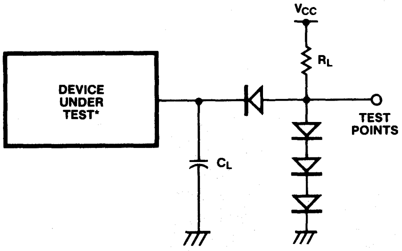
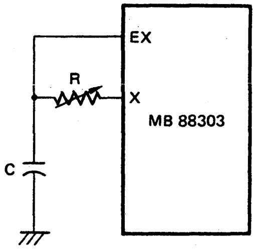


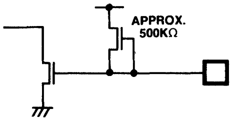
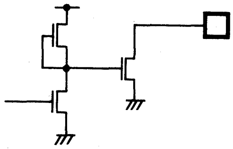
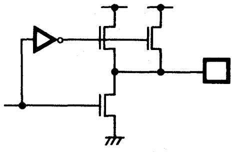
Figure 19. RC—Network Oscillator Circuit



Note: The clock frequency (fc) has wide variation from device to device. The clock frequency also considerably depends on the ambient temperature and supply voltage.

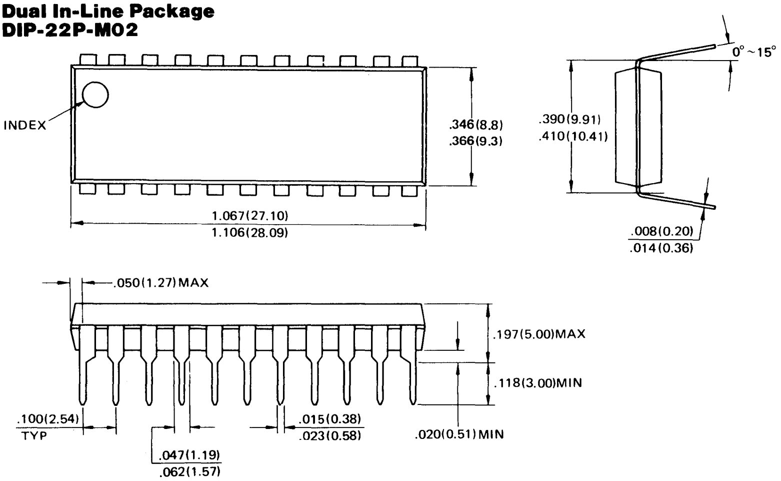
Therefore, to limit the clock frequency within the specified range, it is required to adjust it with the external resistor in advance.

I/O Circuit Configuration

Pin	Type	Circuit Diagram	Characteristics
$\overline{\text{RESET}}$ LDI ADM DA0-DA7 $\overline{\text{HSYNC}}$ $\overline{\text{VSYNC}}$	Input		***Pull Up Resistor:*** $I_{IL} \leqq 60\mu A$ at $V_{CC} = 5.5V$, $V_{IL} = 0.4V$
DO0-DO2	Output		***High-Voltage Open Drain:*** $I_{IL} \leqq 0.4V$ at $V_{CC} = 4.5V$, $V_{OL} = 1.8mA$,* $I_{leak} \leqq 50\mu A$ at $V_{CC} = 5.5V$, $V_{OH} = 13.2V$, OFF state,* *with external 5kΩ pull up resistor
VOW $\overline{\text{VOB}}$	Output		***Pull Up Resistor:*** $V_{OH} \geqq 2.4V$ at $V_{CC} = 4.5V$, $I_{OH} = -200\mu A$ $V_{OL} \leqq 0.4V$ at $V_{CC} = 4.5V$, $I_{OL} = 1.8mA$

Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Plastic Dual In-Line Package DIP-22P-M02



Preliminary

Advanced Products

FUJITSU

MB88313

October 1986

CMOS Television Display Controller (TVDC)

DESCRIPTION

The Fujitsu MB88313 CMOS Television Display Controller (TVDC) is a programmable interface LSI device, which displays 16 alphanumeric and symbol characters of a 32-character set in four colors on a standard color TV (NTSC, PAL, SECAM, etc.) screen under control of a general 4 or 8-bit microcomputer.

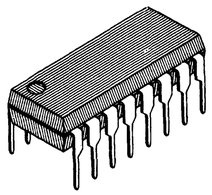
The MB88313 contains a display memory (16 x 8 bit static RAM), an address counter, six programmable control registers, a character generator (5 x 7 x 32-bit mask ROM), and a clock generator. 16 characters, of which codes are written into the display memory, and displayed on the TV screen, superimposed on the picture. Various screen features, such as screen format, character size, display start position, character attributes (color and blink), are controlled by programming the control registers using control commands serially loaded by the processor. The standard TVDC's character generator contains the Fujitsu standard character set. User designed character patterns are also acceptable on the mask ROM. The on-chip clock generator oscillates with an external RC or LC network.

The MB88313 is fabricated with the silicon-gate CMOS process, and packaged in a standard 16-pin plastic DIP or SOP. It operates with a single +5V power supply and 7 MHz clock over the ambient temperature range of −30°C to +70°C.

The MB88313 is suitable for display of simple character information on the TV screen, such as TV channel numbers, voice volume, VTR tape remainder and recording date and time, for which LCD or LED displays have been used.

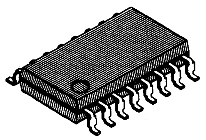
FEATURES

- External synchronization type character display controller
- Display method: Characters are superimposed on the picture of a TV screen synchronized with TV $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals
- Command drive method: Display memory and internal registers are programmed by eight 8-bit control commands serially loaded by the processor
- Programmable screen format:
  —8 characters x 2 lines
  —16 characters x 1 line
- Fixed character format: 5 x 7 dot matrix with automatic rounding function
- 32 mask programmable character patterns:
  —Fujitsu standard character set
  —User-designed character set



8313–1

Plastic DIP
(Suffix -P)
DIP-16P-M02



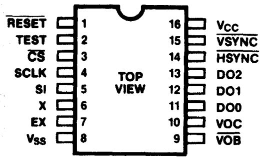
8313–2

Plastic SOP
(Suffix -PF)
FPT-16P-M02

FEATURES (Continued)

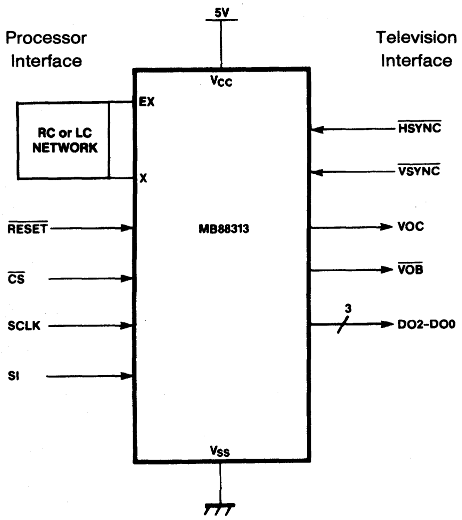
- Programmable character size:
  —4 selections for width
  —4 selections for height
- Programmable display position:
  —29 selections for horizontal position
  —31 selections for vertical position
- Programmable screen controls:
  —Screen format control
  —Background control
  —Blink control
  —Color control
- Interfaceable to general 4 & 8-bit microprocessors
- Interfaceable to standard color TV (NTSC, PAL, SECAM, etc.), standard monochrome TV sets, and interlace & non-interlace CRTs
- Seven programmable registers [address counter & control registers]
- 5 x 7 x 32-bit mask ROM [character generator]
- 16 x 8-bit static RAM [display memory]
- On-chip clock generator for external RC/LC components
- Silicon-gate CMOS process
- Single +5V power supply
- TTL compatible I/O ports
- Up to 7 MHz clock
- −30°C to +70°C operating temperature range
- Two package options:
  —16-pin DIP (Suffix -P)
  —16-pin SOP (Suffix -PF)

PIN ASSIGNMENT AND LOGIC SYMBOL



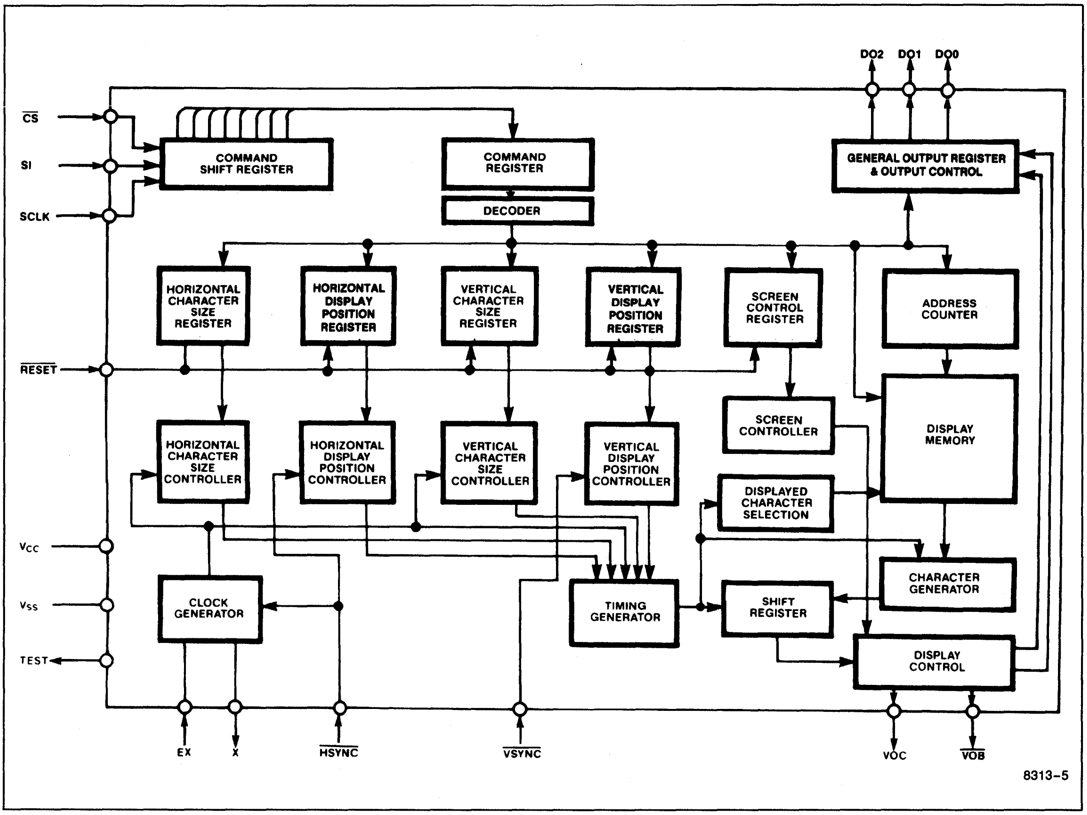
8313-3

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



8313-4

BLOCK DIAGRAM


DO2
DO1
DO0
CS
SI
SCLK
COMMAND SHIFT REGISTER
COMMAND REGISTER
DECODER
GENERAL OUTPUT REGISTER & OUTPUT CONTROL
HORIZONTAL CHARACTER SIZE REGISTER
HORIZONTAL DISPLAY POSITION REGISTER
VERTICAL CHARACTER SIZE REGISTER
VERTICAL DISPLAY POSITION REGISTER
SCREEN CONTROL REGISTER
ADDRESS COUNTER
RESET
SCREEN CONTROLLER
DISPLAY MEMORY
HORIZONTAL CHARACTER SIZE CONTROLLER
HORIZONTAL DISPLAY POSITION CONTROLLER
VERTICAL CHARACTER SIZE CONTROLLER
VERTICAL DISPLAY POSITION CONTROLLER
DISPLAYED CHARACTER SELECTION
VCC
VSS
TEST
CLOCK GENERATOR
TIMING GENERATOR
SHIFT REGISTER
CHARACTER GENERATOR
DISPLAY CONTROL
EX
X
HSYNC
VSYNC
VOC
VOB
8313-5

PIN DESCRIPTION

The MB88313 TVDC has two interfaces: One is the processor interface consisting of, $\overline{\text{CS}}$, SCLK, and SI inputs which are used for the processor to serially load control commands into the TVDC. The other is the television interface, consisting of, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs and VOC, $\overline{\text{VOB}}$ and DO2–DO0 outputs which are used for the TVDC to display characters on the TV screen.

Table 1. Pin Description

Symbol	Number	Type	Name & Function
• Power Supply & Clock			
V_{CC}	16	—	+ 5 V dc power supply pin.
V_{SS}	8	—	Power supply ground pin.
EX X	7 6	I O	Oscillator input/output: With an external capacitor (C) and resistor (R) or, inductor (L) and capacitors (C) connected to the EX and X pins, the on-chip oscillator generates the internal clock. A clock frequency is determined by the values of R and C, or L and C.
TEST	2	O	Test output: This output pin is enabled in the test mode, which is used for the shipping test purposes only at Fujitsu. In the normal operation mode, this output pin is low, and may be left open.
• Processor Interface			
$\overline{\text{RESET}}$	1	I	Reset input: A low level on the $\overline{\text{RESET}}$ pin stops the TVDC's operations, initializes the internal control registers and clamps the outputs as follows: 1. Horizontal/vertical character size registers, horizontal/vertical display position registers, screen control register and general output register are all cleared. 2. All inputs are inactive. 3. VOC and DO2–DO0 output pins are clamped low, and $\overline{\text{VOB}}$ is clamped high. The display memory is not affected by the $\overline{\text{RESET}}$. The command shift register, command register and address counter are undefined after a reset. After the $\overline{\text{RESET}}$ pin is driven high, the TVDC restarts its display operations. *This pin is a hysteresis input.*
$\overline{\text{CS}}$	3	I	Chip select input: A low level on the $\overline{\text{CS}}$ pin resets the internal SCLK counter, and enables the command shift register to receive serial data through the SI input pin.
SCLK	4	I	Shift clock input: The rising edge of the SCLK moves data on the SI pin into the command shift register, and also increments the internal SCLK counter.
SI	5	I	Serial command input: A command bit on the SI pin is shifted into the MSB of the command shift register at the rising edge of the SCLK. At the eighth rising edge, which is counted by the internal SCLK counter, an 8-bit command word is latched into the command register.
• Television Interface			
$\overline{\text{HYSNC}}$	14	I	Horizontal sync input: Horizontal synchronization pulse signal (negative pulse) provided by TV set should be applied to this input pin. The TVDC outputs character and background signals (VOC and $\overline{\text{VOB}}$) synchronously with this signal. *This pin is a hysteresis input.*
$\overline{\text{VSYNC}}$	15	I	Vertical sync input: Vertical synchronization pulse signal (negative pulse) provided by TV set should be applied to this input pin. The TVDC outputs character and background signals (VOC and $\overline{\text{VOB}}$) synchronously with this signal. *This pin is a hysteresis input.*

PIN DESCRIPTION (Continued)

Symbol	Number	Type	Name & Function
VOC	10	O	Video output for character: This pin outputs a high level for character dot patterns, and is clamped low during the reset mode, standby mode, and non-display mode, disabling character display on the TV screen.
$\overline{\text{VOB}}$	9	O	Video output for background: This pin outputs a low level for background or edge portion of character dot matrix during the background or edge mode, respectively. The $\overline{\text{VOB}}$ output is clamped high during the reset mode, standby mode, non-display mode, and non-background/edge mode, disabling background and edge displays on the TV screen.
DO2–DO0	13–11	O	Data outputs: These outputs are controlled by the GOC bit: When GOC = 0 (i.e., the general output mode), a 3-bit data in the on-chip general output register is output at these output pins. These are used for general control outputs. When GOC = 1 (i.e., the color display mode), the attribute code bits AC1 and AC0 are output at the DO1 and DO0 pins, respectively. These are used as color control data. The remaining bit of the general output register appears at the DO2 pin.

BLOCK DESCRIPTION

Refer to Block Diagram on page 3.

The MB88313 TVDC contains the following main functional blocks:

- Clock generator
- Character generator
- Display memory
- Address counter
- Command shift register and command register
- Six control registers

(Address counter, command shift register and command register, six control registers: Register Set)

Clock Generator

The MB88313 has an on-chip clock generator, which provides a basic timing clock to internal circuits. The clock frequency is determined by external RC or LC network.

For synchronization, the clock supply to the internal circuit is stopped while the $\overline{\text{HSYNC}}$ is low. The clock generator is stopped during the standby mode, which is initiated by software (Command 6).

Character Generator

The MB88313 has a 5 x 7 x 32 bit mask ROM as a character generator, which stores thirty-two 5 x 7-dot character patterns encoded into character codes. The character generator defines a character set. The standard MB88313 has the Fujitsu standard character set shown in Figure 15. Those characters are indicated by character codes shown in Table 5. A user-designed character set is also programmed on the mask ROM using metal option. But character codes, (0F)H and (1F)H are reserved as "blank" and "background" codes.

Display Memory

The MB88313 has a 16 x 8 bit static RAM as a display memory, which stores 16 character codes and their attribute codes to be displayed on the TV screen. The 16 memory locations are addressed by a 4-bit address counter (A3–A0). Figure 1 shows the display memory map: Each memory word is divided into two fields: The lower 5 bits (CH4–CH0) defines a character code, and the upper 3 bits (AC2–AC0) defines its attribute codes (color code and blink code). Each field of a word addressed by the address counter is written separately by the processor using Commands 0 and 6 respectively. See Table 1. The display memory is not affected by $\overline{\text{RESET}}$, and is retained during the standby mode.

Register Set

The MB88313 contains a register set consisting of an address counter, command shift register, command register, and six control registers, which are programmed using control commands or directly loaded by the processor. See Table 1.

Command Shift Register and Command Register (CM7–CM0)

The command shift register is an 8-bit serial-in/parallel-out shift register that assembles serial command bits (provided by the processor through the SI input synchronously with the SCLK input) into an 8-bit command word during the command load operation.

The command register is an 8-bit write-only register that holds control commands transferred in parallel from the command shift register. The transferred 8-bit command word is output to

BLOCK DESCRIPTION (Continued)

the command decoder to generate internal control signals. Figure 2 shows the command shift register and command register configuration.

Both registers are undefined after a reset, and hold the current state during the standby mode.

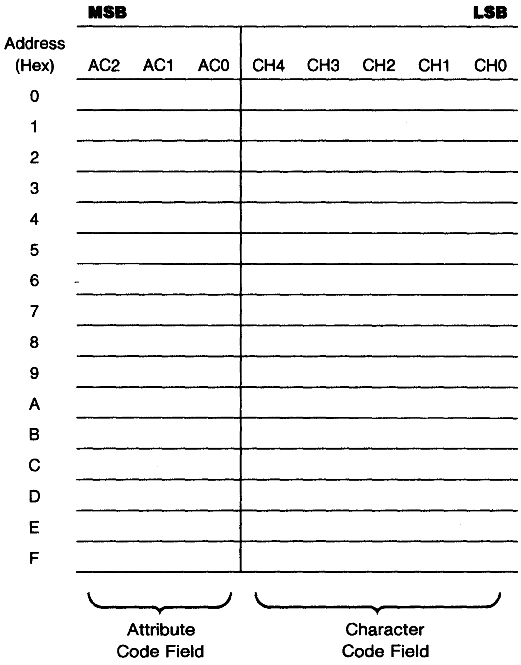
Address Counter (A3-A0)

The address counter is a 4-bit binary counter which addresses a display data memory location written by Commands 0 and 6. The address counter is preset by Command 1, and is automatically incremented by Command 0. Figure 3 shows the address counter format. The address counter is undefined after a reset, and holds the current state during the standby mode.

Horizontal Display Position Register (HP4-HP0)

The horizontal display position register is a 5-bit write-only register which selects one of 29 horizontal positions from where the first character (including blank and background) begins to appear on the screen. This control register is programmed by the processor using Command 2, and cleared by $\overline{\text{RESET}}$. Figure 4 shows the horizontal position register format. During the standby mode, this register holds the current state.

Figure 1. Display Memory Map



Notes:

1. Address is indicated by Address Counter, which is setup using Command 1.
2. Attribute code field is written by Command 6.
3. Character code field is written by Command 0.

Table 2. Display Memory & Register Set Summary

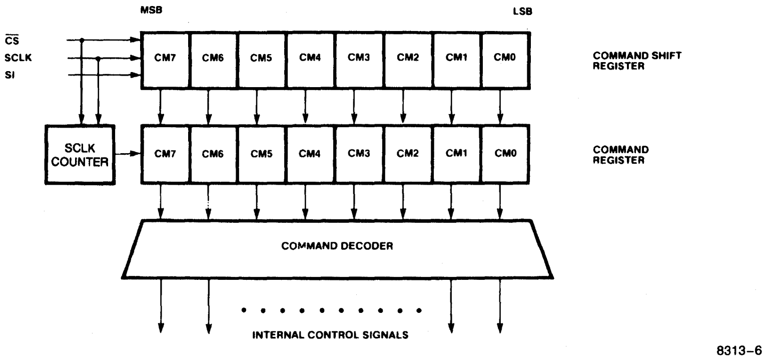
Register Name		Bit Symbol	Programming Method
Display Memory		AC2-AC0: CH4-CH0	Command 0, Command 6
Command Shift Register & Command Register		CM7-CM0	Serial Load & Parallel Latch
Address Counter		A3-A0	Command 1
Control Registers	Horizontal Display Position Register	HP4-HP0	Command 2
	Vertical Display Position Register	VP4-VP0	Command 3
	Horizontal Character Size Register	HS1-HS0	Command 4
	Vertical Character Size Register	VS1-VS0	Command 4
	Screen Control Register	SC4-SC0	Command 5
	General Output Register	GO2-GO0	Command 7

BLOCK DESCRIPTION (Continued)

Vertical Display Position Register (VP4–VP0)

The vertical display position register is a 5-bit write-only register which selects one of 31 vertical positions from which the first character (including blank and background) begins to appear on the screen. This control register is programmed by the processor using Command 3, and is cleared by $\overline{\text{RESET}}$. Figure 5 shows the vertical position register format. During the standby mode, this register holds the current state.

Figure 2. Command Register Configuration



Note:
Command register is written by the processor through command shift register.

Figure 3. Address Counter Format

MSB			LSB
A3	A2	A1	A0

Note:
Address counter is programmed by Command 1.

Figure 4. Horizontal Position Register Format

MSB				LSB
HP4	HP3	HP2	HP1	HP0

Notes:

1. HP = T × (4 × (2^5HP4 + 2^4HP3 + 2^3HP2 + 2^2HP1 + 2HP0) + P)
   Where, P = 10, 11, 12 and 13 for (HS1, HS0) = (0,0), (0,1), (1,0) and (1,1), respectively
   HP: Horizontal display start position; referenced to the rising edge of $\overline{\text{HSYNC}}$
   T: Clock Cycle time; T(S) = 1/fc [Hz]
2. Horizontal position register is programmed by Command 2.

Figure 5. Vertical Position Register Format

MSB				LSB
VP4	VP3	VP2	VP1	VP0

Notes:

1. VP = H × 4 × (2^5VP4 + 2^4VP3 + 2^3VP2 + 2^2VP1 + 2VP0) + 1)
   Where, VP: Vertical display start position; referred to the rising edge of $\overline{\text{VSYNC}}$
   H: Horizontal sync cycle time; H = 63.5 [μs]
2. Vertical position register is programmed by Command 3.

Table 3. DO Outputs in Color Display Mode

Video Signal		DO Outputs			Display
$\overline{\text{VOB}}$	VOC	DO2 = GO2	DO2 = AC1	DO0 = AC0	
X	1	X	0	0	Character
			0	1	
			1	0	
			1	1	
1	0	0	0	X	Blank
0					Black (Background)

BLOCK DESCRIPTION (Continued)

Horizontal Character Size Register (HS1 and HS0)

The horizontal character size register is a 2-bit write-only register which selects one of 4 character widths. This control register is programmed by the processor using Command 4, and cleared by RESET. Figure 6 shows the horizontal character size register format. During the standby mode, this register holds the current state.

Vertical Character Size Register (VS1 and VS0)

The vertical character size register is a 2-bit write-only register which selects one of 4 character heights. This control register is programmed by the processor using Command 4, and cleared by RESET. Figure 7 shows the vertical character size register format. During the standby mode, this register holds the current state.

Screen Control Register (SC4–SC0)

The screen control register is a 5-bit write-only register which controls screen features: Screen format, display mode, and blinking. This control register is programmed by the processor using Command 5, and cleared by RESET. Figure 8 shows the screen control register format and bit functions. During the standby mode, this register holds the current state.

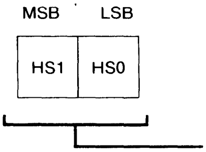
Note:

When the display is disabled (SC0 = 0), the background must be also disabled (SC1 = 0).

General Output Register (GO2–GO0)

The general output register is a 3-bit write-only output register which latches 3-bit output data written into by Command 7. Depending on the general output register control bit GOC, the TVDC has two output modes for the DO2–DO0 pins. During the general output mode (GOC = "0"), the latched data appears at

Figure 6. Horizontal Character Size Register Format

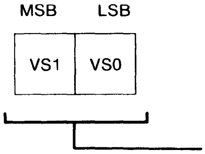


Horizontal Size Code		Horizontal Character Size (Width)	Horizontal Dot Size
HS1	HS0		
0	0	10T	2T
0	1	20T	4T
1	0	30T	6T
1	1	40T	8T

8313-7

Notes:
1. T: Clock cycle time; T[s] = 1/fc [Hz]
2. Horizontal character size register is programmed by Command 4.

Figure 7. Vertical Character Size Register Format



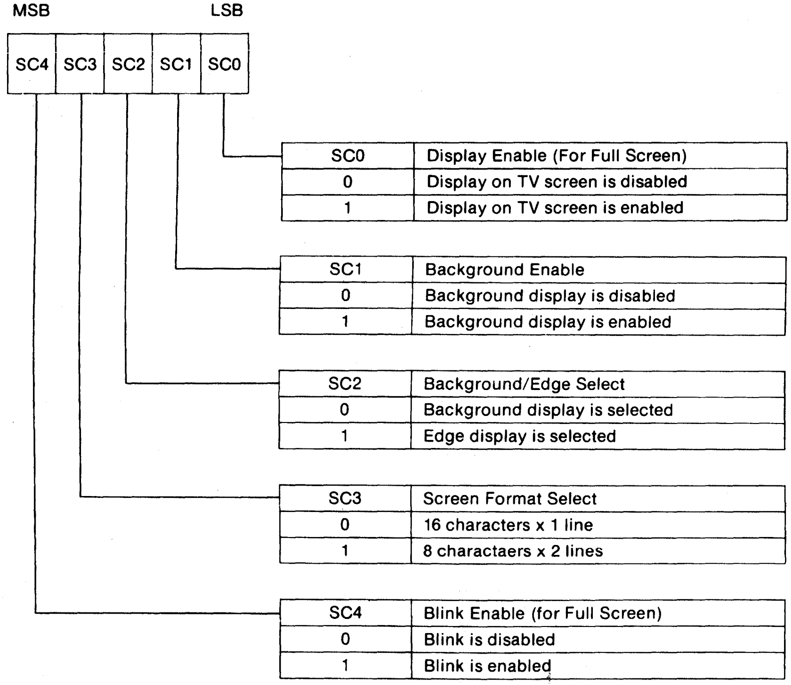
Vertical Size Code		Vertical Character Size (Height)	Vertical Dot Size
VS1	VS0		
0	0	14H	2H
0	1	28H	4H
1	0	42H	6H
1	1	56H	8H

8313-8

Notes:
1. H: Horizontal sync cycle time; H = 63.5 [μs]
2. Vertical character size register is programmed by Command 4.

BLOCK DESCRIPTION (Continued)

Figure 8. Screen Control Register Format



SC0	Display Enable (For Full Screen)
0	Display on TV screen is disabled
1	Display on TV screen is enabled

SC1	Background Enable
0	Background display is disabled
1	Background display is enabled

SC2	Background/Edge Select
0	Background display is selected
1	Edge display is selected

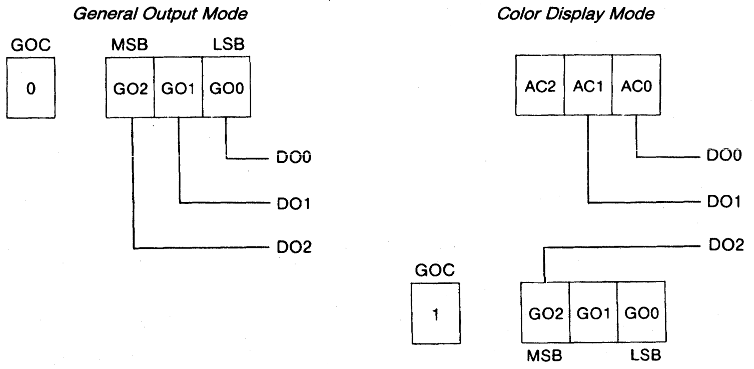
SC3	Screen Format Select
0	16 characters x 1 line
1	8 charactaers x 2 lines

SC4	Blink Enable (for Full Screen)
0	Blink is disabled
1	Blink is enabled

8313-9

Note:
Screen control register is programmed by Command 5.

Figure 9. General Output Register Format



8313-10

Note:
General output register is programmed by Command 7.

BLOCK DESCRIPTION (Continued)

the DO2–DO0 output pins. During the color display mode (GOC = "1"), the color code bits AC1 and AC0 stored in each attribute field of the display memory are automatically output on the DO1 and the DO0 pins respectively while the VOC output is high. When the VOC is low, the DO1 and DO0 pins are clamped low. The GO2 bit only appears at the DO2 in the color display mode. See Table 3. Controlling RGB signals by the DO1 and DO0 and VOC, four-colored characters can be displayed.

This control register and control bit GOC are programmed by the processor using Command 7, and cleared by $\overline{\text{RESET}}$. Figure 9 shows the general output register format. During the standby mode and non-display mode, the DO2–DO0 output are clamped low, regardless of the general output mode or the color display mode.

FUNCTIONAL DESCRIPTION

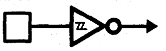
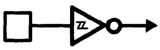
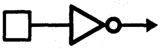
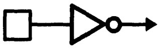
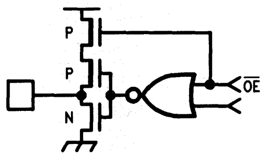
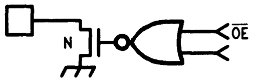
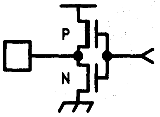
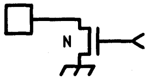
The MB88313 TVDC is an external synchronization type programmable character display controller. Under control of a 4 or 8-bit general microprocessor, it displays 16 characters of 32-character set with various character attributes (color and blink) and screen features (screen format, character size, and display position) on a standard monochrome or color TV screen, superimposed on the picture. The MB88313 can interface to NTSC, PAL and SECAM standard color TV set, and also to the raster scan type CRT, regardless of interlace or noninterlace scan.

The MB88313 has three operation modes; the active mode, standby mode and reset mode. The active mode operations are described on pages 10–16. Both Standby mode operations, and Reset mode operations are described starting on page 17.

Active Operations

Character & attribute codes and feature control codes are written into the on-chip display memory and control registers by the processor using control commands, respectively. The control commands are serially loaded into the on-chip command register through the processor interface pins, $\overline{\text{CS}}$, SCLK, and SI. According to the programmed character & attribute codes and control codes, the MB88313 issues the character & background video signals from the VOC and $\overline{\text{VOB}}$ pins synchronously with $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$, signals provided by the TV set. Also, the DO2–DO0 outputs are used as color control or other general control signals to the TV set.

INPUT/OUTPUT CIRCUITS

TYPE	PIN	MB88306/308	MB88307/309
INPUTS	$\overline{\text{LOAD}}$ SC ($\overline{\text{SC}}$) $\overline{\text{RESET}}$	HYSTERESIS INPUT 	HYSTERESIS INPUT 
	$\overline{\text{OE}}$ SI	NON-HYSTERESIS INPUT 	NON-HYSTERESIS INPUT 
OUTPUTS	$O_7 - O_0$	CMOS 3–STATE OUTPUT 	NMOS OPEN–DRAIN OUTPUT 
	SO	CMOS OUTPUT 	NMOS OPEN–DRAIN OUTPUT 

8313-11

FUNCTIONAL DESCRIPTION (Continued)

Command Load Operation

The processor serially loads 8-bit commands into the TVDC's command shift register using the processor inputs, $\overline{CS}$, SCLK and SI. The loaded command is parallel latched into the command register. According to the command, control data is written into a designated memory location, address counter, or control register.

Figures 10 and 11 show the command register configuration and command load timing: A low level on the $\overline{CS}$ pin initializes the SCLK counter and enables the command shift register to receive command words. Then, synchronously with the SCLK shift clock input, an 8-bit command word is serially loaded into the command shift register through the SI input pin. At the rising edge of SCLK, a command bit on the SI pin is shifted into the MSB of the command shift register and at the same time the command shift register bits are right shifted. The rising edge of SCLK is counted by the SCLK counter, and at the eighth rising edge, the 8-bit command word is latched into the command register, where the first-in bit is the LSB and the last-in bit is the MSB. After that, the command is decoded to generate internal control signals.

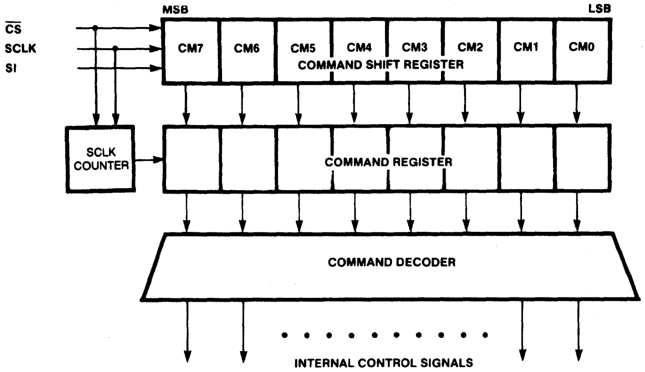
Note:

In successive command loading a few hundred ns after completion of one command loading, the next loading should not be made.

Display Operations

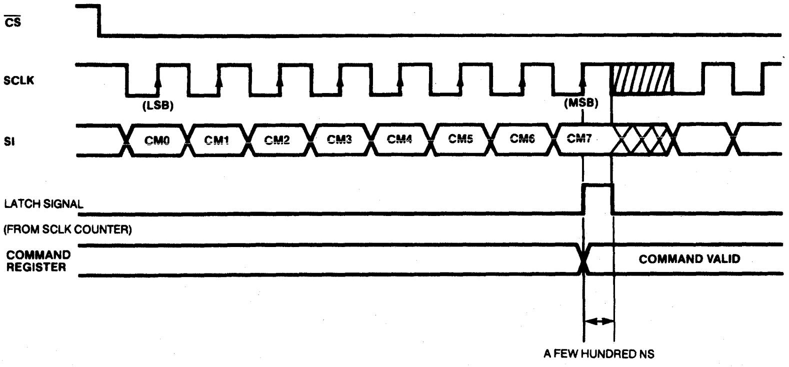
According to programmed display memory and control registers, the MB88313 issues video signals, VOC and $\overline{VOB}$ for character patterns synchronously with $\overline{HSYNC}$ and $\overline{VSYNC}$ signals supplied by the TV set, and also outputs feature control signals on the DO2–DO0 pins.

Figure 10. Command Register Configuration



8313-12

Figure 11. Command Load Timing



8313-13

FUNCTIONAL DESCRIPTION (Continued)

Screen Format Control

The MB88313 can display 16 characters in the format of 16 characters x 1 line (with one-dot horizontal spacing) or 8 characters x 2 lines (with one-dot horizontal & two-dot vertical spacings) on the TV screen. Either format can be selected by controlling the SC3 bit using Command 5: SC3 = "1" for 16 characters x 1 line, and SC3 = "0" for 8 characters x 2 lines. Figure 12 shows the two screen formats.

Character Format and Automatic Rounding Function

The character patterns are formatted as 5 x 7 dot matrix, stored in the on-chip character generator mask ROM. Figure 13 shows the character format. But, on the actual TV screen, this format is modified by the automatic rounding function. See Figure 14-1: When the internal original dot pattern (i.e., raw output signal from the character generator) contains diagonally aligned dots, a dot is automatically inserted between every diagonal dot to smooth the character form. Figure 14-2 shows an example of this rounding function.

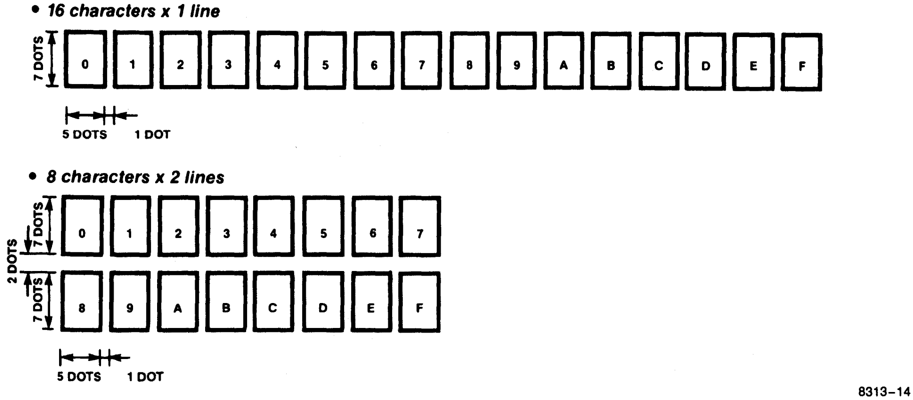
Character Patterns and Codes

The MB88313 has a character set of 32 character patterns, which is defined by the on-chip character generator mask ROM. Figure 15 shows the standard character set. Each character pattern is encoded as shown in Table 5. The MB88313 can also have user-designed character set (except blank and background) by programming the mask ROM.

Display Mode Control (Character/Background Control)

One of four display modes can be selected by the five screen control bits SC4–SC0 using Command 5, as shown in Table 4. Figure 16 shows examples of the display states, as well as the VOC and $\overline{\text{VOB}}$ output timing signals on line AA′ for character codes of 1, 2, blank, background, 3, and 4 in the three display modes, except the non-display mode.

Figure 12. Screen Format



Note:
Each box represents one character display area (5 x 7 dots). The hexadecimals represent display memory addresses.

Table 4. Display Mode Control

Screen Control Bits					
SC4	**SC3**	**SC2**	**SC1**	**SCO**	**Display Modes**
X	X	X	X	0	Non Display Mode: No characters nor background are displayed
X	0	X	0	1	Non-Background/Edge Mode: Characters are displayed, nor background
X	0	0	1	1	Edge Mode: Edged characters are displayed
X	0	1	1	1	Background Mode: Characters with black background are displayed

FUNCTIONAL DESCRIPTION (Continued)

Display Start Position Control

The horizontal and vertical display start positions on the TV screen are defined by the horizontal and vertical display position registers. Programming these control registers using Commands 2 and 4, the display start position (HP, VP) can be determined. For the horizontal position, 29 selections, and for the vertical position, 31 selections are possible. Figure 17 shows the definition of the display start position.

The horizontal display start position HP (from the rising edge of $\overline{\text{HSYNC}}$ to the falling edge of $\overline{\text{VOB}}$) and the vertical display start position VP (from the rising edge of $\overline{\text{VSYNC}}$ to the falling edge of $\overline{\text{VOB}}$) are calculated from programmed values of HP5 to HP0 and VP5 to VP0 using the following equations:

$HP = T \times 4 \times [(2^5 \times HP5 + 2^4 \times HP4 + 2^3 \times HP3 + 2^2 \times HP2 + 2 \times HP1 + HP0) + P]$

$VP = H \times 4 \times (2^5 \times VP5 + 2^4 \times VP4 + 2^3 \times VP3 + 2^2 \times VP2 + 2 \times VP1 + VP0)$

Where: P = 9, 10, 11, 12 for (HS1, HS0) = (0,0), (0,1), (1,0), and (1,1) respectively

T = Clock (oscillation) cycle time [7 MHz max.]

H = Horizontal sync cycle time [63.5 μs typ.]

Character Size Control

The character width and height on the TV screen are defined by the horizontal and vertical character size registers. Programming these control registers using Command 4, the character size can be determined. As shown in Tables 6 and 7, 4 selections are possible for each of the horizontal and vertical sizes.

Blink Control

The MB88313 can blink any desired character(s) on the TV screen. Blinking function is enabled when the SC4 bit of the screen control register is set to "1". Blinking effects only those characters for which the AC2 bit (blink control bit) is set to "1". Blinking characters appear for approximately 0.5s and disappear for the same period (vertical sync pulse cycle time × 64).

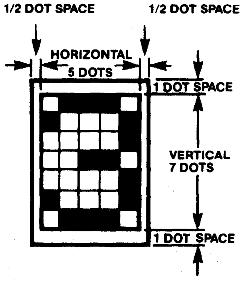
Blinking can be set as follows:

1. Preset a display memory address where the character blink is required, using Command 1.

2. Set the AC2 bit (blink control bit) of the location of the address, using Command 6.

3. Set the SC4 bit (blink enable bit) of the screen control register, using Command 5.

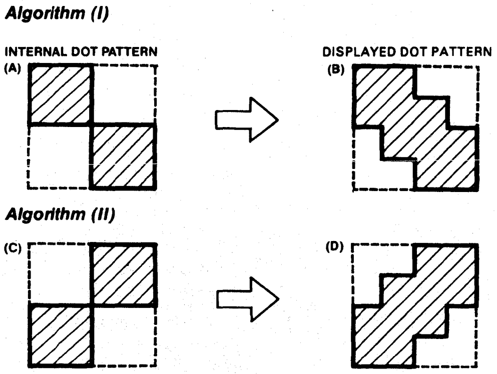
Figure 13. Character Format



8313-15

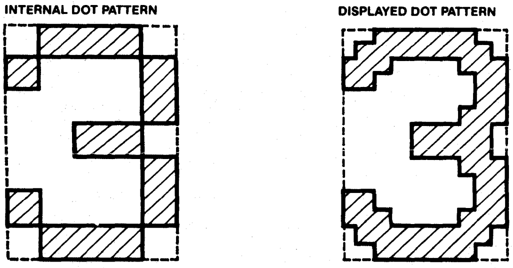
Note:
Each box presents one dot, and hatched boxes indicate displayed dots.

Figure 14-1. Automatic Rounding Function (Algorithm)



8313-16

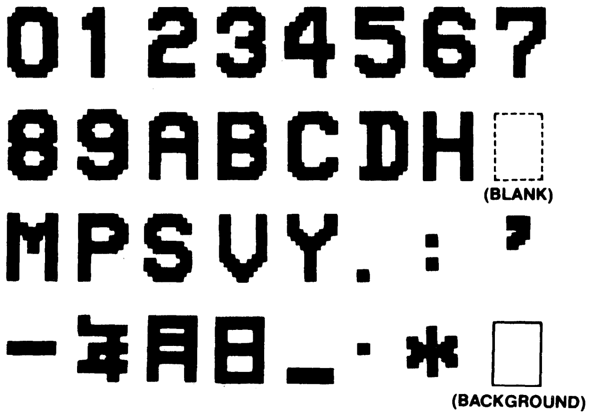
Figure 14-2. Automatic Rounding Function (Example)



8313-17

FUNCTIONAL DESCRIPTION (Continued)

Figure 15. Standard Character Set (Character Patterns)



8313-18

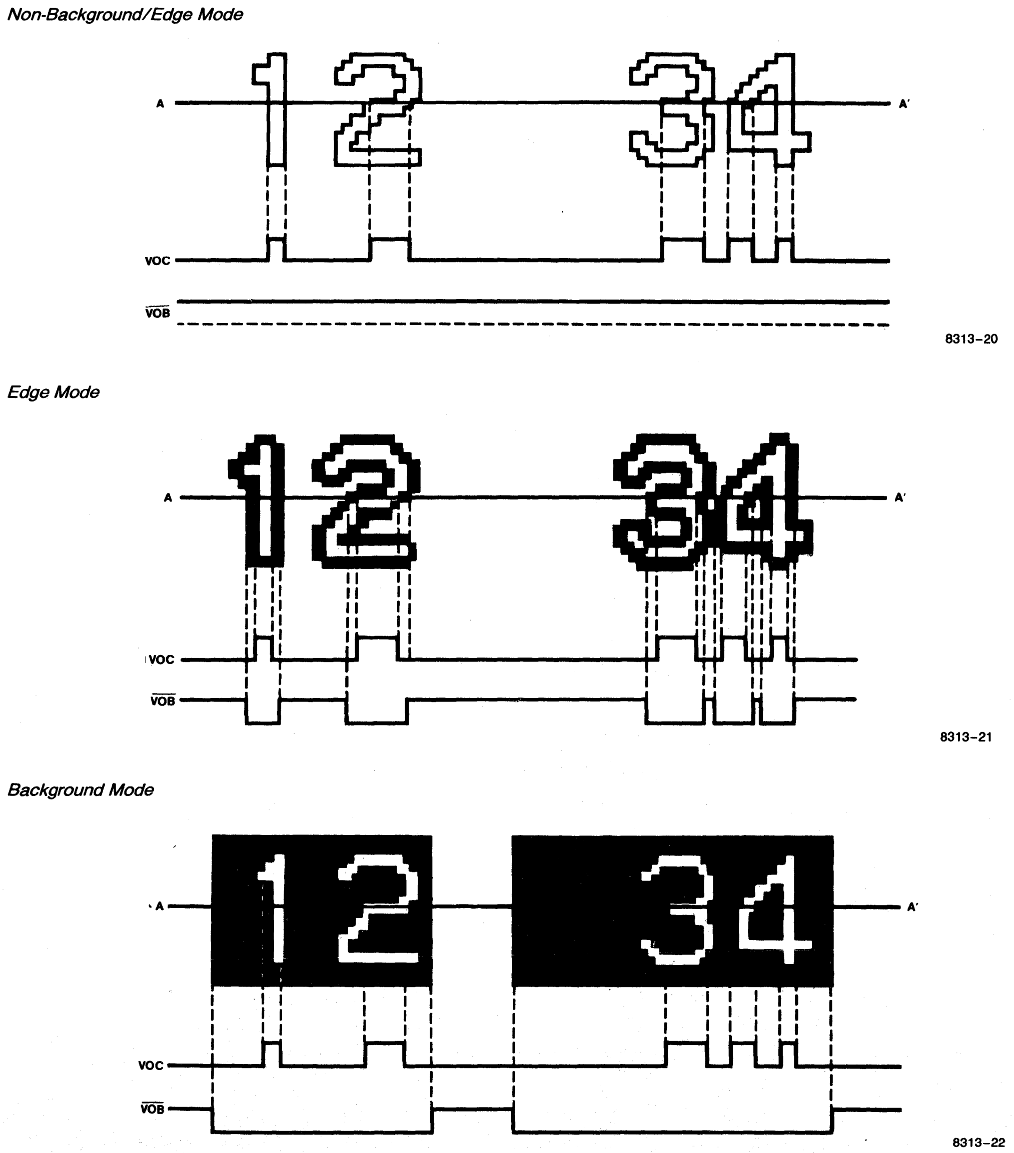
Table 5. Standard Character Codes

CH4 CJ3-CH0	0	1
0	0	M
1	1	P
2	2	S
3	3	V
4	4	Y
5	5	. (Period)
6	6	: (Colon)
7	7	' (Apostrophe)
8	8	- (Hyphen)
9	9	年 Kanji (Year)
A	A	月 Kanji (Month)
B	B	日 Kanji (Day)
C	C	_ (Underline)
D	D	• (Dot)
E	H	* (Asterisk)
F	▨ (Blank)	□ (Background)

8313-19

FUNCTIONAL DESCRIPTION (Continued)

Figure 16. Display Modes and VOC & $\overline{\text{VOB}}$ Output Timing



Non-Background/Edge Mode

8313-20

Edge Mode

8313-21

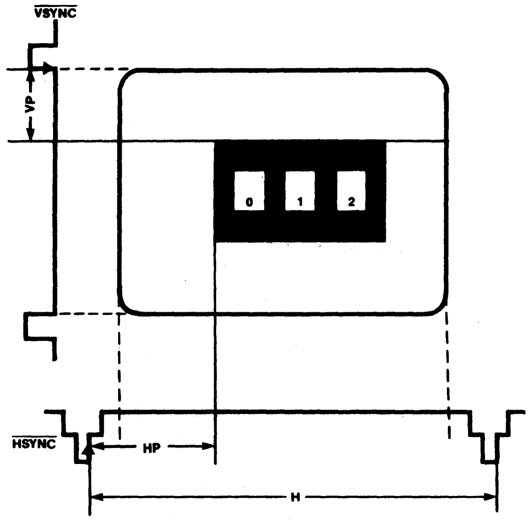
Background Mode

8313-22

Note:
During the non-display mode, the VOC and $\overline{\text{VOB}}$ outputs are clamped low and high, respectively, disabling display on TV screen.

FUNCTIONAL DESCRIPTION (Continued)

Figure 17. Display Start Position



8313-23

Table 6. Horizontal Character Size

Horizontal Size Code		Horizontal Character Size (Width)	Horizontal Dot Size
HS1	HS0		
0	0	10T	2T
0	1	20T	4T
1	0	30T	6T
1	1	40T	8T

Note:
T: Clock cycle time
T [s] = 1/fc [Hz]

Table 7. Vertical Character Size

Vertical Size Code		Vertical Character Size (Height)	Vertical Dot Size
VS1	VS0		
0	0	14H	2H
0	1	28H	4H
1	0	42H	6H
1	1	56H	8H

Note:
H: Horizontal sync cycle time
H = 63.5 [μs]

Functional Description (Continued)

Color Control

The MB88313 has a color display mode, in which color control signals are output on the DO1 and DO0 pins, in addition to the VOC and $\overline{\text{VOB}}$ signals. The color display mode is initiated by setting the GOC bit to "1" using Command 7. During this mode, the color code bits AC1 and AC0 stored in each attribute field of the display memory are automatically output on the DO1 and DO0 pins respectively, while the VOC output is high. When the VOC is low, the color control signals are clamped low. Controlling RGB signals of the color TV set by the VOC, DO1 and DO0 signals, characters are displayed in four of eight colors shown in Table 8. One of four colors is selected for each character by writing color codes to each attribute field of the display memory. Four colors to be displayed are selected by a combination of connections between MB88313's VOC/DO1/DO0 and TV's RGB pins.

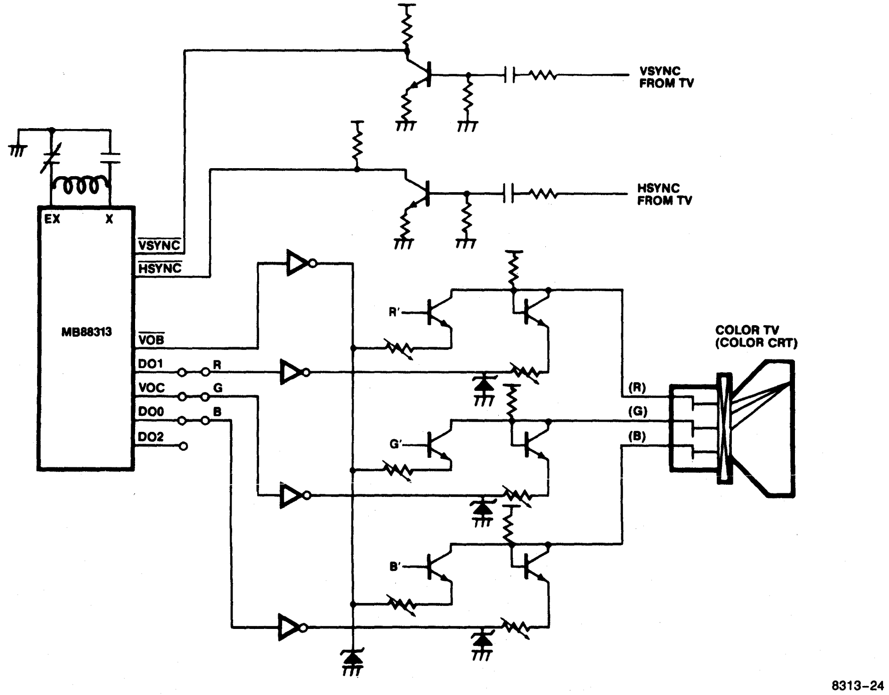
Figure 18 shows an example circuit for selecting character colors: green, cyanogen, yellow and white.

In this example circuit, the $\overline{\text{VOB}}$ (background) signal is used to inhibit all TV color video signals R'G'B' simultaneously. When the $\overline{\text{VOB}}$ is low, the R'G'B' signals are all disabled to create a black background. When the $\overline{\text{VOB}}$ is high, the R'G'B' signals are enabled to display TV signal. The VOC (character) signal and the DO1 & DO0 (i.e., AC1 & AC0) color code outputs are used to enable color character signals R, G, B, respectively, RGB and R'G'B' signals control (R)(G)(B) signals of the CRT in parallel.

Table 8. Displayable Colors

R	G	B	Displayed Colors
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyanogen
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Figure 18. TV Interface Configuration (Example)



Note:
R'G'B' are TV RGB signals.

FUNCTIONAL DESCRIPTION (Continued)

Table 9. Color Control (In Color Display Mode: GOC = "1")

Video Signals		**Color Control Codes**		
$\overline{\text{VOB}}$	**VOC (G)**	**AC1 = DO1 (R)**	**AC0 = DO0 (B)**	**Displayed Colors**
X	1	0	0	Green (RB: disabled)
		0	1	Cyanogen (R: disabled)
		1	0	Yellow (B: disabled)
		1	1	White (RGB: enabled)
1	0	0	0	Blank (RGB: disabled, R'G'B': enabled)
0		0	0	Black (Background) (RGB and R'G'B': disabled)

Standby Operation

The MB88313 has a low power standby mode (i.e., clock stop mode) which is initiated by software. A logic "1" on the STP bit stops the on-chip clock generator, reducing the power dissipation, and sets the internal states and input/output pin states, as follows:

1. All internal control registers, display memory, address counter, and command shift & command registers keep their current states.
2. All input pins are inactive.
3. Output pins hold the states before the standby mode.

During the standby mode, characters disappear on the TV screen.

When the STP bit is reset to "0", the clock generator restarts, and characters reappear on the screen. The STP is controlled by Command 6.

Notes:

1. When the STP bit is reset and the clock generator restarts, the vertical display position of each character is disturbed in the first screen field. To avoid this problem, the following procedure is recommended when resetting the STP bit:
   1) Before resetting, disable the screen display, resetting the SC0 bit with Command 5.
   2) Reset the STP bit using Command 6.
   3) At least 16.7 ms after resetting the STP bit, set the SC0 bit, enabling the screen display.
2. When set/reset the STP bit using Command 6, the AC2–AC0 bits addressed by the current address counter may change also.

Reset Operation

A low level on the $\overline{\text{RESET}}$ pin stops the TVDC's operations, and initializes its internal control registers and input/output pins to the following states:

1. All internal control registers are cleared.
2. All input pins are inactive.
3. VOC and DO2–DO1 output pins are clamped low, and $\overline{\text{VOB}}$, clamped high.

The display memory data is not affected by $\overline{\text{RESET}}$. The command shift register, command register, and address counter are undefined after $\overline{\text{RESET}}$.

During the reset mode, characters are not displayed on the TV screen because the output pins are deactivated as mentioned in item 3 above.

After the $\overline{\text{RESET}}$ pin is driven high, the TVDC restarts its normal operations. But, VOC, $\overline{\text{VOB}}$, and DO2–DO1 outputs remain deactivated, that is, no character is displayed on the TV screen, until the SC0 screen enable bit is set in the screen control register.

COMMAND DESCRIPTION

Command Set

The MB88313's display memory, address counter, and control registers are programmed using control commands. The MB88313 can accept eight 8-bit display control commands. These commands are serially loaded into the command register by the processor, and write their operand field data (control codes) into the display memory, address counter, and control registers. According to the programmed registers and memory, the MB88313 displays characters on the TV screen. The command format and functions are shown in Table 10. The upper 3 bits define op code, and the lower 5 bits are operand (control code).

Command 0 (Character Code Set)

Command 0 writes its lower 5 bits (character code: CH4–CH0) into character code field of a display memory location indicated by the address counter, and then increments the address counter. For the command format, see Table 6.

Command 1 (Address Preset)

Command 1 writes the lower 4 bits (display memory address: A3–A0) into the address counter, which addresses a display memory location into which Commands 0 and 6 write character and attribute codes. For the command format, see Table 10.

Note:
Bit 4 should be "0".

Command 2 (Horizontal Display Position Control)

Command 2 writes its lower 5 bits (horizontal display position code: HP4–HP0) into the horizontal display position register. Values of (00000) to (00010) can not be used as HP4–HP0. For the command format, see Table 10.

Command 3 (Vertical Display Position Control)

Command 3 writes its lower 5 bits (vertical display position code: VP4–VP0) into the vertical display position register. For the command format, see Table 10.

Command 4 (Character Size Control)

Command 4 writes its lower 2 bits (horizontal character size code: HS1 and HS0) and the next 2 bits (vertical character size code: VS1 and VS0) into the horizontal character size register and the vertical character size register, respectively. For the command format, see Table 10.

Note:
Bit 4 should be "0".

Command 5 (Screen Control)

Command 5 writes its lower 5 bits (screen control bits: SC4–SC0) into the screen control register to control various screen features. For the command format, see Table 10.

Command 6 (Attribute Control)

Command 6 writes its lower 3 bits (attribute codes: AC2 and AC1–AC0) into the attribute field of a display memory location indicated by the address counter. Note that this command does not increment the address counter, differently from Command 0. This command sets/resets Bit 4 to initiate/release the standby mode (clock stop mode). Bit 3 should be "0". For the command format, see Table 10.

Command 7 (General Output Control)

Command 7 writes its lower 3 bits (general output data: GO2–GO0) into the general output register, and sets/resets Bit 4 (general output control bit: GOC). For the command format, see Table 10.

NOTICE

1. The test mode is initiated by test mode command (code = 00111XXX), and is released by a low level on the $\overline{\text{HSYNC}}$ pin. In the test mode, output operations of the VOC, $\overline{\text{VOB}}$ and DO2–DO1 pins are different from in the normal operation mode.
2. The MB88313 may enter the test mode when a control command, which is wrongly transferred due to noises, matches the test mode command.
3. When the command transmission from the processor to the MB88313 fails on the way due to noises, the command word must be retransferred after once making $\overline{\text{CS}}$ high and then returning low.

COMMAND DESCRIPTION (Continued)

Table 10. Command Set Summary

Command Number	Command Word Format						Name & Function
	Opecode Field	Operand Field					
	MSB	LSB					
0	0 0 0	CH4	CH3	CH2	CH1	CH0	Character code set: Write operand field data (character code: CH4–CH0) into the character code field of the display memory.
1	0 0 1	0	A3	A2	A1	A0	Address preset: Write operand field data (display memory address: A3–A0) into the address counter to indicate memory locations.
2	0 1 0	HP4	HP3	HP2	HP1	HP0	Horizontal display position control: Write operand field data (position code: HP4–HP0) into the horizontal display position register.
3	0 1 1	VP4	VP3	VP2	VP1	VP0	Vertical display position control: Write operand field data (position code: VP4–VP0) into the vertical display position register.
4	1 0 0	0	VS1	VS0	HS1	HS0	Character size control: Write operand field data (horizontal & vertical character size codes: HS1 & 0, VS1 & 0) into the horizontal and vertical character size registers.
5	1 0 1	SC4	SC3	SC2	SC1	SC0	Screen control: Write operand field data (screen control codes: SC4–SC0) into screen control register.
6	1 1 0	STP	0	AC2	AC1	AC0	Attribute control: Write operand field data (clock stop code: STP, attribute codes: AC2–AC0) into the attribute field of the display memory, and the standby mode (clock stop mode) control bit.
7	1 1 1	GOC	0	GO2	GO1	GO0	General output control: Write operand field data (GOC, GO2–GO0) into the general output register (GO2–GO0) and its control bit (GOC).

ABSOLUTE MAXIMUM RATINGS†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	
Input Voltage	V_{IN}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Voltage	V_{OUT}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	−30		+70	°C	
Storage Temperature	T_{STG}	−55		+150	°C	

†Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	V_{CC}
	V_{SS}		0		V	
Input High Voltage	V_{IH}	$0.8 \times V_{CC}$		$V_{CC}+0.3$	V	$\overline{\text{RESET}}$, $\overline{\text{CS}}$, SCLK, SI $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.2 \times V_{CC}$	V	$\overline{\text{RESET}}$, $\overline{\text{CS}}$, SCLK, SI $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$
Operating Ambient Temperature	T_A	−30		70	°C	

DC CHARACTERISTICS

(Recommended operating conditions, unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	DO2–DO0, VOC, $\overline{\text{VOB}}$	$V_{CC} = 4.5V$ $I_{OH} = -200\ \mu A$	2.4			V
			$V_{CC} = 4.5V$ $I_{OH} = -10\ \mu A$	4.0			V
Output Low Voltage	V_{OL}	DO2–DO0, VOC, $\overline{\text{VOB}}$	$V_{CC} = 4.5V$ $I_{OL} = 1.8$ mA			0.4	V
			$V_{CC} = 4.5V$ $I_{OL} = 3.2$ mA			0.6	V
Input Leakage Current	I_{IL}	$\overline{\text{RESET}}$	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$		−20	−60	μA
		$\overline{\text{CS}}$, SCLK, SI $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$		−20	−60	μA
		EX	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$		−10	−20	μA
Supply Current	I_{CC}	V_{CC}	$V_{CC} = 5.0V$ (Typ.) fc = 6 MHz (Active) Reset state All outputs open		8.0		mA

AC CHARACTERISTICS

(Recommended operating conditions, unless otherwise noted.)

Clock Timing

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Clock Frequency	f_c	EX, X	RC-network OSC, LC-network OSC Figure 19	4.0		7.0	MHz

Input Timing

Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
Shift Clock Pulse Width	t_{WCH}	SCLK	Figure 20	300		ns
	t_{WCL}			300		
Shift Clock Rise/Fall Times	t_{cr}	SCLK	Figure 20		200	ns
	t_{cf}				200	
Shift Clock Cycle Time	t_{CYC}	SCLK	Figure 20	1000		ns
Shift Clock Start Time	t_{SS}	SCLK	Figure 20	200		ns
Shift Clock Hold Time	t_{HS}	SCLK	Figure 20	1000		ns
Input Data Setup Time	t_{SU}	SI	Figure 20	200		ns
Input Data Hold Time	t_H	SI	Figure 20	50		ns
Chip Select End Time	t_{EC}	$\overline{CS}$	Figure 20	1000		ns
Chip Select Rise/Fall Times	t_{crc}	$\overline{CS}$	Figure 20		200	ns
	t_{cfc}					
Horizontal Sync Valid Time	t_{HSDF}[1]	$\overline{HSYNC}$	Figure 21	200		ns
	t_{HSDR}[2]			200		

Notes:

1. The rising edge of $\overline{HSYNC}$ is not counted during t_{HSDF} period to calculate the vertical display position.
2. The rising edge of $\overline{HSYNC}$ is counted during t_{HSDR} period to calculate the vertical display position.

Output Timing

Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
General Output Delay Time	t_{DD}	DO2–DO0	5 kΩ External Pull-Up Figure 22		600	ns

AC CHARACTERISTICS

(Recommended operating conditions, unless otherwise noted.) (Continued)

Figure 19. Clock Circuit Configurations

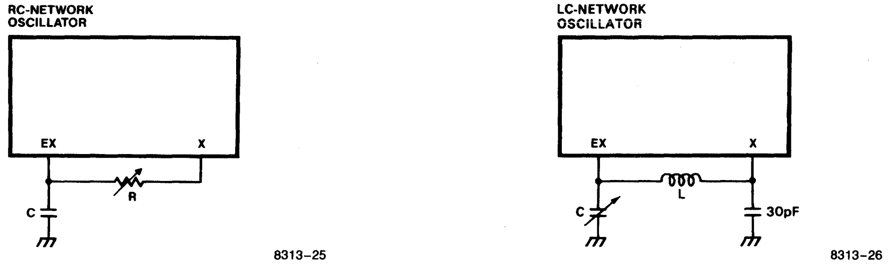


Figure 20. Input Timing (Processor Interface)

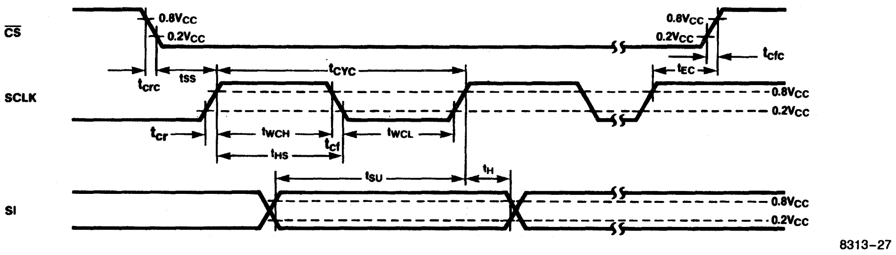


Figure 21. Input Timing (Television Interface)

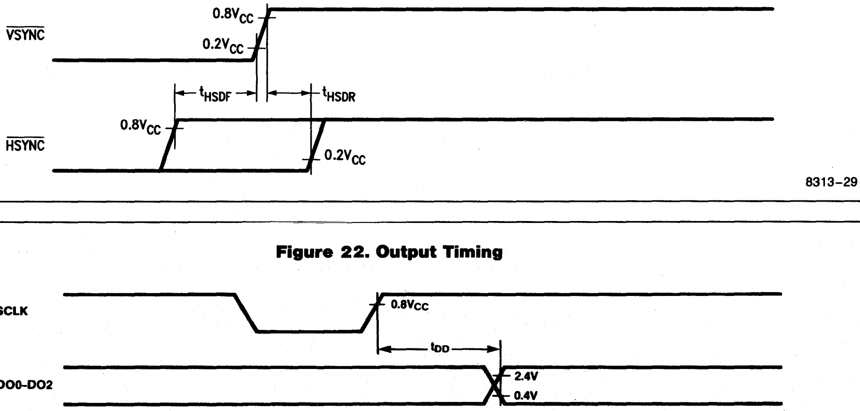
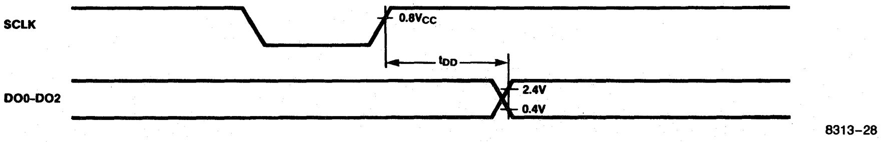
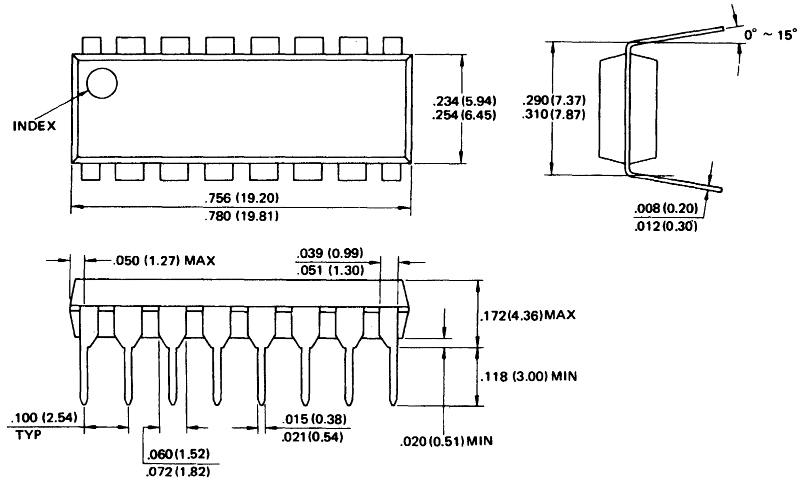


Figure 22. Output Timing



PACKAGE DIMENSIONS

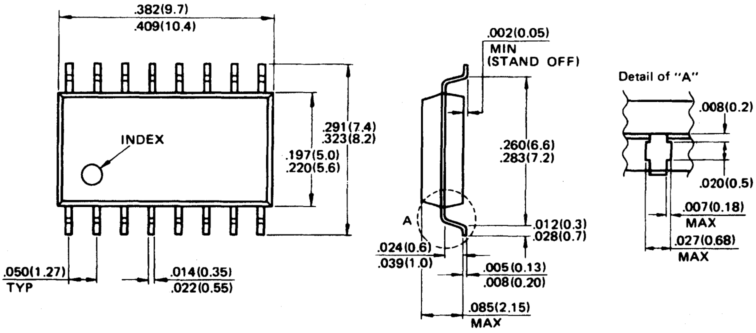
16-LEAD PLASTIC DUAL IN-LINE PACKAGE DIP-16P-M02



8313–30

Dimensions in inches (millimeters)

16-LEAD PLASTIC FLAT PACKAGE FPT-16P-M02



8313–31

Dimensions in inches (millimeters)

FUJITSU

SCSI PROTOCOL CONTROLLER

MB87030

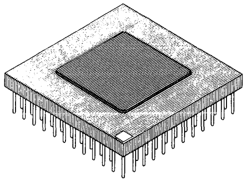
April 1986
Edition 1.0

DESCRIPTION

The MB87030 SCSI Protocol Controller (SPC) is a CMOS LSI circuit specifically designed to control a Small Computer Systems Interface (SCSI). The SPC can serve as either an Initiator or Target for the SCSI; thus, it can be used as an I/O controller or as a host adapter. To use the device in the most effective manner, it is recommended that the user be thoroughly familiar with the SCSI protocol. For detailed information in these areas, the user should request the "Users Guide for MB87030 SCSI" from the nearest Sales Office of Fujitsu.

The SPC is designed to control all SCSI interface signals and virtually all interface control procedures. Used as an 8- or 16-bit peripheral, the device provides high-level control for almost all SCSI configurations.

To achieve optimum performance and interface flexiblity, the SPC contains an 8-byte First In First Out (FIFO) data buffer register and a 24-bit transfer byte counter. Independent data busses for the CPU and the DMA controller plus separate input/output pins for all control signals greatly reduces the possiblity of a "busy" condition. Data transfers can be executed in either the synchronous or asynchronous mode with a maximum offset of 8-bytes.



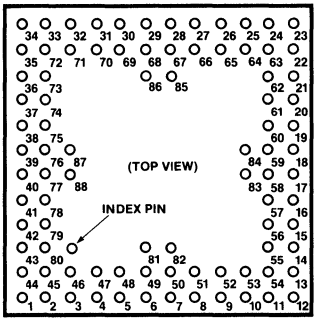
PGA-88C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- Independent data transfer bus for CPU and DMA controller
- Full support for SCSI control
- Serves as either *Initiator* or *Target* device
- Synchronous mode transfer with a programmable offset of up to eight bytes
- In synchronous mode, data transfer speed programmable at four rates
- Data transfer rates of up to 4 megabytes per second
- Eight-byte data buffer register
- 24-bit transfer byte counter
- Compatible with single-ended and/or differential alternative for SCSI
- Single +5V supply
- Low power dissipation
- TTL-compatible I/O
- 88-Pin Ceramic Repeated Quad-In-Line Package

PIN ASSIGNMENTS



Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I	HIM	23	O	SDBOP	45	I	A1	67	O	SDBE5
2	I/O	HDB0	24	O	SDBE7	46	I	A2	68	O	SDBE4
3	I/O	1	25	I	SDBI7	47	I	A3	69	I	SDBI4
4	I/O	2	26	O	SDBE6	48	I/O	D4	70	O	SDBO3
5	I/O	3	27	O	SDBO5	49	I/O	D5	71	I	SDBI2
6	I/O	4	28	I	SDBI5	50	I/O	D6	72	O	SDBO1
7	I/O	5	29	O	SDBO4	51	I/O	D7	73	O	SDBE0
8	I/O	6	30	O	SDBE3	52	I/O	DP	74	I	SDBI0
9	I/O	7	31	I	SDBI3	53	O	INTR	75	I	$\overline{\text{RST}}$
10	I/O	P	32	O	SDBO2	54	I	I/OI	76	O	DREQ
11	O	INIT	33	O	SDBE2	55	I	C/DI	77	I	$\overline{\text{WT}}$
12	O	TARG	34	I	SDBI1	56	I	SELI	78	I	$\overline{\text{WTG}}$
13	O	I/OO	35	O	SDBE1	57	I	MSG1	79	I/O	D2
14	O	C/DO	36	O	SDBOO	58	I	REQI	80	I/O	D3
15	O	SELO	37	I	$\overline{\text{CS}}$	59	I	RSTI	81	Power Supply	VSS
16	O	MSGO	38	I	$\overline{\text{CLK}}$	60	I	ACKI	82	Power Supply	VDD
17	O	REQO	39	I	$\overline{\text{RD}}$	61	I	BSYI	83	Power Supply	VDD
18	O	RSTO	40	I	$\overline{\text{RGD}}$	62	I	ANTI	84	Power Supply	VSS
19	O	ACKO	41	I	DRESP	63	I	SDBIP	85	Power Supply	VSS
20	O	BSYO	42	I/O	D0	64	O	SDBO7	86	Power Supply	VDD
21	O	ATNO	43	I/O	D1	65	O	SDBO6	87	Power Supply	VDD
22	O	SDBEP	44	I	A0	66	I	SDBI6	88	Power Supply	VSS

PIN DESCRIPTIONS

Pin Number	Designator	Function
82, 83, 86, 87	V_{DD}	+5V power supply
81, 84, 85, 88	V_{SS}	Ground (0V)
38	$\overline{\mathrm{CLK}}$	Input clock for controlling SPC internal operation and data transfer speed.
75	$\overline{\mathrm{RST}}$	Asynchronous reset signal for clearing internal circuits of SPC.
37	$\overline{\mathrm{CS}}$	Selection enable signal for accessing an internal register in SPC. When $\overline{\mathrm{CS}}$ is active, the following input/output signals are valid: $\overline{\mathrm{RD}}$, $\overline{\mathrm{RDG}}$, $\overline{\mathrm{WT}}$, $\overline{\mathrm{WTG}}$, DP, A3-A0, and D7-D0.
47 46 45 44	A3 A2 A1 A0	Address input signals for selecting an internal register in SPC. MSB: A3, LSB: A0 When $\overline{\mathrm{CS}}$ is active low, read/write is enabled and an internal register is selected by these address inputs via data bus lines D7-D0 and DP.
39 40	$\overline{\mathrm{RD}}$ $\overline{\mathrm{RDG}}$	Input strobes used for reading out the contents of the SPC internal register and are effective only when $\overline{\mathrm{CS}}$ is active low. When $\overline{\mathrm{RDG}}$ is active, the contents of an internal register selected by address inputs A3-A0 are placed on data bus lines D7-D0 and DP. For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{\mathrm{RD}}$ is used as a timing signal to indicate the end of data read.
77	$\overline{\mathrm{WT}}$	Input strobe used for writing data into an SPC internal register and is only effective when $\overline{\mathrm{CS}}$ is active low. On the trailing edge of $\overline{\mathrm{WT}}$, data placed on data bus lines D7-D0 and DP are loaded into an internal register selected by address inputs A3 to A0, except when all address lines are high (A3-A0 = H). For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{\mathrm{WT}}$ is used as a timing signal to indiacte a data-ready state.

78	$\overline{\mathrm{WTG}}$	When $\overline{\mathrm{WTG}}$ is active low, data appearing on data bus lines D7-D0 and DP is output to HDB7-HDB0 and HDBP if the following input conditions are satisfied:
		$\overline{\mathrm{CS}}$ = 'L'
		A3 = A2 = A1 = A0 = 'H'
		HIN = 'H'

51 50 49 48 80 79 43 42 52	D7 D6 D5 D4 D3 D2 D1 D0 DP	Used for writing-or-reading data into-or-from an internal register in SPC. This data bus is three-state and bidirectional. MSB: D7 LSB: D0 Odd Parity Bit: DP When the $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RDG}}$ inputs are active, the contents of the internal register are output to the data bus (read operation). In operations other than read, this data bus is kept at a high impedance level.

PIN DESCRIPTIONS (Cont'd)

<table>
<tr><th>Pin Number</th><th>Designator</th><th>Function</th></tr>
<tr><td>53</td><td>INTR</td><td>Requests an interrupt to indicate completion of an SPC internal operation or the occurrence of an error.
Interrupt masking is allowed except for an interrupt caused by the RSTI input (reset condition is SCSI).
When an interrupt request is permitted, the INTR signal remains active until the cause of the interrupt is cleared.</td></tr>
<tr><td>25
66
28
69
31
71
34
74
63</td><td>SDBI7
SDBI6
SDBI5
SDBI4
SDBI3
SDBI2
SDBI1
SDBI0
SDBIP</td><td>Used as input for the SCSI data bus.
MSB: SDBI7
LSB: SDBI0
Odd parity bit: SDBIP
Parity checking for the SCSI data bus is programmable.</td></tr>
<tr><td>64
65
27
29
70
32
72
36
23</td><td>SDBO7
SDBO6
SDBO5
SDBO4
SDBO3
SDBO2
SDBO1
SDBO0
SDBOP</td><td>Used as outputs to the SCSI data bus.
MSB: SDBO7
LSB: SDBO0
Odd parity bit: SDBOP
If the bus driver is an open collector device, these signals should be applied directly to the driver circuit.
If the bus driver is a three-state device, these signals are used as data and the SDBE7-SDBE0 and SDBEP signals are used as drive-enable signals.</td></tr>
<tr><td>24
26
67
68
30
33
35
73
22</td><td>SDBE7
SDBE6
SDBE5
SDBE4
SDBE3
SDBE2
SDBE1
SDBE0
SDBEP</td><td>Used as drive enable signals (corresponding to respective bit positions) when a three state-buffer is used for the SCSI data bus.
SDBE7-SDBE0 and SDBEP correspond to SDBO7-SDBO0 and SDBOP, respectively. The relationship with respect to the SCSI bus status is shown below.
<table>
<tr><th colspan="2" rowspan="2">SCSI bus status</th><th colspan="2">SDBOn</th><th colspan="2">SDBEn</th></tr>
<tr><th>(ID)</th><th>($\overline{\text{ID}}$)</th><th>(ID)</th><th>($\overline{\text{ID}}$)</th></tr>
<tr><td colspan="2">Bus Free</td><td>'L'</td><td>'L'</td><td>'L'</td><td>'L'</td></tr>
<tr><td colspan="2">Arbitration</td><td>'H'</td><td>'L'</td><td>'H'</td><td>'L'</td></tr>
<tr><td colspan="2">Selection/Reselection</td><td>D</td><td>D</td><td>'H'</td><td>'H'</td></tr>
<tr><td rowspan="2">Information Transfer</td><td>SPC → SCSI</td><td>D</td><td>D</td><td>'H'</td><td>'H'</td></tr>
<tr><td>SPC ← SCSI</td><td>'L'</td><td>'L'</td><td>'L'</td><td>'L'</td></tr>
</table>
● (ID) indicates a bit positions corresponding to the SCSI bus device ID, and ($\overline{\text{ID}}$) indicates the other bit position.
● D denotes that valid information is sent out.</td></tr>
</table>

PIN DESCRIPTIONS (Cont'd)

<table>
<tr><th>Pin Number</th><th>Designator</th><th>Function</th></tr>
<tr><td>56
61
58
60
57
55
54
62
59</td><td>SELI
BSYI
REQI
ACKI
MSGI
C/DI
I/OI
ATNI
RSTI</td><td>Used for receiving SCSI control signals. The outputs of the SCSI receiver can be directly connected.
Note: Waveform distortion or any other disturbance should not occur in the REQI and ACKI signals which are used as timing control signals for sequencing data transfer.</td></tr>
<tr><td>15
20
17
19
16
14
13
21
18</td><td>SELO
BSYO
REQO
ACKO
MSGO
C/DO
I/OO
ATNO
RSTO</td><td>Used to output SCSI control signals. The following signals become active only when SPC serves as a target; otherwise, these signals are always low: REQO, MSGO, C/DO and I/OO.
The following signals become active only when SPC serves as an initiator; otherwise, these signals are always low: ACKO and ATNO.</td></tr>
<tr><td>11
12</td><td>INIT
TARG</td><td>Used to indicate operating state of SPC. These signals are also available as control signals for the SCSI driver/receiver circuits.
<table>
<tr><th>Initiator</th><th>Target</th><th>Status</th></tr>
<tr><td>'L'</td><td>'L'</td><td>SPC is not connected to SCSI.</td></tr>
<tr><td>'L'</td><td>'H'</td><td>SPC is executing reselection phase or is operating as a target.</td></tr>
<tr><td>'H'</td><td>'L'</td><td>SPC is executing selection phase or is operating as an initiator.</td></tr>
</table></td></tr>
<tr><td>76</td><td>DREQ</td><td>When executing a data transfer cycle in DMA mode, the DREQ signal is used to indicate a request for data transfer between SPC and the external buffer memory.
In DMA mode, data is routed as shown below:
<b>Output operation</b>
External buffer memory
↓
HDB7 to HDB0, and HDBP pins
↓
SPC internal data buffer register (8 bytes)
↓
SDBO7 to SDBO0 and SDBOP pins
↓
(SCSI)</td></tr>
</table>

PIN DESCRIPTIONS (Cont'd)

Pin Number	Designator	Function
76	DREQ (cont'd)	**Input operation** (SCSI) ↓ SDBI7 to SDBI0 and SDBIP pins ↓ SPC internal data buffer register (8 bytes) ↓ HDB7 to HDB0, and HDBP pins ↓ External buffer memory In an output operation, DREQ becomes active to request a data transfer from the external buffer memory when the SPC internal data buffer register has free space available. In an input operation, it becomes active to request a data transfer to the external buffer memory when the SPC internal buffer memory contains valid data.
41	DRESP	Used as a response signal to the above data transfer request signal (DREQ) in DMA mode during a data transfer cycle. Pin DRESP must be refreshed with an applied pulse after each byte transferred. In an output operation, SPC uses the trailing edge of the DRESP signal for sampling data on the HDB7-HDB0 and HDBP bus lines. In an input operation, SPC holds data to be transferred onto HDB7-HDB0 and HDBP bus lines until the trailing edge of the DRESP signal.
9 8 7 6 5 4 3 2 10	HDB7 HDB6 HDB5 HDB4 HDB3 HDB2 HDB1 HDB0 HDBP	Three-state, bidirectional data bus for transferring data to-or-from the external buffer memory in DMA mode. MSB: HDB7 LSB: HDB0 Odd parity bit: HDBP The data transmission direction depends on the HIN input signal. **HIN** **HDBn** **Operation** 'L' Input mode Output 'H' Output mode Input
1	HIN	This signal indicates transmission direction along data bus lines HDB7-HDB0 and HDBP in DMA transfer mode. To be executed, transmission direction must be properly coordinated with internal operation of the SPC. When the HIN signal is Low, data bus lines HDB7-HDB0 and HDBP are put in the high impedance state (input mode). When the HIN signal is High, they are switched to the output mode.

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Values		Unit
		Min	Max	
Supply Voltage	V_{DD}	$V_{SS}{}^2 - 0.5$	7.0	V
Input Voltage	V_I	$V_{SS}{}^2 - 0.5$	$V_{DD} + 0.5$	V
Output Voltage	V_O	$V_{SS}{}^2 - 0.5$	$V_{DD} + 0.5$	V
Storage Temperature (Ceramic)	T_{stg}	-65	+150	°C
Temperature Under Bias (Ceramic)	T_{bias}	-40	+125	°C
Output Current[3]	I_{OS}	-40	+70	mA

Notes:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the SCSI User's Guide. Absolute maximum rating conditions for extended periods may affect device reliability.
2. V_{SS} = 0V.
3. Not more than one output may be shorted at a time for a maximum duration of one second.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.2			V
Input Low Voltage	V_{IL}			0.8	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power Supply Current	I_{DDS}	Steady state[1]			100	μA
Power Dissipation	PD			300		mW
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	4.2		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA	V_{SS}		0.4	V
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{LI}	$V_I = 0 - V_{DD}$	−10		10	μA
Input Leakage Current	I_{LZ}	3-state $V_I = 0 - V_{DD}$	−10		10	μA

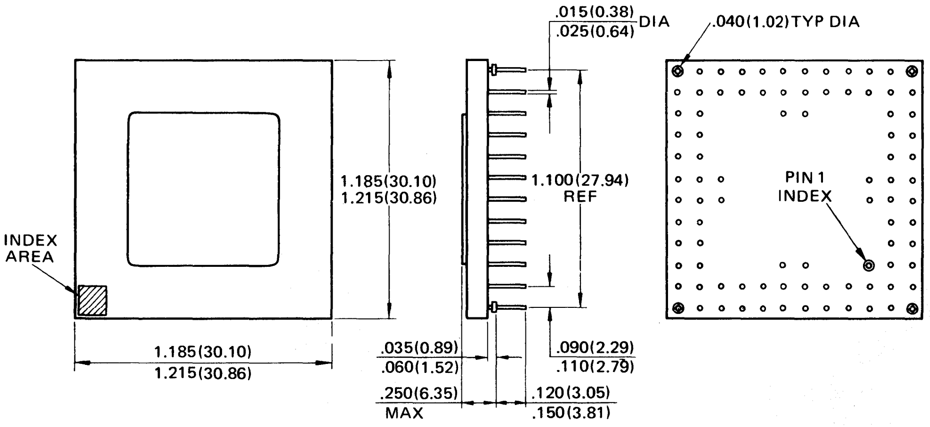
Note:
1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$

CAPACITANCE (T_A = 25°C, $V_{DD} = V_I$ = 0V, f = 1 MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Pin Capacitance	C_{IN}			9	pF
Output Pin Capacitance	C_{OUT}			9	pF
I/O Pin Capacitance	$C_{I/O}$			11	pF

PACKAGE DIMENSIONS

88-Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
PGA-88C-A01



Dimensions in inches (millimeters)

October 1986
Edition 2.0

MBL8041A/H/E/N

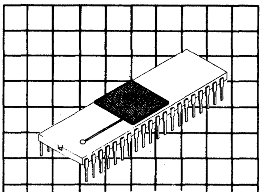
NMOS Universal Peripheral Interface 8-Bit Microcomputer

Description

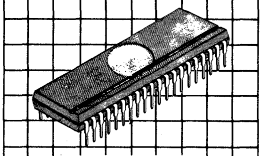
The MBL8041A Universal Peripheral Interface is a single-chip 8-bit microcomputer based on a 8-bit parallel microprocessor chip.

The MBL8041A is fabricated with an N-channel silicongate MOS process. The MBL8041A has a 1Kx8 bit ROM for program memory, a 64x8 bit RAM for data memory, 18 I/O ports, an 8-bit timer/counter and clock generator on the chip, and is powered by single +5V supply.

The MBL8041A is designed to operate as a slave Processor, which receives commands and data from the master processor, controls peripheral devices and transfers input data from peripheral devices to the master processor. And by using the MBL8041A an intelligent peripheral controller can be designed freely.



Ceramic DIP
DIP-40C-A01

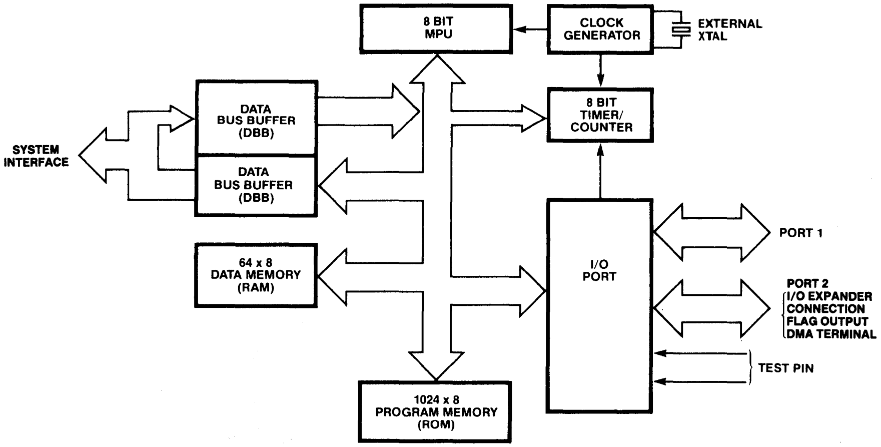


Plastic DIP
DIP-40P-M01

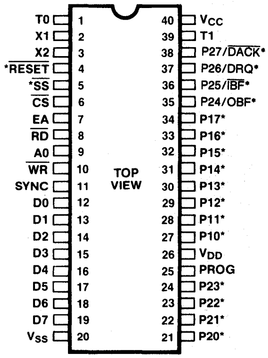
Features

- **Processor:**
  8-bit parallel processing
- **Register:**
  One 8-bit Status Register (for Interface with master processor)
  Two 8-bit Data Bus Buffer Registers (for Input/Output)
- **Memory:**
  1Kx8 bit ROM (for program memory)
  64x8 bit RAM (for data memory)
- **I/O:**
  One 8-bit Bidirectional Data Bus
  Two 8-bit Bidirectional I/O Ports
  Two Test Inputs
- **Clock Source:**
  Clock Generator (with External Crystal Resonator) or External Clock
- **8-Bit Interval Timer/Event Counter**
- **Low-power Standby Operation Capability**
- **Power-on Reset Capability (with External Capacitor)**
- **Instruction Set:**
  93 Instructions (217 Instruction Codes)
  — 1-byte Instruction (about 70%),
  2-byte Instruction (about 30%)
  — 1-cycle or 2-cycle instruction (1 cycle = 2.5 μs at 6MHz XTAL)
- **Technology:**
  N-channel Silicon-gate E/D MOS Process
- **Two Package Options:**
  Standard 40-pin Ceramic (Suffix-C) or Plastic DIP (Suffix-P)
- **Equivalent:**
  Intel 8041A

Block Diagram



Pin Assignment



*These pins are internally pulled up

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Pin Descriptions

Pin No.	Name	Symbol	Description
1	Test 0	T_0	Conditional Input for Conditional Branch
2	Crystal 1	XTAL 1	Input pin for the internal Clock Generator to be connected to one terminal of the external crystal. Also, this pin can be used as the input from an external clock source.
3	Crystal 2	XTAL 2	Input pin for the internal Clock Generator to be connected to the other terminal of the external crystal. (Note: The XTAL 1 and XTAL 2 input levels are not TTL compatible).
4	Reset	$\overline{\text{RESET}}$	Input which resets and forces the MPU to be initialized. (Note: This input level is not TTL compatible).
5	Single Step	$\overline{\text{SS}}$	Input pin used for single step operation.
6	Chip Select	$\overline{\text{CS}}$	Input pin used for the master processor to select the UPI.
7	External Address	EA	Input pin used for controlling program memory access. Holding EA high forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.
8	Read Strobe	$\overline{\text{RD}}$	A Strobe input used to enable the MBL8041A to be read contents of the Data Bus Buffer register or Status register.
9	Address "0"	A_0	An Address input to determine whether read/write data or read/write commands. A_0 = "L" indicates data read or write. A_0 = "H" indicates status read or command write.
10	Write Strobe	$\overline{\text{WR}}$	A strobe input used to enable the MBL8041A to be written into its Data Bus Buffer register.
11	Sync	SYNC	A clock output pin indicating the MBL8041A instruction cycle. This pin is used when a synchronization signal is required for external circuits.
12 thru 19	Data Bus	DB_0 thru DB_7	8-bit bidirectional I/O port used to interface the MBL8041A to the master processor.
20	Ground	V_{SS}	Ground terminal.
21 thru 24	Port 2	$P2_0$ thru $P2_3$	Lower 4 bits of the quasi-bidirectional I/O port (Port 2). These function as interface port with the I/O expander (MBL8243) when an expansion I/O executes instruction. During single step operation upper 2 bits of the program fetch address are output on $P2_0$ and $P2_1$.
25	Program	PROG	A strobe signal output pin for an I/O expander (MBL8243) used, when performing an expansion I/O instruction.
26	Power Supply	V_{DD}	Power supply Pin (+5V) for internal RAM.
27 thru 34	Port 1	$P1_0$ thru $P1_7$	Quasi-bidirectional I/O ports (Port 1). During single step operation, the next program fetch address (Lower 8 bits) is output.
35 thru 38	Port 2	$P2_4$ thru $P2_7$	Upper 4 bits of the quasi-bidirectional I/O port (Port 2). These function as the flag output pins ($P2_4$ and $P2_5$) and DMA pins ($P2_6$ and $P2_7$) according to instructions.
39	Test 1	T_1	This pin as the following functions according to instruction: 1. Event Input pin for the Event Counter. 2. Condition Input pin for Conditional Branch.
40	Power Supply	V_{CC}	Power supply pin (+5V).

System Interface

The master processor and MBL8041A are interfaced through the data bus buffer.

MBL8041A has 2 internal DBB (Data Bus Buffer) registers. It is determined by the address line and strobe signal which register is accessed.

Flag 1 (F1) is set when a command is written (A_0 = 1), and reset when data is written (A_0 = 0).

The master processor can read only data from the output DBB register, and cannot read and check data or commands which the master processor has written itself.

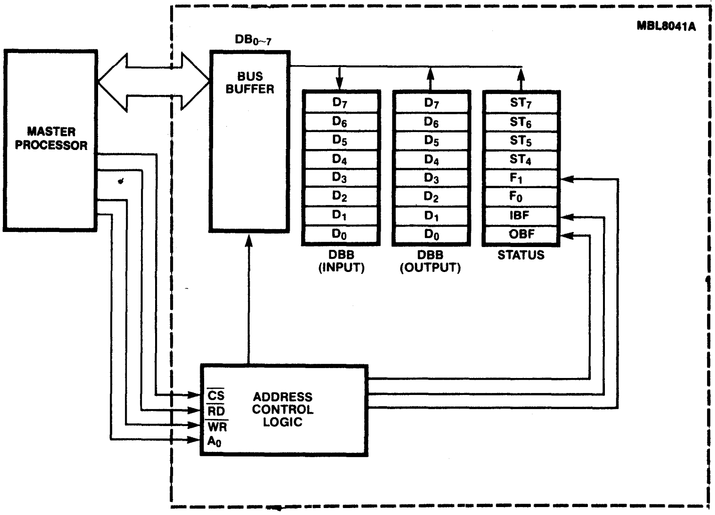
When MBL8041A writes data to the output DBB with the OUT DBB, A instruction, OBF is set.

When DBB is read (CS = RE = A_0 = 0, WR = 1) by the master processor, OBF is reset. IBF is set when the master processor writes in the DBB, and reset when MBL8041A reads the data from the DBB with IN A, DBB instruction.

The internal status of the MBL8041A does not change even when the status register contents is read out.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	Description
0	0	1	0	Read DBB (Output) register.
0	0	1	1	Read Status Register.
0	1	0	0	Write DBB (Input) register (Data).
0	1	0	1	Write DBB (Input) register (Command).
1	x	x	x	Invalid.

Interface between MBL8041A and Master Processor



Resident Data Memory Map (RAM)

Address (Hex)		
0	R_0 Register 0	Register Bank 0
1	R_1 Register 1	
2	R_2 Register 2	
3	R_3 Register 3	
4	R_4 Register 4	
5	R_5 Register 5	
6	R_6 Register 6	
7	R_7 Register 7	
8		Stack Register (16 Bytes) (8 Level Stack)
9		
	PC_L	
	C AC FO BS PC_H	
16		
17		
18	R_0 Register 0	Register Bank 1
19	R_1 Register 1	
1A	R_2 Register 2	
1B	R_3 Register 3	
1C	R_4 Register 4	
1D	R_5 Register 5	
1E	R_6 Register 6	
1F	R_7 Register 7	
20	Working Area (32 Bytes)	
21		
22		
≀		
3D		
3E		
3F		

Status Register (PSW)

The Status Register is an 8-bit register configured as shown in the following figure. The upper four bits are used for flags to indicate the status of the MPU and when a sub-routine call or an interrupt occurs, the contents of the program counter is transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register.

The remaining one bit is an unused bit.

7	6	5	4	3	2	1	0
C	AC	F_0	BS	1	SP_2	SP_1	SP_0
← Flags →				(Unused Bit)	← Stack Pointer →		

Flags

C (Carry): When an overflow occurs in the Accumulator, this bit is set to "1".

AC (Auxiliary Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator, this bit is set to "1".

F_0(User Flag): This flag can be controlled as a user flag by the proper instruction.

BS (Bank select): This flag can be controlled to select a Register Bank by an instruction. When BS = 0, the Register Bank 0 is selected. When BS = 1, the Register Bank 1 is selected.

Stack Register (8 Level Capability)

The Stack Register has 16 bytes of memory area in the built-in RAM. The stack Register consists of eight levels, i.e. a Stack level consists of two bytes as shown below.

SP (Stack Pointer): In the diagram below, "SP" indicates a Stack Pointer address to be used for the next sub-routine call or interrupt. "SP" is given as an 8-bit code from the lower three bits of Status Register as follows:

$SP = 00001SP_2SP_1SP_0$

→Status Register Bits 0 to 2.

PC_n (Program Counter): "PC_n" indicates the content of the n-th bit in the Program Counter.

Interrupt Processing (IBF Interrupt, Timer/Counter Interrupt)

There are two types of interrupt: the IBF interrupt and Timer/Counter interrupt.

If an interrupt occurs when the system is in "interrupt enable" status, the interrupt flag is set as soon as the current instruction is completed.

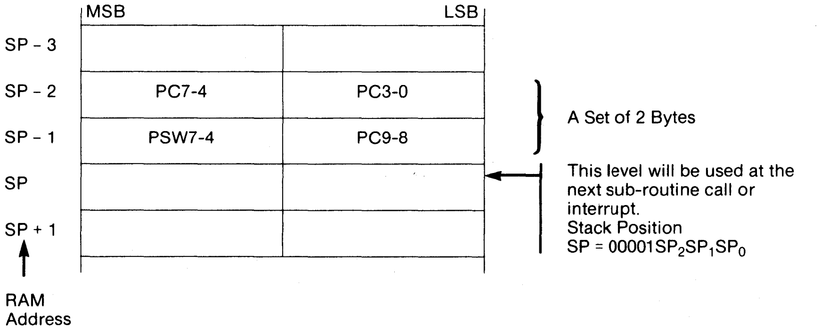
When the interrupt processing begins, the Status and Program Counter contents are first stored in the stack. Then, operation jumps to Address 3 in the case of the IBF interrupt and Address 7 in the case of a timer interrupt.

After the interrupt has been processed by a user program and RETR (Return and Restore Status) instruction has been executed, the Status and Program Counter contents stored in the stack are restored, the interrupt flag is reset and the system is ready to accept the next interrupt request.

A Timer/Counter interrupt request occurs when the Timer/Counter overflow flag is set due to Timer/Counter overflow.

However, since the Timer/Counter interrupt request is masked by the IBF interrupt request, IBF interrupt has first priority.

The Timer/Counter interrupt is enabled after the IBF interrupt has been executed and the system has become ready to receive the next interrupt request.



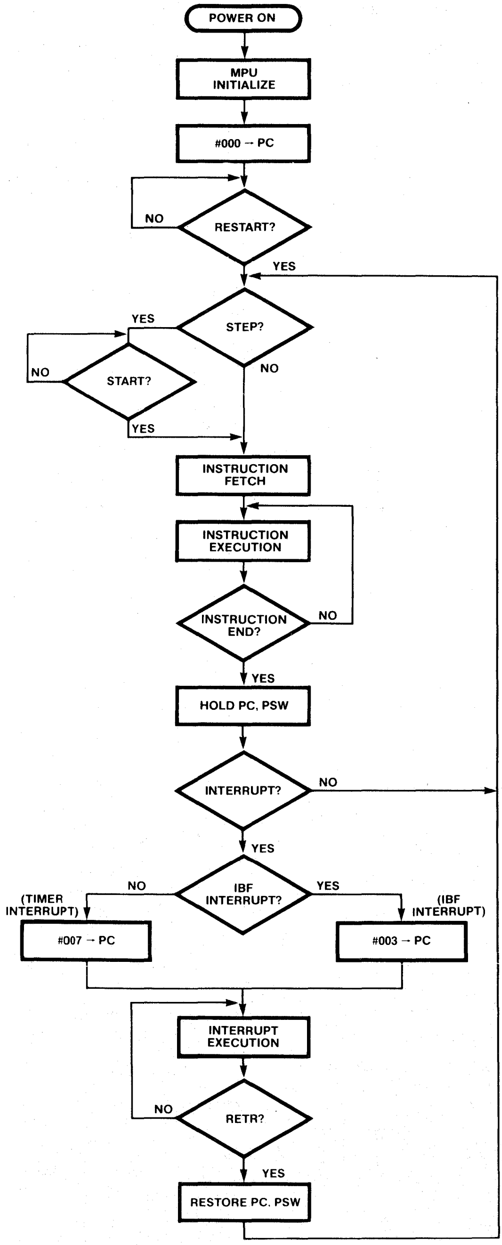
	MSB	LSB
SP - 3		
SP - 2	PC7-4	PC3-0
SP - 1	PSW7-4	PC9-8
SP		
SP + 1		

RAM Address

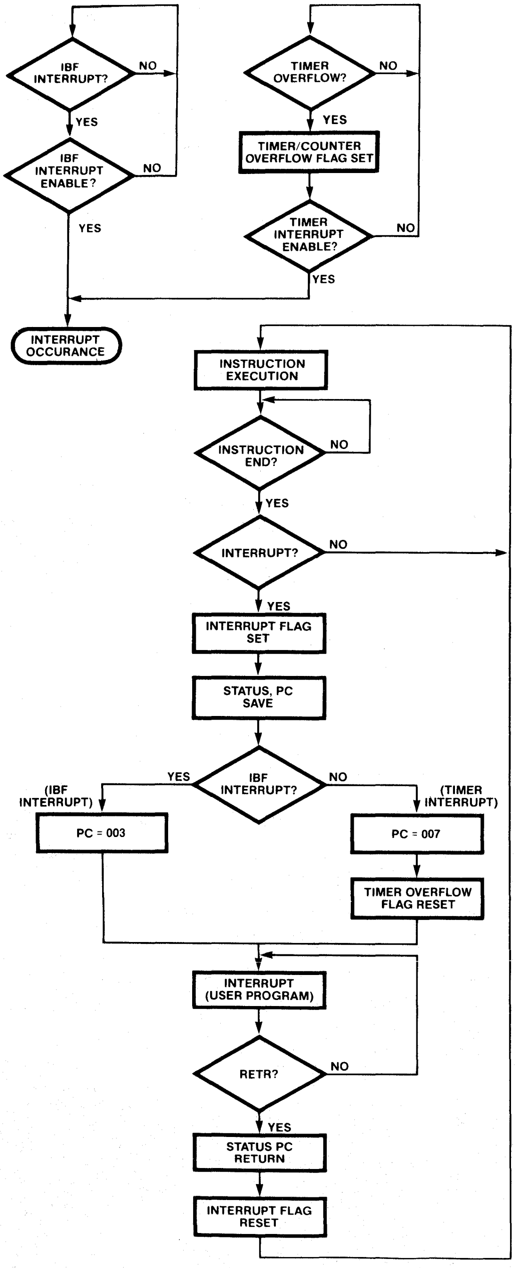
A Set of 2 Bytes

This level will be used at the next sub-routine call or interrupt.
Stack Position
$SP = 00001SP_2SP_1SP_0$

Operation Flow Chart

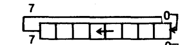
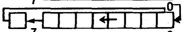
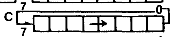
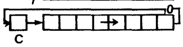


Interrupt Flow Chart



Instruction Set Summary

Accumulator

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Add register to A	ADD A,Rr	6X	1	1	*	*	(A) ← (A) + (Rr)
Add data memory to A	ADD A,@R0	60	1	1	*	*	(A) ← (A) + ((R0))
	ADD A,@R1	61	1	1	*	*	(A) ← (A) + ((R1))
Add immediate to A	ADD A,#data	03	2	2	*	*	(A) ← (A) + data
Add register to A with Carry	ADDC A,Rr	7X	1	1	*	*	(A) ← (A) + (Rr) + (C)
Add data memory to A with Carry	ADDC A,@R0	70	1	1	*	*	(A) ← (A) + ((R0)) + (C)
	ADDC A,@R1	71	1	1	*	*	(A) ← (A) + ((R1)) + (C)
Add immediate to A with Carry	ADDC A,#data	13	2	2	*	*	(A) ← (A) + data + (C)
AND register to A	ANL A,Rr	5X	1	1	—	—	(A) ← (A) AND (Rr)
AND data memory to A	ANL A,@R0	50	1	1	—	—	(A) ← (A) AND ((R0))
	ANL A,@R1	51	1	1	—	—	(A) ← (A) AND ((R1))
AND immediate to A	ANL A,#data	53	2	2	—	—	(A) ← (A) AND data
OR register to A	ORL A,Rr	4X	1	1	—	—	(A) ← (A) OR (Rr)
OR data memory to A	ORL A,@R0	40	1	1	—	—	(A) ← (A) OR ((R0))
	ORL A,@R1	41	1	1	—	—	(A) ← (A) OR ((R1))
OR immediate to A	ORL A,#data	43	2	2	—	—	(A) ← (A) OR data
Exclusive OR register to A	XRL A,Rr	DX	1	1	—	—	(A) ← (A) XOR (Rr)
Exclusive OR data memory to A	XRL A,@R0	D0	1	1	—	—	(A) ← (A) XOR ((R0))
	XRL A,@R1	D1	1	1	—	—	(A) ← (A) XOR ((R1))
Exclusive OR immediate to A	XRL A,#data	D3	2	2	—	—	(A) → (A) XOR data
Increment A	INC A	17	1	1	—	—	(A) ← (A) + 1
Decrement A	DEC A	07	1	1	—	—	(A) ← (A) − 1
Clear A	CLR A	27	1	1	—	—	(A) ← 0
Complement A	CPL A	37	1	1	—	—	(A) ← ($\overline{A}$)
Decimal Adjust A	DA A	57	1	1	*	—	Note (1)
Swap nibbles of A	SWAP A	47	1	1	—	—	(A7 ~ 4) ⇄ (A3 ~ 0)
Rotate A Left	RL A	E7	1	1	—	—	
Rotate A Left through Carry	RLC A	F7	1	1	*	—	
Rotate A Right	RR A	77	1	1	—	—	
Rotate A Right through Carry	RRC A	67	1	1	*	—	

Note 1: The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.
Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction.

Input/Output

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Input port to A	IN A,P1	09	1	2	—	—	(A) ← (P1)
	IN A,P2	0A	1	2	—	—	(A) ← (P2)
Output A to port	OUTL P1,A	39	1	2	—	—	(P1) ← (A)
	OUTL P2,A	3A	1	2	—	—	(P2) ← (A)
AND immediate to port	ANL P1,#data	99	2	2	—	—	(P1) ← (P1) AND data
	ANL P2,#data	9A	2	2	—	—	(P2) ← (P2) AND data
OR immediate to port	ORL P1,#data	89	2	2	—	—	(P1) ← (P1) OR data
	ORL P2,#data	8A	2	2	—	—	(P2) ← (P2) OR data
Input DBB to A clear IBF	IN A,DBB	22	1	1	—	—	(A) ← (DBB), (IBF) ← 0
Output A to DBB, set OBF	OUT DBB,A	02	1	1	—	—	(DBB) ← (A), (OBF) ← 1
A7~4 to bits 7~4 of Status	MOV STS,A	90	1	1	—	—	(STS7 ~ 4) ← (A7 ~ 4)
Input Expander port to A	MOVD A,P_P	0X	1	2	—	—	(A3 ~ 0) ← (P_P), (A7 ~ 4) ← 0
Output A to Expander port	MOVD P_P,A	3X	1	2	—	—	(P_P) ← (A3 ~ 0)
AND A to Expander port	ANLD P_P,A	9X	1	2	—	—	(P_P) ← (P_P) AND (A3 ~ 0)
OR A to Expander port	ORLD P_P,A	8X	1	2	—	—	(P_P) ← (P_P) OR (A3 ~ 0)

Operation Code X: Table 2

Instruction Set Summary
(Continued)

Data Moves

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Move register to A	MOV A,Rr	FX	1	1	—	—	(A) ← (Rr)
Move data memory to A	MOV A,@R0	F0	1	1	—	—	(A) ← ((R0))
	MOV A,@R1	F1	1	1	—	—	(A) ← ((R1))
Move immediate to A	MOV A,#data	23	2	2	—	—	(A) ← data
Move A to register	MOV Rr,A	AX	1	1	—	—	(Rr) ← (A)
Move A to data memory	MOV @R0,A	A0	1	1	—	—	((R0)) ← (A)
	MOV @R1,A	A1	1	1	—	—	((R1)) ← (A)
Move immediate to register	MOV Rr,#data	BX	2	2	—	—	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	—	—	((R0)) ← data
	MOV @R1, #data	B1	2	2	—	—	((R1)) ← data
Move PSW to A	MOV A,PSW	C7	1	1	—	—	(A) ← (PSW)
Move A to PSW	MOV PSW,A	D7	1	1	*	*	(PSW) ← (A)
Exchange A and register	XCH A,Rr	2X	1	1	—	—	(A) ⇄ (Rr)
Exchange A and data memor	XCH A,@R0	20	1	1	—	—	(A) ⇄ ((R0))
	XCH A,@R1	21	1	1	—	—	(A) ⇄ ((R1))
Exchange digit of A and data memory	XCHD A,@R0	30	1	1	—	—	(A3~0) ⇄ ((R0)3~0)
	XCHD A,@R1	31	1	1	—	—	(A3~0) ⇄ ((R1)3~0)
Move to A from current page	MOVP A,@A	A3	1	2	—	—	(A) ← ((A)) within page
Move to A from Page 3	MOVP3 A,@A	E3	1	2	—	—	(A) ← ((A)) within page 3

Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction.

Timer/Counter

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Read Timer/Counter	MOV A,T	42	1	1	—	—	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	—	—	(T) ← (A)
Start Timer	STRT T	55	1	1	—	—	
Start Counter	STRT CNT	45	1	1	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	
Enable Timer/ Counter Interrupt	EN TCNTI	25	1	1	—	—	
Disable Timer/ Counter Interrupt	DIS TCNTI	35	1	1	—	—	

Control

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Enable DMA Handshake Lines	EN DMA	E5	1	1	—	—	
Enable IBF Interrupt	EN I	05	1	1	—	—	
Disable IBF Interrupt	DIS I	15	1	1	—	—	
Enable Master Interrupts	EN FLAGS	F5	1	1	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	—	—	(BS) ← 1
No Operation	NOP	00	1	1	—	—	

Instruction Set Summary
(Continued)

Register

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Increment register	INC Rr	1X	1	1	—	—	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	—	—	((R0)) ← (R0)) +1
	INC @R1	11	1	1	—	—	((R1)) ← ((R1)) + 1
Decrement register	DEC Rr	CX	1	1	—	—	(Rr) ← (Rr) 1

Operation Code X: Table 1

Subroutine

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Jump to Subroutine	CALL addr	%4	2	2	—	—	Note (2)
Return	RET	83	1	2	—	—	Note (3)
Return and restore status	RETR	93	1	2	*	*	Note (4)

Operation Code %: Table 3
Flag*: This flag is set or reset in the state after executed instruction.

Flags

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Clear Carry	CLR C	97	1	1	Z	—	(C) ← 0
Complement Carry	CPL C	A7	1	1	CP	—	(C) ← ($\overline{\text{C}}$)
Clear Flag 0	CLR F0	85	1	1	—	—	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	—	—	(F0) ← ($\overline{\text{F0}}$)
Clear Flag 1	CLR F1	A5	1	1	—	—	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	—	—	(F1) ← ($\overline{\text{F1}}$)

Flag Z: Reset   CP: Invert

Branch

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Jump unconditional	JMP addr	%4	2	2	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	Unconditional Branch Note (5)
Decrement register and jump	DJNZ Rr, addr	EX	2	2	—	—	(Rr) ≠ 0 Note (6)
Jump on Carry = 1	JC addr	F6	2	2	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	(C) = 0
Jump on A Zero	JZ addr	C6	2	2	—	—	(A) = 0
Jump on A not Zero	JNZ addr	96	2	2	—	—	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	—	—	(T0) = 1
Jump on T0 = 0	JNT0 addr	26	2	2	—	—	(T0) = 0
Jump on T1 = 1	JT1 addr	56	2	2	—	—	(T1) = 1
Jump on T1 = 0	JNT1 addr	46	2	2	—	—	(T1) = 0
Jump on F0 = 1	JF0 addr	B6	2	2	—	—	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	—	—	(F1) = 1
Jump on Timer Flag = 1, Clear Flag	JTF addr	16	2	2	—	—	(TF) = 1
Jump on IBF Flag = 0	JNIBF addr	D6	2	2	—	—	(IBF) = 0
Jump on OBF Flag = 1	JOBF addr	86	2	2	—	—	(OBF) = 1
Jump on Accumulator Bit	JBb addr	%2	2	2	—	—	(Ab) = 1

Operation Code %: Table 3
X: Table 1

Note 2: Call addr
((SP)) ← (PC), (PSW7~4)
(SP) ← (SP) + 1
(PC9~8) ← A_H
(PC7~0) ← A_L

Note 3: RET
(SP) ← (SP) — 1
(PC) ← ((SP))

Note 4: RETR
(SP) ← (SP) — 1
(PC) ← ((SP))
(PSW7~4) ← ((SP))

Note 5: JMMP @
(PC7~0) ← ((A))

Note 6: DJNZ Rr, addr
(Rr) ← (Rr) — 1
if (Rr) ≠ 0 (PC7~0) ← addr
if (Rr) = 0 Execute next instruction

Instruction Set Summary
(Continued)

O.P. Code Of Register Access (Table 1)

Mnemonic	Rr	R0	R1	R2	R3	R4	R5	R6	R7
ADD A,Rr		63	69	6A	6B	6C	6D	6E	6F
ADDC A,Rr		78	79	7A	7B	7C	7D	7E	7F
ANL A,Rr		58	59	5A	5B	5C	5D	5E	5F
DEC Rr		C8	C9	CA	CB	CC	CD	CE	CF
DJNZ Rr, addr		E8	E9	EA	EB	EC	ED	EE	EF
INC Rr		18	19	1A	1B	1C	1D	1E	1F
MOV A,Rr		F8	F9	FA	FB	FC	FD	FE	FF
MOV Rr,A		A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr,#data		B8	B9	BA	BB	BC	BD	BE	BF
ORL A, Rr		48	49	4A	4B	4C	4D	4E	4F
XCH A,Rr		28	29	2A	2B	2C	2D	2E	2F
XRL A,Rr		D8	D9	DA	DB	DC	DD	DE	DF

bit

7	6	5	4	3	2	1	0
					r_2	r_1	r_0

O.P.Code Of Expander Port Access (Table 2)

Mnemonic	PP	P4	P5	P6	P7
ANLD P_P.A		9C	9D	9E	9F
MOVD A. P_P		0C	0D	0E	0F
MOVD P_P, A		3C	3D	3E	3F
ORLD P_P, A		8C	8D	8E	8F

bit

7	6	5	4	3	2	1	0
						P_1	P_0

O.P Code of JMP, CALL, JBb (Table 3)

	First Byte								Second Byte							
	bit 7	6	5	4	3	2	1	0	bit 7	6	5	4	3	2	1	0
JMP	0	A_H		0	0	1	0	0	A_L							
CALL	0	A_H		1	0	1	0	0	A_L							
JB_b	B_b			1	0	0	1	0	A_L							

A_H; Address A_9, A_8
A_L; Address A_7 to A_0
B_b; b-th Bit on Accumulator

Instruction Codes

L H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUT DBB,A	◥ ADD A,#	◥ JMP 0 x x	EN 1		DEC A		◤ IN A,P1	◤ IN A,P2		◤ MOVD A,P4	◤ MOVD A,P5	◤ MOVD A,P6	◤ MOVD A,P7
1	INC @R0	INC @R1	◥ JB0 addr	◥ ADDC A,#	◥ CALL 0 x x	DIS 1	◥ JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A,@R0	XCH A,@R1	IN A,DBB	◥ MOV A,#	◥ JMP 1 x x	EN TCNT1	◥ JNT0 addr	CLR A	XCH A,R0	XCH A,R1	XCH A,R2	XCH A,R3	XCH A,R4	XCH A,R5	XCH A,R6	XCH A,R7
3	XCHD A,@R0	XCHD A,@R1	◥ JB1 addr		◥ CALL 1 x x	DIS TCNT1	◥ JT0 addr	CPL A		◤ OUTL P1,A	◤ OUTL P2,A		◤ MOVD P4,A	◤ MOVD P5,A	◤ MOVD P6,A	◤ MOVD P7,A
4	ORL A,@R0	ORL A,@R1	MOV A,T	◥ ORL A,#	◥ JMP 2 x x	STRT CNT	◥ JNT1 addr	SWAP A	ORL A,R0	ORL A,R1	ORL A,R2	ORL A,R3	ORL A,R4	ORL A,R5	ORL A,R6	ORL A,R7
5	ANL A,@R0	ANL A,@R1	◥ JB2 addr	◥ ANL A,#	◥ CALL 2 x x	STRT T	◥ JT1 addr	DA A	ANL A,R0	ANL A,R1	ANL A,R2	ANL A,R3	ANL A,R4	ANL A,R5	ANL A,R6	ANL A,R7
6	ADD A,@R0	ADD A,@R1	MOV T.A		◥ JMP 3 x x	STOP TCNT		RRC A	ADD A,R0	ADD A,R1	ADD A,R2	ADD A,R3	ADD A,R4	ADD A,R5	ADD A,R6	ADD A,R7
7	ADDC A,@R0	ADDC A,@R1	◥ JB3 addr		◥ CALL 3 x x		◥ JF1 addr	RR A	ADDC A,R0	ADDC A,R1	ADDC A,R2	ADDC A,R3	ADDC A,R4	ADDC A,R5	ADDC A,R6	ADDC A,R7
8				◤ RET		CLR F0	◥ JOBF addr			◥ ORL P1,#	◥ ORL P2,#		◤ ORLD P4,A	◤ ORLD P5,A	◤ ORLD P6,A	◤ ORLD P7,A
9	MOV STS, A		◥ JB4 addr	◤ RETR		CPL F0	◥ JNZ addr	CLR C		◥ ANL P1,#	◥ ANL P2,#		◤ ANLD P4,A	◤ ANLD P5,A	◤ ANLD P6,A	◤ ANLD P7,A
A	MOV @R0,A	MOV @R1,A		◤ MOVP A,@A		CLR F1		CPL C	MOV R0,A	MOV R1,A	MOV R2,A	MOV R3,A	MOV R4,A	MOV R5,A	MOV R6,A	MOV R7,A
B	◥ MOV @R0,#	◥ MOV @R1,#	◥ JB5 addr	◤ JMPP @A		CPL F1	◥ JF0 addr		◥ MOV R0,#	◥ MOV R1,#	◥ MOV R2,#	◥ MOV R3,#	◥ MOV R4,#	◥ MOV R5,#	◥ MOV R6,#	◥ MOV R7,#
C						SEL RB0	◥ JZ addr	MOV A,PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A,@R0	XRL A,@R1	◥ JB6 addr	◥ XRL A,#		SEL RB1	◥ JNIBF addr	MOV PSW,A	XRL A,R0	XRL A,R1	XRL A,R2	XRL A,R3	XRL A,R3	XRL A,R5	XRL A,R6	XRL A,R7
E				◤ MOVP3 A,@A		EN DMA	◥ JNC addr	RL A	◥ DJNZ R0,addr	◥ DJNZ R1,addr	◥ DJNZ R2,addr	◥ DJNZ R3,addr	◥ DJNZ R4,addr	◥ DJNZ R5,addr	◥ DJNZ R6,addr	◥ DJNZ R7,addr
F	MOV A,@R0	MOV A,@R1	◥ JB7 addr			EN FLAGS	◥ JC addr	RLC A	MOV A,R0	MOV A,R1	MOV A,R2	MOV A,R3	MOV A,R4	MOV A,R5	MOV A,R6	MOV A,R7

#: Immediate data

□	1 Byte, 1 Cycle Instruction
◤	1 Byte, 2 Cycle Instruction
◥	2 Byte, 2 Cycle Instruction

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	+5.0 ±10%	V
	V_{SS}	0	V
Operating Temperature		0 to +70	°C

DC Characteristics

(T_A = 0° C to +70° C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Value		Unit
				Min.	Max.	
Input Low Voltage	All Except XTAL1, 2, $\overline{RESET}$	V_{IL}		-0.3	0.8	V
	XTAL1,2, $\overline{RESET}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All Except XTAL1, 2, $\overline{RESET}$	V_{IH}		2.0	V_{CC}	V
	XTAL1,2, $\overline{RESET}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	DB_0 to DB_7	V_{OL}	I_{OL} = 2.0mA		0.45	V
	P10-P17, P20-P27 SYNC	V_{OL1}	I_{OL} = 1.6mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
Output High Voltage	DB_0 to DB_7	V_{OH}	I_{OH} = -400μA	2.4		
	All other outputs	V_{OH1}	I_{OH} = -50μA	2.4		
Input Leakage Current	T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0, EA	I_{IL}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		±10	μA
Output Leakage Current	DB_0 to DB_7 (High Z State)	I_{OL}	$V_{SS}+0.45V \leqq V_{IN} \leqq V_{CC}$		±10	μA
Input Low Current	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$	I_{LI}	V_{IL} = 0.8V		0.5	mA
	$\overline{RESET}$, $\overline{SS}$	I_{LI1}	V_{IL} = 0.8V		0.2	mA
V_{DD} Supply Current		I_{DD}			15	mA
Supply Current		I_{CC} + I_{DD}			125	mA

AC Characteristics

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V)

Data Bus Buffer Register Read (Refer to the Fig. 1)

			Test	Value		
Parameter		**Symbol**	**Conditions**	**Min.**	**Max.**	**Unit**
$\overline{\text{CS}}$, A_0 Setup Time (to $\overline{\text{RD}}$)		t_{AR}		0		ns
$\overline{\text{CS}}$, A_0 Hold Time (from $\overline{\text{RD}}$)		t_{RA}		0		ns
$\overline{\text{RD}}$ Pulse Width		t_{RR}		250		ns
Data Delay Time (from $\overline{\text{CS}}$, A_0)		t_{AD}	C_L = 150pF		225	ns
Data Delay Time (from $\overline{\text{RD}}$)		t_{RD}	C_L = 150pF		225	ns
Data Floating Time (from $\overline{\text{RD}}$)		t_{DF}			100	ns
Recovery Time		t_{RV}		300		ns
Cycle Time	MBL8041AN	t_{CY}	*	2.5	15.0	μs
	MBL8041AE		**	1.875	15.0	μs
	MBL8041AH		***	1.36	15.0	μs

*t_{CY} = 2.50μs at 6MHz XTAL (N version)
**t_{CY} = 1.875μs at 8MHz XTAL (E version)
***t_{CY} = 1.36μs at 11MHz XTAL (H version)

Data Bus Buffer Register Write (Refer to the Fig. 2)

		Test	Value		
Parameter	**Symbol**	**Conditions**	**Min.**	**Max.**	**Unit**
$\overline{\text{CS}}$, A_0 Setup Time (to $\overline{\text{WR}}$)	t_{AW}		0		ns
$\overline{\text{CS}}$, A_0 Hold Time (to $\overline{\text{WR}}$)	t_{WA}		0		ns
$\overline{\text{WR}}$ Pulse Width	t_{WW}		250		ns
Data Setup Time (to $\overline{\text{WR}}$)	t_{DW}		150		ns
Data Hold Time (to $\overline{\text{WR}}$)	t_{WD}		0		ns

Port 2 (Refer to the Fig. 3)*

		MBL8041AN		MBL8041AE		MBL8041AH		
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Port Control Setup before Falling Edge of PROG Time (to PROG)	t_{CP}	100		105		110		ns
Port Control Hold after Falling Edge of PROG Time (from PROG)	t_{PC}	60		80		100		ns
Output Data Setup Time (to PROG)	t_{DP}	200		210		250		ns
Output Data Hold Time (from PROG)	t_{PD}	20		45		65		ns
Input Data Hold Time (from PROG)	t_{PF}	0	150	0	150	0	150	ns
PROG Time P2 Input Must be Valid	t_{PR}		650		700		810	ns
PROG Pulse Width	t_{PP}	700		1150		1200		ns

*at 6MHz XTAL for N version
at 8 MHz XTAL for E version
at 11 MHz XTAL for H version.

AC Characteristics
(Continued)

DMA Characteristics (Refer to the Fig. 4)

Parameter	Symbol	Test Conditions	Value Min.	Value Max.	Unit
DACK Setup Time (to RD, WR)	t_{ACC}		0		ns
DACK Hold Time (from RD,WR)	t_{CAC}		0		ns
Input Data Delay Time (from DACK)	t_{ACD}	C_L = 150pF		225	ns
DRQ Clear Time (from RD, WR)	t_{CRQ}			200	ns

AC Test Conditions
V_{IL} = 0.8V (All except XTAL1, 2, RESET)
= 0.6V (XTAL1, 2, RESET)
V_{IH} = 2.0V (All except XTAL1, 2, RESET)
= 3.8V (XTAL1, 2, RESET)
V_{OL} = 0.45V
V_{OH} = 2.4V

Output Load
D0-D7 : C_L = 150pF
All other outputs: C_L = 80pF

Timing Diagram

Figure 1. Data Bus Buffer (DBB) Read Operation

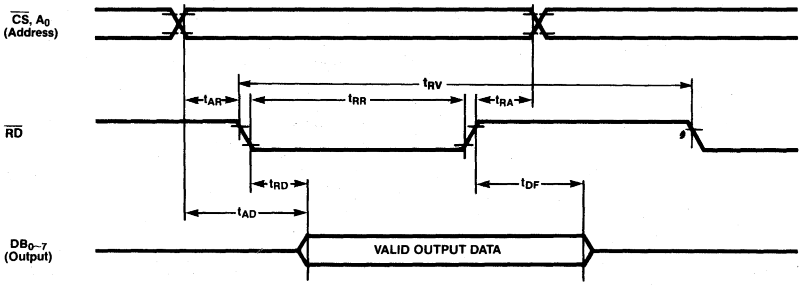
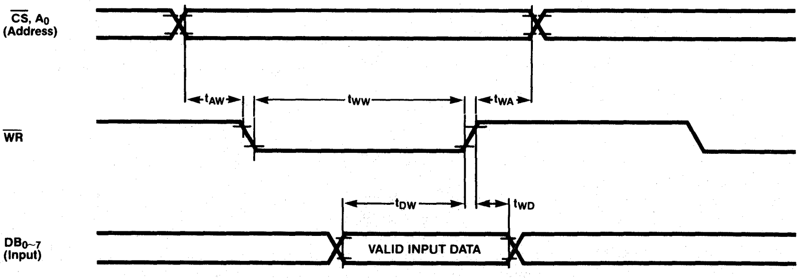


Figure 2. Data Bus Buffer (DBB) Write Operation



Timing Diagram
(Continued)

Figure 3. Port 2 (Lower 4 Bits) Operation in Connection with I/O Expander

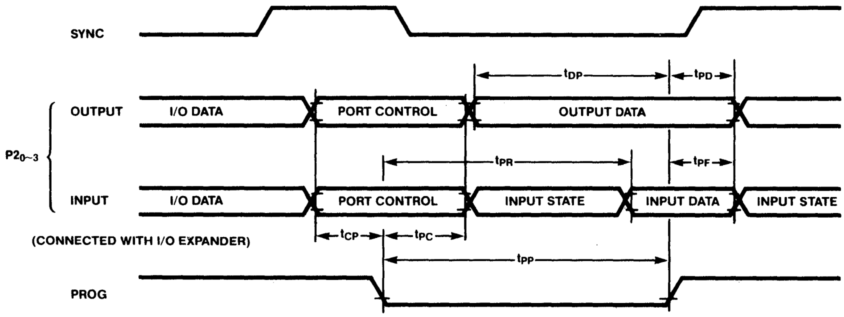
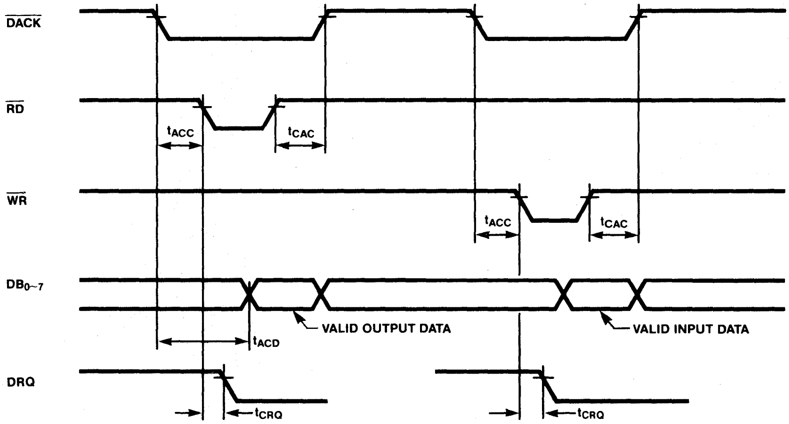
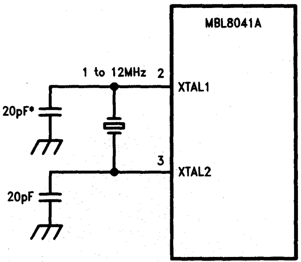


Figure 4. DMA Operation



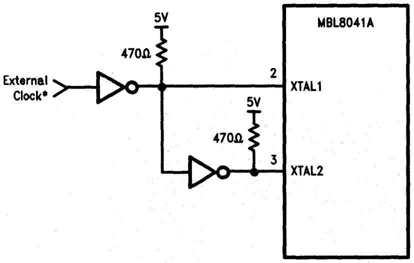
Oscillation Circuits

Crystal Oscillator



*Including capacitances

External Clock Drive

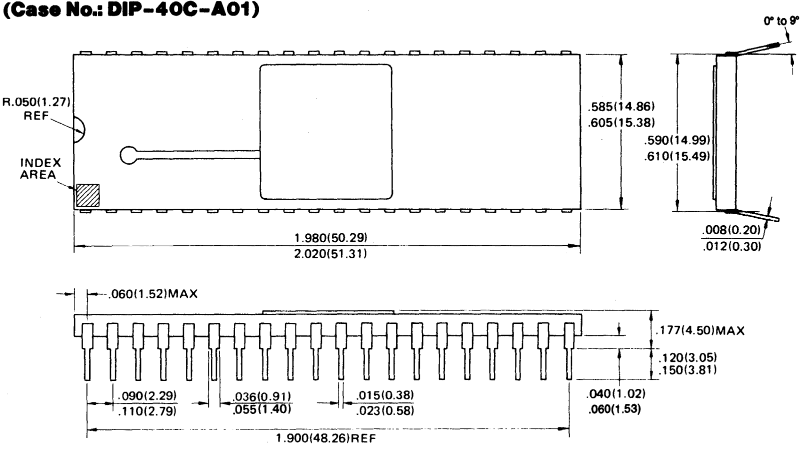


* Both high and low times should be more than 35% of the cycle time, and rise and fall times should be less than 20 ns.

Package Dimensions

Dimensions in inches (millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)



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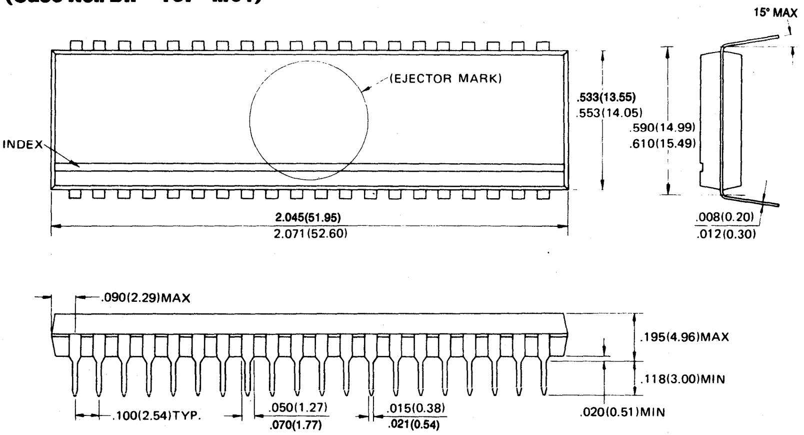
Dimensions in inches (millimeters)

40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



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MBL8042H/N

NMOS Universal Peripheral Interface 8-Bit Microcomputer

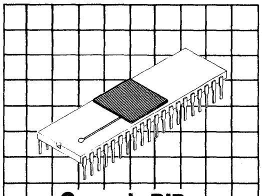
October 1986
Edition 2.0

Description

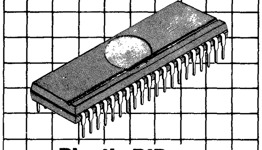
The MBL8042 Universal Peripheral Interface is a single-chip 8-bit microcomputer based on an 8-bit parallel microprocessor chip.

The MBL8042 is fabricated with an N-channel silicon-gate MOS process. The MBL8042 has a 2K x 8-bit ROM for program memory, a 128 x 8-bit RAM for data memory, 18 I/O ports, an 8-bit timer/counter and clock generator on the chip, and is powered by single +5V.supply.

The MBL8042 is designed to operate as a slave processor, which receives commands and data from the master processor, controls peripheral devices and transfers input data from peripheral devices to the master processor. By using the MBL8042 an intelligent peripheral controller can be designed freely.



Ceramic DIP
DIP-40C-A01

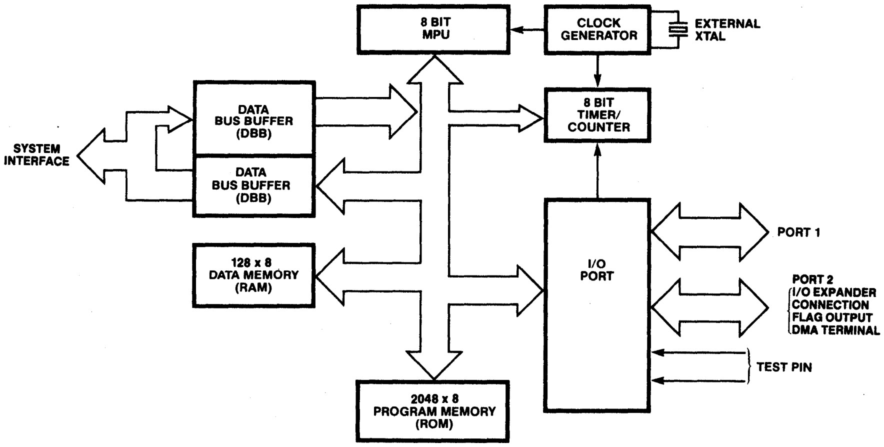


Plastic DIP
DIP-40P-M01

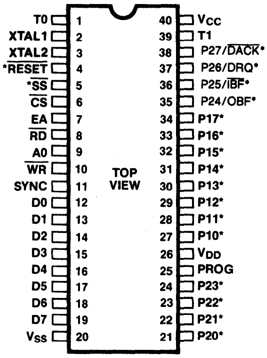
Features

- **Processor:**
  8-bit parallel processing
- **Register:**
  One 8-bit Status Register (for Interface with master processor)
  Two 8-bit Data Bus Buffer Registers (for Input/Output)
- **Memory**
  — 2K x 8 bit ROM (for program memory)
  — 128 x 8 bit RAM (for data memory)
- **I/O:**
  One 8-bit Bidirectional Data Bus
  Two 8-bit Bidirectional I/O Ports
  Two Test Inputs
- **Clock Source:**
  Clock Generator (with External Crystal Resonator) or External Clock
- **8-Bit Interval Timer/Event Counter**
- **Low-power Standby Operation Capability**
- **Power-on Reset Capability (with External Capacitor)**
- **Instruction Set:**
  93 Instructions
  (217 Instruction Codes)
  — 1-byte Instruction (about 70%), 2-byte Instruction (about 30%)
  — 1-cycle or 2-cycle Instruction (1 cycle = 2.5µs at 6MHz XTAL)
- **Technology:**
  N-channel Silicon-gate E/D MOS Process
- **Two Package Options:**
  Standard 40–pin Ceramic (Suffix-C) or Plastic DIP (Suffix–P)
- **Equivalent:**
  Intel 8042

Block Diagram



Pin Assignment



*These pins are internally pulled up

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Pin Descriptions

Pin No.	Name	Symbol	Description
1	Test 0	T_0	Conditional Input for Conditional Branch
2	Crystal 1	XTAL 1	Input pin for an internal Clock Generator connected to external crystal. Also, this pin can be used as input from an external clock source.
3	Crystal 2	XTAL 2	Input pin for an internal Clock Generater connected to external crystal. (Note: The XTAL 1 and XTAL 2 input levels are not TTL compatible).
4	Reset	$\overline{\text{RESET}}$	Resets and forces the MPU to be initialized. (Note: This input level is not TTL compatible).
5	Single Step	$\overline{\text{SS}}$	Input pin used for single step operation.
6	Chip Select	$\overline{\text{CS}}$	Input pin used for the master processor to select the UPI.
7	External Address	EA	Input pin used for controlling program memory access. Holding EA high forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.
8	Read Strobe	$\overline{\text{RD}}$	Strobe input enables the MBL8042 to read contents of the Data Bus Buffer register or Status register.
9	Address "0"	A_0	Address input to read/write data or read/write commands. A_0 = "L" indicates data read or write. A_0 = "H" indicates status read or command write.
10	Write Strobe	$\overline{\text{WR}}$	Strobe input enables the MBL8042 to write data into its Data Buffer register.
11	Sync	SYNC	A clock output pin indicating the MBL8042 instruction cycle. This pin is used when a synchronization signal is required for external circuits .
12 thru 19	Data Bus	DB_0 thru DB_7	8-bit bidirectional I/O port used to interface the MBL8042 to the master processor.
20	Ground	V_{SS}	Ground terminal.
21 thru 24	Port 2	$P2_0$ thru $P2_3$	Lower 4 bits of the quasi-bidirectional I/O port (Port 2). These function as interface port with the I/O expander (MBL8243) when an expansion I/O executes instruction. During single step operation upper 3 bits of the program fetch address are output on P20, P21, P22.
25	Program	PROG	A strobe signal output pin for an I/O expander (MBL8243) used, when performing an expansion I/O instruction.
26	Power Supply	V_{DD}	Power supply pin (+5V) for internal RAM.
27 thru 34	Port 1	$P1_0$ thru $P1_7$	Quasi-bidirectional I/O ports (Port 1). During single step operation, the next program fetch address (Lower 8 bits) is output.
35 thru 38	Port 2	$P2_4$ thru $P2_7$	Upper 4 bits of the quasi-bidirectional I/O port (port 2). These function as the flag output pins ($P2_4$ and $P2_5$) and DMA pins ($P2_6$ and $P2_7$) according to instructions.
39	Test 1	T_1	This pin has the following functions according to instruction: 1. Event Input pin for the Event Counter. 2. Condition Input pin for Conditional Branch.
40	Power Supply	V_{CC}	Power supply pin (+5V).

System Interface

The master processor and MBL8042 are interfaced through the data bus buffer.

MBL8042 has 2 internal DBB (Data Bus Buffer) registers. The register to be accessed is determined by the address line and strobe signal.

Flag 1 (F1) is set when a command is written (A_0 = 1), and reset when data is written (A_0 = 0).

The master processor can read only data from the output DBB register, and cannot read and check data or commands which the master processor has written itself.

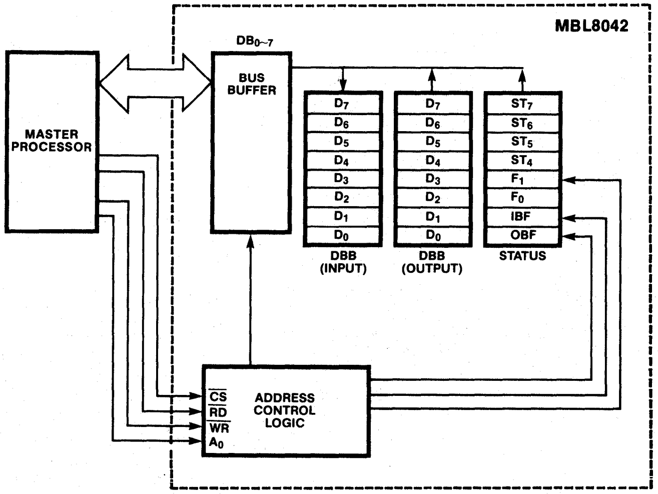
When MBL8042 writes data to the output DBB with the OUT DBB, A instruction, OBF is set.

When DBB is read ($\overline{CS}$ = RD = A_0 = 0, $\overline{WR}$ = 1) by the master processor, OBF is reset. IBF is set when the master processor writes to the DBB, and reset when MBL8042 reads data from the DBB with IN A, DBB instruction.

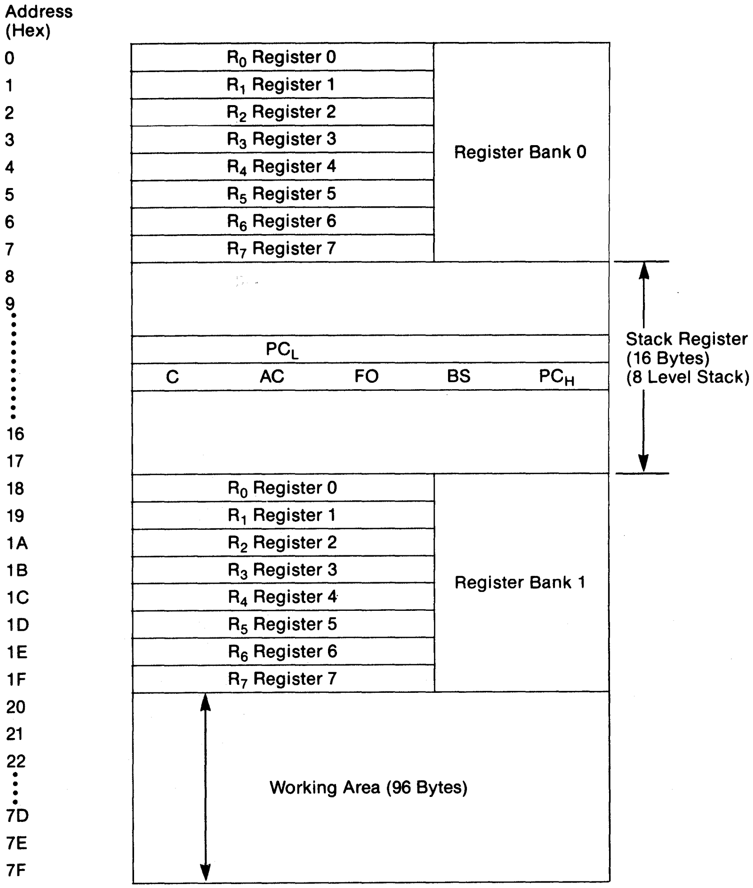
The internal status of the MBL8042 does not change when the status register contents are read out.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	Description
0	0	1	0	Read DBB (Output) register.
0	0	1	1	Read Status Register.
0	1	0	0	Write DBB (Input) register (Data).
0	1	0	1	Write DBB (Input) register (Command).
1	x	x	x	Invalid.

Interface between MBL8042 and Master Processor



Resident Data Memory Map (RAM)



Status Register (PSW)

The Status Register is an 8-bit register configured as shown in the following figure. The upper four bits are used for flags to indicate the status of the MPU and when a sub-routine call or an interrupt occurs, the contents of the program counter is transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining one bit is an unused bit.

7	6	5	4	3	2	1	0
C	AC	F_0	BS	1	SP_2	SP_1	SP_0
← Flags →				(Unused Bit)	← Stack Pointer →		

Flags

C (Carry): When an overflow occurs in the Accumulator, this bit is set to "1".

AC (Auxiliary Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator, this bit is set to "1".

F_0 (User Flag): This flag can be controlled as a user flag by the proper instruction.

BS (Bank Select): This flag can be controlled to select a Register Bank by an instruction. When BS = 0, Register Bank 0 is selected. When BS = 1, the Register Bank 1 is selected.

Stack Register (8 Level Capability)

The Stack Register has 16 bytes of memory area in the built-in RAM. The stack Register consists of eight levels, i.e. a Stack level consists of two bytes as shown below.

SP (Stack Pointer): In the diagram below, "SP" indicates a Stack Pointer address to be used for the next sub-routine call or interrupt. "SP" is given an 8-bit code from the lower three bits of Status Register as follows:

$$SP = 00001\underbrace{SP_2SP_1SP_0}_{\text{Status Register Bits 0 to 2.}}$$

PC_n (Program Counter): "PC_n" indicates the contents of the n-th bit in the Program Counter.

Interrupt Processing (IBF Interrupt, Timer/Counter Interrupt)

There are two types of interrupt: the IBF interrupt and Timer/Counter interrupt.

If an interrupt occurs when the system is in "interrupt enable" status, the interrupt flag is set as soon as the current instruction is completed.

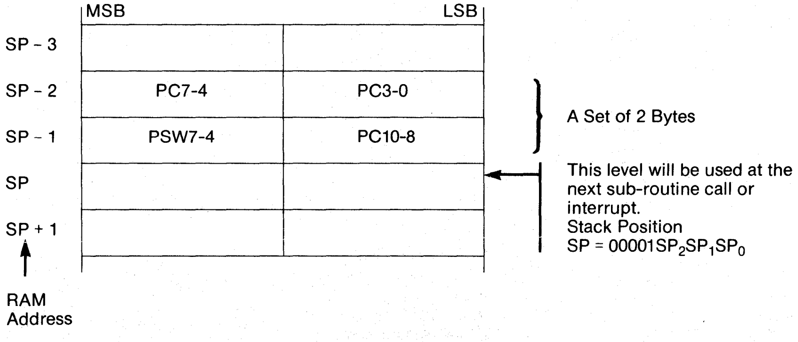
When the interrupt processing begins, the Status and Program Counter contents are first stored in the stack. Then, operation jumps to Address 3 in the case of the IBF interrupt and Address 7 in the case of a timer interrupt.

After the interrupt has been processed by a user program and RETR (Return and Restore Status) instruction has been executed, the Status and Program Counter contents stored in the stack are restored, the interrupt flag is reset and the system is ready to accept the next interrupt request.

A Timer/Counter interrupt request occurs when the Timer/Counter overflow flag is set due to Timer/Counter overflow.

However, since the Timer/Counter interrupt request is masked by the IBF interrupt request, IBF interrupt has first priority.

The Timer/Counter interrupt is enabled after the IBF interrupt has been executed and the system has become ready to receive the next interrupt request.

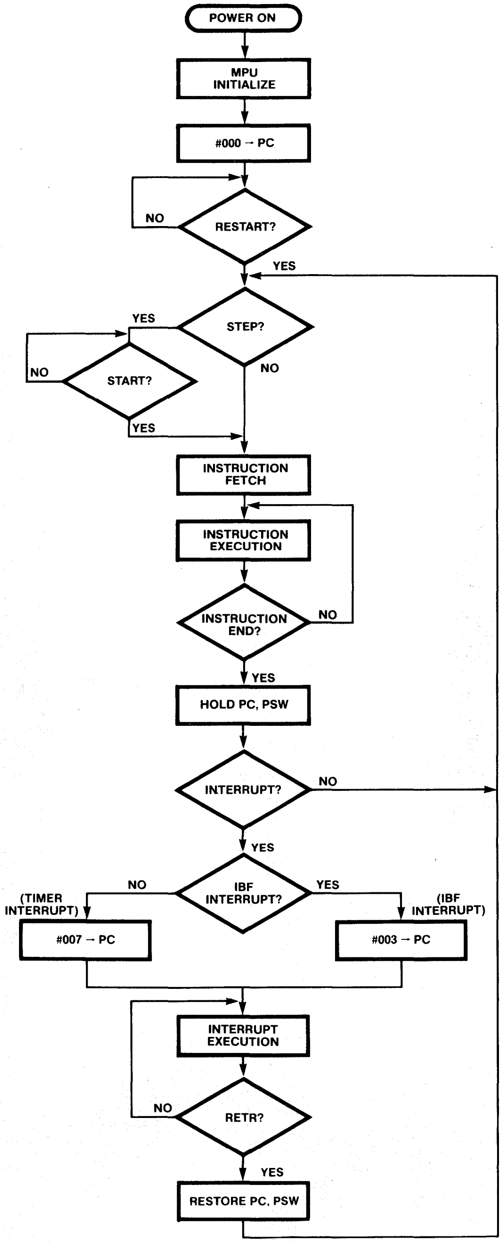


RAM Address	MSB	LSB
SP - 3		
SP - 2	PC7-4	PC3-0
SP - 1	PSW7-4	PC10-8
SP		
SP + 1		

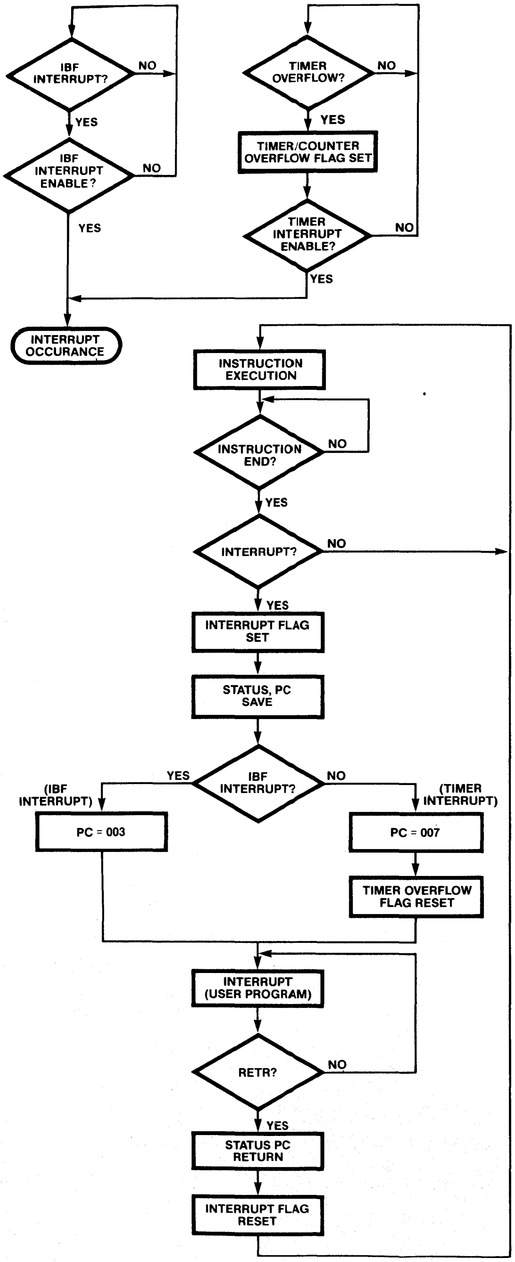
A Set of 2 Bytes

This level will be used at the next sub-routine call or interrupt.
Stack Position
$SP = 00001SP_2SP_1SP_0$

Operation Flow Chart

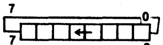
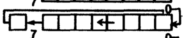
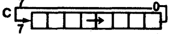
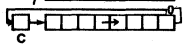


Interrupt Flow Chart



Instruction Set Summary

Accumulator

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Add register to A	ADD A, Rr	6X	1	1	*	*	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	*	*	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	*	*	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	*	*	(A) ← (A) + data
Add register to A with Carry	ADDC A, Rr	7X	1	1	*	*	(A) ← (A) + (Rr) + C
Add data memory to A with Carry	ADDC A, @R0	70	1	1	*	*	(A) ← (A) + ((R0)) + C
	ADDC A, @R1	71	1	1	*	*	(A) ← (A) + ((R1)) + C
Add immediate to A with Carry	ADDC A, #data	13	2	2	*	*	(A) ← (A) + data + C
AND register to A	ANL A, Rr	5X	1	1	—	—	(A) ← (A) AND (Rr)
AND data memory to A	ANL A, @R0	50	1	1	—	—	(A) ← (A) AND (R0)
	ANL A, @R1	51	1	1	—	—	(A) ← (A) AND (R1)
AND immediate to A	ANL A, #data	53	2	2	—	—	(A) ← (A) AND data
OR register to A	ORL A, Rr	4X	1	1	—	—	(A) ← (A) OR (Rr)
OR data memory to A	ORL A, @R0	40	1	1	—	—	(A) ← (A) OR ((R0))
	ORL A, @R1	41	1	1	—	—	(A) ← (A) OR ((R1))
OR immediate to A	ORL A, #data	43	2	2	—	—	(A) ← (A) OR data
Exclusive OR register to A	XRL A, Rr	DX	1	1	—	—	(A) ← (A) XOR (Rr)
Exclusive OR data memory to A	XRL A, @R0	D0	1	1	—	—	(A) ← (A) XOR ((R0))
	XRL A, @R1	D1	1	1	—	—	(A) ← (A) XOR ((R1))
Exclusive OR immediate to A	XRL A, #data	D3	2	2	—	—	(A) → (A) XOR data
Increment A	INC A	17	1	1	—	—	(A) ← (A) + 1
Decrement A	DEC A	07	1	1	—	—	(A) ← (A) - 1
Clear A	CLR A	27	1	1	—	—	(A) ← 0
Complement A	CPL A	37	1	1	—	—	(A) ← $(\bar{A})$
Decimal Adjust A	DA A	57	1	1	*	—	Note (1)
Swap nibbles of A	SWAP A	47	1	1	—	—	(A7~4) ⇄ (A3~0)
Rotate A Left	RL A	E7	1	1	—	—	
Rotate A Left through Carry	RLC A	F7	1	1	*	—	
Rotate A Right	RR A	77	1	1	—	—	
Rotate A Right through Carry	RRC A	67	1	1	*	—	

Note 1: The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.
Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction.

Input/Output

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Input port to A	IN A, P1	09	1	2	—	—	(A) ← (P1)
	IN A, P2	0A	1	2	—	—	(A) ← (P2)
Output A to port	OUTL P1, A	39	1	2	—	—	(P1) ← (A)
	OUTL P2, A	3A	1	2	—	—	(P2) ← (A)
AND immediate to port	ANL P1, #data	99	2	2	—	—	(P1) ← (P1) AND data
	ANL P2, #data	9A	2	2	—	—	(P2) ← (P2) AND data
OR immediate to port	ORL P1, #data	89	2	2	—	—	(P1) ← (P1) OR data
	ORL P2, #data	8A	2	2	—	—	(P2) ← (P2) OR data
Input DBB to A, clear IBF	IN A, DBB	22	1	1	—	—	(A) ← (DBB), (IBF) ← 0
Output A to DBB, set OBF	OUT DBB, A	02	1	1	—	—	(DBB) ← (A), (OBF) ← 1
A7~4 to bits 7~4 of Status	MOV STS, A	90	1	1	—	—	(STS7)~4) ← (A7~4)
Input Expander port to A	MOVD A, P_P	0X	1	2	—	—	(A3~0) ← (P_P), (A7~4) ← 0
Output A to Expander port	MOVD P_P, A	3X	1	2	—	—	(P_P) ← (A3~0)
AND A to Expander port	ANLD P_P, A	9X	1	2	—	—	(P_P) ← (P_P) AND (A3~0)
OR A to Expander port	ORLD P_P, A	8X	1	2	—	—	(P_P) ← (P_P) OR (A3~0)

Operation Code X: Table 2

Instruction Set Summary
(Continued)

Data Moves

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Move register to A	MOV A, Rr	FX	1	1	—	—	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	—	—	(A) ← ((R0))
	MOV A, @R1	F1	1	1	—	—	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	—	—	(A) ← data
Move A to register	MOV Rr, A	AX	1	1	—	—	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	—	—	((R0)) ← (A)
	MOV @R1, A	A1	1	1	—	—	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX	2	2	—	—	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	—	—	((R0)) ← data
	MOV @R1, #data	B1	2	2	—	—	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	—	—	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*	*	(PSW) ← (A)
Exchange A and register	XCH A, Rr	2X	1	1	—	—	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	—	—	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	—	—	(A) ⇄ ((R1))
Exchange digit of A and data memory	XCHD A, @R0	30	1	1	—	—	(A3~0) ⇄ ((R0)3~0)
	XCHD A, @R1	31	1	1	—	—	(A3~0) ⇄ ((R1)3~0)
Move to A from current page	MOVP A, @A	A3	1	2	—	—	(A) ← ((A)) within page
Move to A from Page 3	MOVP3 A, @A	E3	1	2	—	—	(A) ← ((A)) within page 3

Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction.

Timer/Counter

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Read Timer/Counter	MOV A, T	42	1	1	—	—	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	—	—	(T) ← (A)
Start Timer	STRT T	55	1	1	—	—	
Start Counter	STRT CNT	45	1	1	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	
Enable Timer/ Counter Interrupt	EN TCNTI	25	1	1	—	—	
Disable Timer/ Counter Interrupt	DIS TCNTI	35	1	1	—	—	

Control

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	Flag AC	Note
Enable DMA Handshake Lines	EN DMA	E5	1	1	—	—	
Enable IBF Interrupt	EN I	05	1	1	—	—	
Disable IBF Interrupt	DIS I	15	1	1	—	—	
Enable Master Interrupts	EN FLAGS	F5	1	1	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	—	—	(BS) ← 1
No Operation	NOP	00	1	1	—	—	

Instruction Set Summary
(Continued)

Register

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Increment register	INC Rr	1X	1	1	—	—	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	—	—	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	—	—	((R1)) ← ((R1)) + 1
Decrement register	DEC Rr	CX	1	1	—	—	(Rr) ← (Rr) - 1

Operation Code X: Table 1

Subroutine

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Jump to Subroutine	CALL addr	%4	2	2	—	—	Note (2)
Return	RET	83	1	2	—	—	Note (3)
Return and restore status	RETR	93	1	2	*	*	Note (4)

Operation Code %: Table 3
Flag*: This flag is set or reset in the state after executed instruction.

Flags

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Clear Carry	CLR C	97	1	1	Z	—	(C) ← 0
Complement Carry	CPL C	A7	1	1	CP	—	(C) ← ($\overline{C}$)
Clear Flag 0	CLR F0	85	1	1	—	—	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	—	—	(F0) ← ($\overline{F0}$)
Clear Flag 1	CLR F1	A5	1	1	—	—	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	—	—	(F1) ← ($\overline{F1}$)

Flag Z: Reset CP: Invert

Branch

Operation	Mnemonic	OP Code	Byte	Cycle	Flag C	AC	Note
Jump unconditional	JMP addr	%4	2	2	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	Unconditional Branch Note (5)
Decrement register and jump	DJNZ Rr,addr	EX	2	2	—	—	(Rr) ≠ 0 Note (6)
Jump on Carry = 1	JC addr	F6	2	2	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	(C) = 0
Jump on A Zero	JZ addr	C6	2	2	—	—	(A) = 0
Jump on A not Zero	JNZ addr	96	2	2	—	—	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	—	—	(T0) = H
Jump on T0 = 0	JNT0 addr	26	2	2	—	—	(T0) = L
Jump on T1 = 1	JT1 addr	56	2	2	—	—	(T1) = H
Jump on T1 = 0	JNT1 addr	46	2	2	—	—	(T1) = L
Jump on F0 = 1	JF0 addr	B6	2	2	—	—	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	—	—	(F1) = 1
Jump on Timer Flag = 1, Clear Flag	JTF addr	16	2	2	—	—	(TF) = 1
Jump on IBF Flag = 0	JNIBF addr	D6	2	2	—	—	(IBF) = 0
Jump on OBF Flag = 1	JOBF addr	86	2	2	—	—	(OBF) = 1
Jump on Accumulator Bit	JBb addr	%2	2	2	—	—	(Ab) = 1

Operation Code X: Table 1
%: Table 3

Note 2: Call addr
((SP)) ← (PC), (PSW7~4)
(SP) ← (SP) + 1
(PC10 ~ 8) ← A_H
(PC7~0) ← A_L

Note 3: RET
(SP) ← (SP) - 1
(PC) ← ((SP))

Note 4: RETR
(SP) ← (SP) - 1
(PC) ← ((SP))
(PSW7~4) ← ((SP))

Note 5: JMPP @
(PC7~0) ← ((A))

Note 6: DJNZ Rr, addr
(Rr) ← (Rr) - 1
if (Rr) ≠ 0 (PC7~0) ← addr
if (Rr) = 0 Execute next instruction

Instruction Set Summary
(Continued)

OP Code Of Register Access (Table 1)

Mnemonic	Rr	R0	R1	R2	R3	R4	R5	R6	R7
ADD A,Rr		63	69	6A	6B	6C	6D	6E	6F
ADDC A,Rr		78	79	7A	7B	7C	7D	7E	7F
ANL A,Rr		58	59	5A	5B	5C	5D	5E	5F
DEC Rr		C8	C9	CA	CB	CC	CD	CE	CF
DJNZ Rr, addr		E8	E9	EA	EB	EC	ED	EE	EF
INC Rr		18	19	1A	1B	1C	1D	1E	1F
MOV A,Rr		F8	F9	FA	FB	FC	FD	FE	FF
MOV Rr,A		A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data		B8	B9	BA	BB	BC	BD	BE	BF
ORL A, Rr		48	49	4A	4B	4C	4D	4E	4F
XCH A,Rr		28	29	2A	2B	2C	2D	2E	2F
XRL A,Rr		D8	D9	DA	DB	DC	DD	DE	DF

bit 7	6	5	4	3	2	1	0
					r_2	r_1	r_0

OP Code Of Expander (Table 2)

Mnemonic	PP	P4	P5	P6	P7
ANLD P_P, A		9C	9D	9E	9F
MOVD A, P_P		0C	0D	0E	0F
MOVD P_P, A		3C	3D	3E	3F
ORLD P_P, A		8C	8D	8E	8F

bit 7	6	5	4	3	2	1	0
						P_1	P_0

OP Code Of JMP, CALL, JBb (Table 3)

	First Byte						Second Byte
	bit 7 6 5	4	3	2	1	0	bit 7 6 5 4 3 2 1 0
JMP	A_H	0	0	1	0	0	A_L
CALL	A_H	1	0	1	0	0	A_L
JB_b	B_b	1	0	0	1	0	A_L

A_H; Address A_{10}, A_9, A_8
A_L; Address A_7 to A_0
B_b; b-th Bit on Accumulator

Instruction Codes

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUT DBB,A	ADD A, # ◥	JMP 0 x x ◥	EN I		DEC A		◤ IN A, P1	◤ IN A, P2		◤ MOVD A, P4	◤ MOVD A, P5	◤ MOVD A, P6	◤ MOVD A, P7
1	INC @R0	INC @R1	JB0 addr ◥	ADDC A, # ◥	CALL 0 x x ◥	DIS I	JTF addr ◥	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A, @R0	XCH A, @R1	IN A, DBB	MOV A, # ◥	JMP 1 x x ◥	EN TCNTI	JNT0 addr ◥	CLR A	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
3	XCHD A, @R0	XCHD A, @R1	JB1 addr ◥		CALL 1 x x ◥	DIS TCNTI	JT0 addr ◥	CPL A		◤ OUTL P1, A	◤ OUTL P2, A		◤ MOVD P4, A	◤ MOVD P5, A	◤ MOVD P6, A	◤ MOVD P7, A
4	ORL A, @R0	ORL A, @R1	MOV A, T	ORL A, # ◥	JMP 2 x x ◥	STRT CNT	JNT1 addr ◥	SWAP A	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5	ANL A, @R0	ANL A, @R1	JB2 addr ◥	ANL A, # ◥	CALL 2 x x ◥	STRT T	JT1 addr ◥	DA A	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6	ADD A, @R0	ADD A, @R1	MOV T, A		JMP 3 x x ◥	STOP TCNT		RRC A	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
7	ADDC A, @R0	ADDC A, @R1	JB3 addr ◥		CALL 3 x x ◥		JF1 addr ◥	RR A	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
8				◤ RET	JMP 4 x x ◥	CLR F0	JOBF addr ◥			ORL P1, # ◥	ORL P2, # ◥		◤ ORLD P4, A	◤ ORLD P5, A	◤ ORLD P6, A	◤ ORLD P7, A
9	MOV STS, A		JB4 addr ◥	◤ RETR	CALL 4 x x ◥	CPL F0	JNZ addr ◥	CLR C		ANL P1, # ◥	ANL P2, # ◥		◤ ANLD P4, A	◤ ANLD P5, A	◤ ANLD P6, A	◤ ANLD P7, A
A	MOV @R0, A	MOV @R1, A		◤ MOVP A, @A	JMP 5 x x ◥	CLR F1		CPL C	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A
B	MOV @R0, # ◥	MOV @R1, # ◥	JB5 addr ◥	◤ JMPP @A	CALL 5 x x ◥	CPL F1	JF0 addr ◥		MOV R0, # ◥	MOV R1, # ◥	MOV R2, # ◥	MOV R3, # ◥	MOV R4, # ◥	MOV R5, # ◥	MOV R6, # ◥	MOV R7, # ◥
C					JMP 6 x x ◥	SEL RB0	JZ addr ◥	MOV A, PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A, @R0	XRL A, @R1	JB6 addr ◥	XRL A, # ◥	CALL 6 x x ◥	SEL RB1	JNIBF addr ◥	MOV PSW, A	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
E				◤ MOVP3 A.@A	JMP 7 x x ◥	EN DMA	JNC addr ◥	RL A	DJNZ R0, addr ◥	DJNZ R1, addr ◥	DJNZ R2, addr ◥	DJNZ R3, addr ◥	DJNZ R4, addr ◥	DJNZ R5, addr ◥	DJNZ R6, addr ◥	DJNZ R7, addr ◥
F	MOV A, @R0	MOV A, @R1	JB7 addr ◥		CALL 7 x x ◥	EN FLAGS	JC addr ◥	RLC A	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7

#: Immediate data

□	1 Byte, 1 Cycle Instruction
◤	1 Byte, 2 Cycle Instruction
◥	2 Byte, 2 Cycle Instruction

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	+5.0 ±10%	V
	V_{SS}	0	V
Operating Temperature		0 to +70	°C

DC Characteristics

(T_A = 0° C to +70° C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Value		Unit
				Min.	Max.	
Input Low Voltage	All Except XTAL1, 2, $\overline{\text{RESET}}$	V_{IL}		-0.3	0.8	V
	XTAL1,2, $\overline{\text{RESET}}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All Except XTAL1, 2, $\overline{\text{RESET}}$	V_{IH}		2.0	V_{CC}	V
	XTAL1,2, $\overline{\text{RESET}}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	DB_0 to DB_7	V_{OL}	I_{OL} = 2.0mA		0.45	V
	P10-P17, P20-P27 SYNC	V_{OL1}	I_{OL} = 1.6mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
Output High Voltage	DB_0 to DB_7	V_{OH}	I_{OH} = -400μA	2.4		
	All other outputs	V_{OH1}	I_{OH} = -50μA	2.4		
Input Leakage Current	T_0, T_1, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, A_0, EA	I_{IL}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		±10	μA
Output Leakage Current	DB_0 to DB_7 (High Z State)	I_{OL}	$V_{SS}+0.45V \leqq V_{IN} \leqq V_{CC}$		±10	μA
Input Low Current	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$	I_{LI}	V_{IL} = 0.8V		0.5	mA
	$\overline{\text{RESET}}$, $\overline{\text{SS}}$	I_{LI1}	V_{IL} = 0.8V		0.2	mA
V_{DD} Supply Current		I_{DD}			15	mA
Supply Current		I_{CC} + I_{DD}			125	mA

AC Characteristics

(T_A = 0° C to +70° C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V)

Data Bus Buffer Register Read (Refer to the Fig. 1)

Parameter		Symbol	Test Conditions	Value Min.	Value Max.	Unit
$\overline{\text{CS}}$, A_0 Setup Time (to $\overline{\text{RD}}$)		t_{AR}		0		ns
$\overline{\text{CS}}$, A_0 Hold Time (from $\overline{\text{RD}}$)		t_{RA}		0		ns
$\overline{\text{RD}}$ Pulse Width		t_{RR}		160		ns
Data Delay Time (from $\overline{\text{CS}}$, A_0)		t_{AD}	C_L = 150pF		130	ns
Data Delay Time (from $\overline{\text{RD}}$)		t_{RD}	C_L = 150pF		130	ns
Data Floating Time (from $\overline{\text{RD}}$)		t_{DF}			85	ns
Cycle Time	MBL8042N	t_{CY}	*	2.5	15.0	μs
	MBL8042H		**	1.25	15.0	μs

*t_{CY} = 2.50μs at 6MHz XTAL (N version)
**t_{CY} = 1.25μs at 12MHz XTAL (H version)

Data Bus Buffer Register Write (Refer to the Fig. 2)

Parameter	Symbol	Test Conditions	Value Min.	Value Max.	Unit
$\overline{\text{CS}}$, A_0 Setup Time (to $\overline{\text{WR}}$)	t_{AW}		0		ns
$\overline{\text{CS}}$, A_0 Hold Time (from $\overline{\text{WR}}$)	t_{WA}		0		ns
$\overline{\text{WR}}$ Pulse Width	t_{WW}		160		ns
Data Setup Time (to $\overline{\text{WR}}$)	t_{DW}		130		ns
Data Hold Time (from $\overline{\text{WR}}$)	t_{WD}		0		ns

Port 2 (Refer to the Fig. 3)*

		MBL8042N		MBL8042H		
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
Port Control Setup before Falling Edge of PROG Time (to PROG)	t_{CP}	100		110		ns
Port Control Hold after Falling Edge of PROG Time (from PROG)	t_{PC}	60		100		ns
Output Data Setup Time (to PROG)	t_{DP}	200		250		ns
Output Data Hold Time (from PROG)	t_{PD}	20		65		ns
Input Data Hold Time (from PROG)	t_{PF}	0	150	0	150	ns
PROG Time P2 Input Must be Valid	t_{PR}		650		810	ns
PROG Pulse Width	t_{PP}	700		1200		ns

*at 6MHz XTAL for N version
at 12MHz XTAL for H version

AC Characteristics
(Continued)

DMA Characteristics (Refer to the Fig. 4)

Parameter	Symbol	Test Conditions	Value Min.	Value Max.	Unit
$\overline{\text{DACK}}$ Setup Time (to $\overline{\text{RD}}$, $\overline{\text{WR}}$)	t_{ACC}		0		ns
$\overline{\text{DACK}}$ Hold Time (from $\overline{\text{RD}}$, $\overline{\text{WR}}$)	t_{CAC}		0		ns
Input Data Delay Time (from $\overline{\text{DACK}}$)	t_{ACD}	C_L = 150pF		130	ns
DRQ Clear Time (from $\overline{\text{RD}}$, $\overline{\text{WR}}$)	t_{CRQ}			100	ns

AC Test Conditions
V_{IL} = 0.8V (All except XTAL1, 2, $\overline{\text{RESET}}$)
= 0.6V (XTAL1, 2, $\overline{\text{RESET}}$)
V_{IH} = 2.0V (All except XTAL1, 2, $\overline{\text{RESET}}$)
= 3.8V (XTAL1, 2, $\overline{\text{RESET}}$)
V_{OL} = 0.45V
V_{OH} = 2.4V

Output Load
D0-D7 : C_L = 150pF
All other outputs: C_L = 80pF

Timing Diagram

Figure 1. Data Bus Buffer (DBB) Read Operation

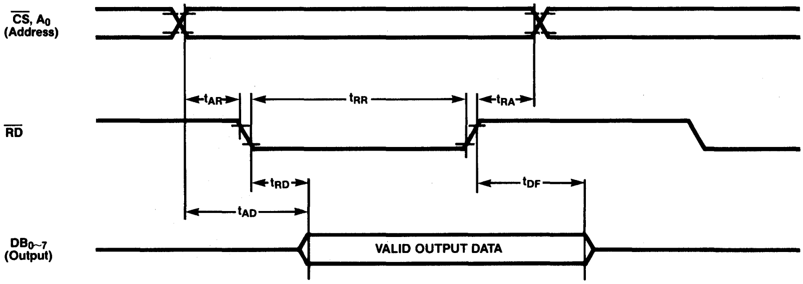
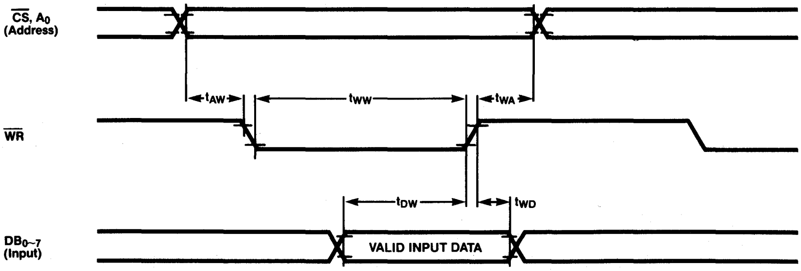


Figure 2. Data Bus Buffer (DBB) Write Operation



Timing Diagram
(Continued)

Figure 3. Port 2 (Lower 4 Bits) Operation in Connection with I/O Expander

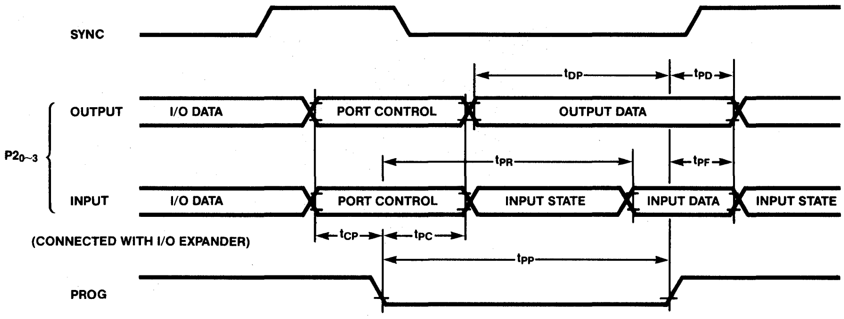
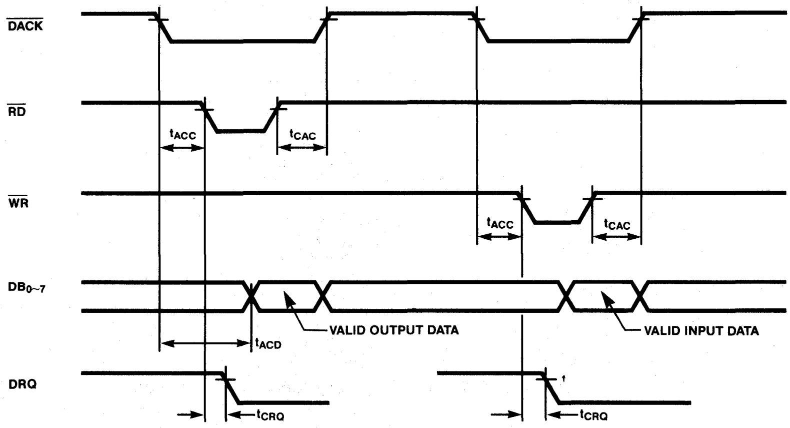
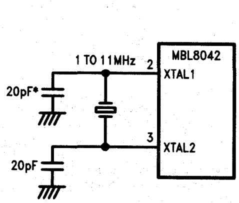


Figure 4. DMA Operation



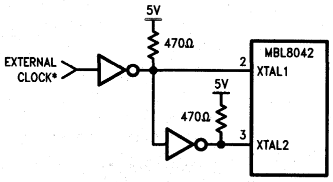
Oscillation Circuits

Crystal Oscillator



* Including stray capacitances

External Clock Driver

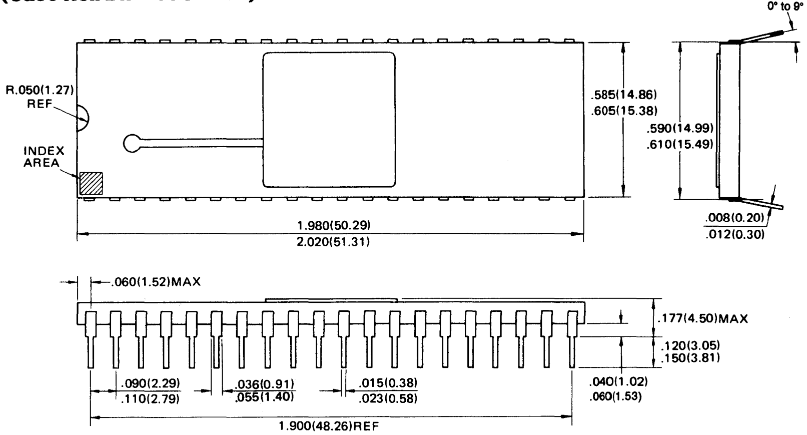


* Both high and low times should be more than 35% of the cycle time, and rise and fall times should be less than 20 ns.

Package Dimensions

Dimensions in inches (millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-40C-A01)



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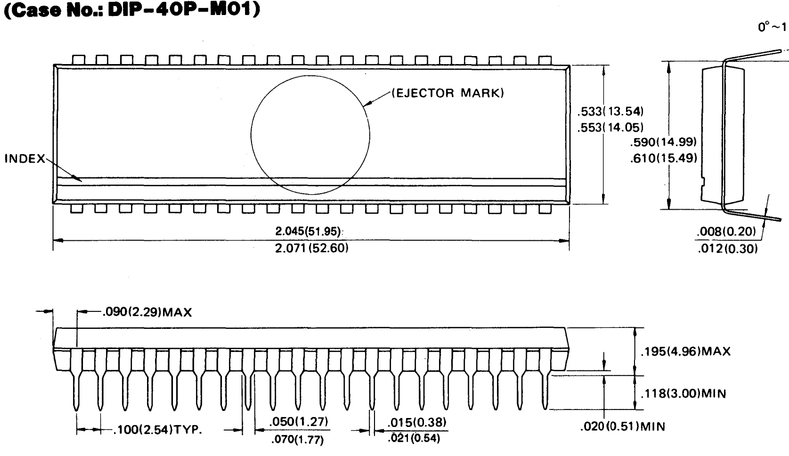
Dimensions in inches (millimeters)

40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)



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FUJITSU

NMOS UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

MBL8742H/N

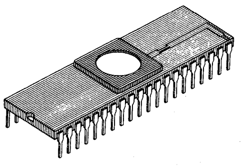
October 1986
Edition 1.0

DESCRIPTION

The Fujitsu MBL8742 Universal Peripheral Interface (UPI) is an 8-bit microcomputer that uses a 2K × 8-bit Electrically Programmable Read Only Memory (EPROM). Besides the EPROM program memory, the microprocessing circuits are supported by a 256 × 8-bit static RAM, 18 I/O lines, an 8-bit timer counter, and a clock generator. The device can be ordered in either of two speed versions: N-version for operation at 6MHz and H-version for operation at 12MHz. For either frequency, the operating temperature is 0° C to 70° C.

The MBL8742 is fabricated using an N-channel polysilicon-gate MOS process and is housed in a 40-pin ceramic windowed DIP. A single +5-volt supply is required for basic operation; the EPROM requires an ultraviolet (UV) light source for erasure and a 21-volt supply for programming.

Using the EPROM program memory, the MBL8742 is ideally suited for such applications as system evaluation, system prototyping, and low-volume production work.

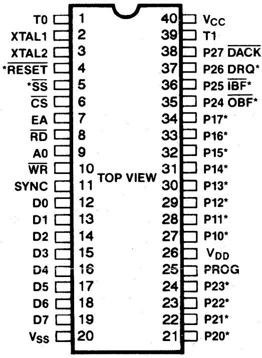


Ceramic DIP
(DIP-40C-A04)

FEATURES

- Processor: 8-bit Microprocessing Unit (MPU)
- Memories: 2K × 8-bit Program Memory (EPROM)
  256 × 8-bit Data Memory (static RAM)
  — 8-level Stack
  — 8 pairs of Working Registers
- I/O: One 8-bit Bidirectional Data Bus
  Two 8-bit Bidirectional I/O Ports
  Two Test Inputs
- Master Processor Interface: One 8-bit Status Register
  Two 8-bit Data Bus Buffer Registers
- DMA Handshake Capability
- 8-bit Timer/Event Counter
- Clock Source: Internal Clock Generator (with external Crystal) or External Clock
- Single-step Operation
- Low-power RAM Retention Mode
- Power-on Reset Capability (with External Capacitor)
- Instruction Cycle: 1.25μs/12MHz (MBL8742H) and 2.5μs/6MHz (MBL8742N)
- Instruction Set: 93 Instructions with 217 Instruction Codes
- Single +5V Power Supply
- Operating Temperature Range: 0° C to 70° C

Pin Assignment



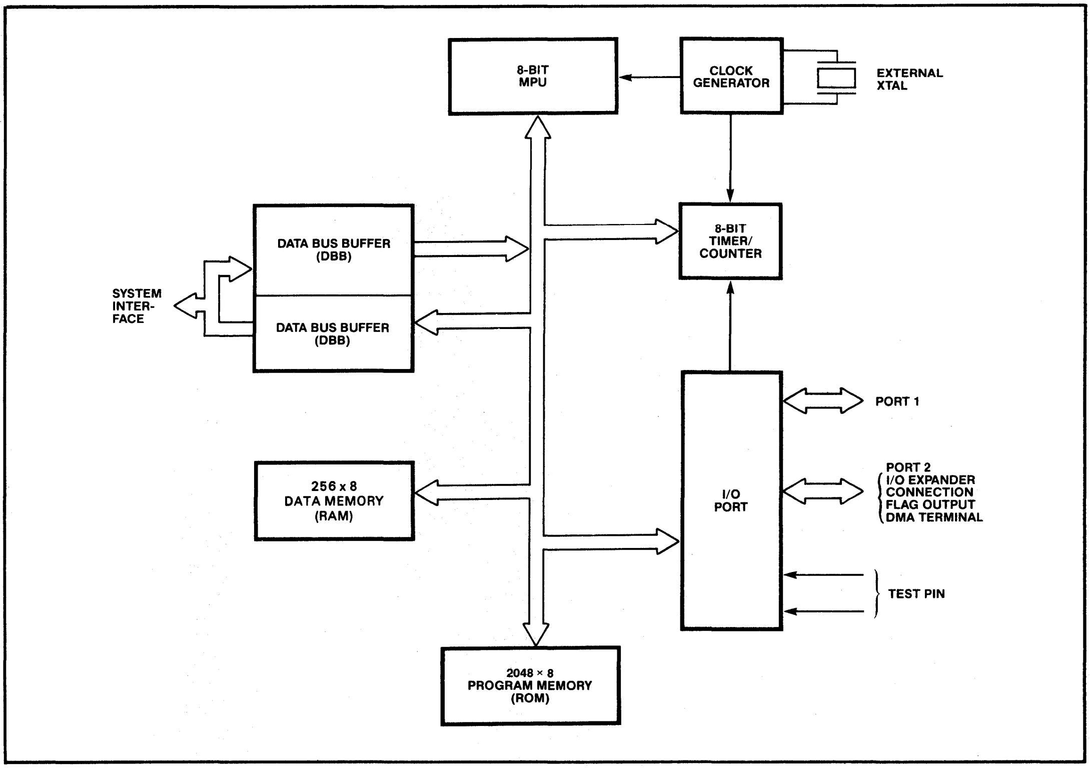
*These pins are internally pulled up.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES (Cont)

- N-channel Silicon-gate MOS Process
- Standard 40-pin Ceramic DIP (Suffix—C)
- Compatible with Intel 8742
- Replaceable with MBL8041A/42 and Intel 8041A/42

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Symbol	Function
40	V_{CC}	+5Vdc power supply input.
26	V_{DD}	+5Vdc power supply input for internal RAM. This pin is also used as the power supply input when programming the EPROM.
20	V_{SS}	Ground terminal.
1	T0	Input used for conditional branching.
39	T1	This pin performs the following functions: ● Event input pin for the event counter. ● Conditional input pin for conditional branch.

PIN DESCRIPTIONS (Cont)

Pin No.	Symbol	Function
2	XTAL 1	Input connection for external crystal. This pin can also be used as an input from an external clock source.
3	XTAL 2	Input connection for external crystal. (Note: The XTAL 1 and XTAL 2 input levels are not directly TTL compatible with a TTL clock source. An open-collector drive with an appropriate pullup is required to properly interface the two circuits.)
4	$\overline{\text{RESET}}$	Input that resets and initializes the MPU. (Note: This input level is not TTL compatible.)
5	$\overline{\text{SS}}$	Input used for single step operation.
6	$\overline{\text{CS}}$	Chip select input.
7	EA	Input used for controlling program memory access. Holding EA high forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.
8	$\overline{\text{RD}}$	Strobe that enables a read operation from data bus buffer or status register.
9	A0	Address input to determine whether read/write data or read/write commands. A0 = "L" indicates data read or write. A0 = "H" indicates status read or command write.
10	$\overline{\text{WR}}$	Strobe that enables a write operation to data bus buffer register.
11	SYNC	An output synchronized with the MBL8742 clock. This pin is used when a synchronization signal is required for external circuits.
12–19	D0–D7	8-bit bidirectional I/O port used to interface the MBL8742 to the master processor.
21–24	P20–P23	Lower 4 bits of the 8-bit quasi-bidirectional I/O port (Port 2). These pins function as an interface port with the I/O expander (MBL8243) when an expansion I/O is used to execute instructions. During single step operation the upper 3 bits of the program address are output on P20, P21, P22.
35–38	P24–P27	Upper 4 bits of the 8-bit quasi-bidirectional I/O port (Port 2). These function as the flag output pins (P24 and P25) and DMA pins (P26 and P27) according to the executed instruction. P24: OBF (Output Data Buffer Register Full) output P25: $\overline{\text{IBF}}$ (Input Data Buffer Register Full) output P26: DRQ (DMA Request) output P27: $\overline{\text{DACK}}$ (DMA Acknowledge) input
25	PROG	Strobe output signal when performing an expansion I/O instruction with an I/O expander such as the MBL8243. Used as a programming input when writing to the EPROM.
27–34	P10–P17	8-bit Quasi-bidirectional I/O ports (Port 1). During single step operation, the next program fetch address (Lower 8 bits) is output from these pins.

FUNCTIONAL DESCRIPTION

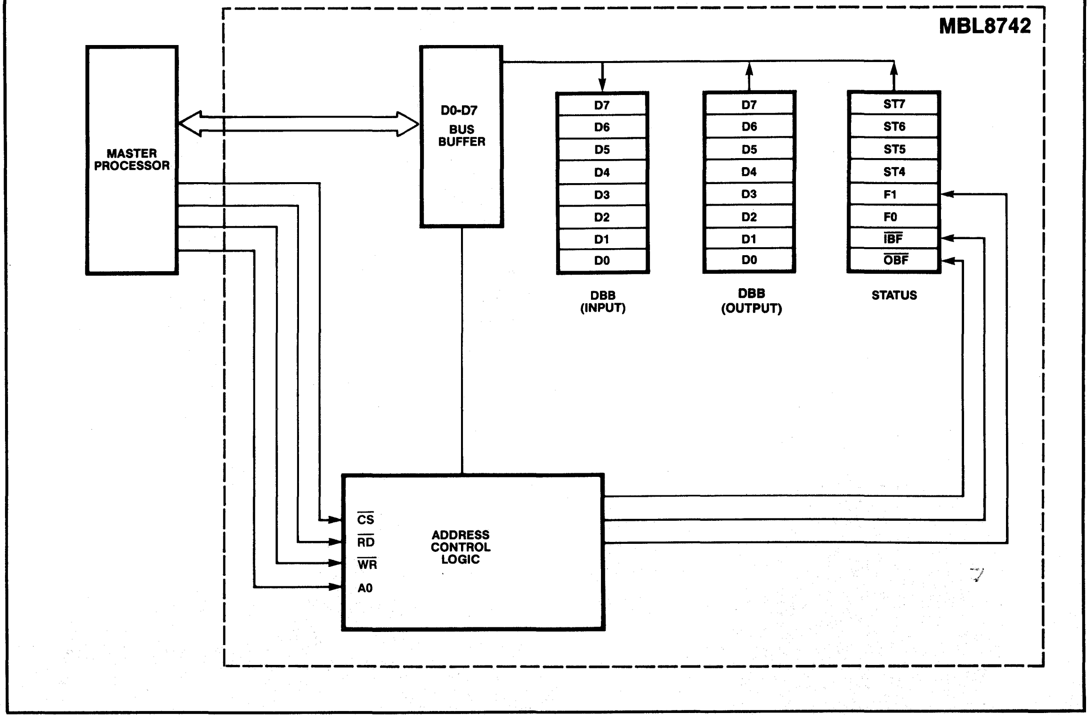
System Interface

The data, command, and status interface between the master processor and the MBL8742 is provided by two Data Bus Buffer(DBB) registers and a status register. Selection logic for these registers is shown in Table 1; a simplified interface is shown in Figure 1. Referring to the interface drawing, note that the master processor can read data from the output buffer register and write data into the input buffer register. When the MBL8742 executes an "OUT DBB, A" instruction, data is written into the DBB and the Output Buffer Full (OBF) flag is set. When data is read from the DBB by the master processor, OBF is reset. If the master processor writes into DBB, the Input Buffer Full ($\overline{\text{IBF}}$) flag is set and is reset when the MBDL8742 reads the data. Reading the status register is non-destructive and does not affect internal operation of the MBL8742.

Table 1. Selection Logic

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	AO	DESCRIPTION
0	0	1	0	Read DBB (Output) register.
0	0	1	1	Read STS (Output) register (Status)
0	1	0	0	Write DBB (Input) register (Data).
0	1	0	1	Write DBB (Input) register (Command).
1	x	x	x	Invalid.

Figure 1. Interface Between MBL8742 and Master Processor



Program Status Word (PSW)

As shown in the following diagram and associated text, the upper four bits of the PSW are used as flags to indicate MPU status. The lower three bits are used to select register pairs in the RAM stack when servicing a subroutine call or an interrupt. The flag bits (C, AC, F_0, and BS) are defined below; the stack pointer bits (SP_0 - SP_2) are defined in the next paragraph. The remaining bit in the PSW is unused.

7	6	5	4	3	2	1	0
C	AC	F_0	BS	1	SP_2	SP_1	SP_0
←——— Flags ———→				Unused Bit	←—Stack Pointer—→		

Flag Bits

C (Carry): When an accumulator overflow occurs during an ALU operation, this bit is set to '1'.

AC (Auxiliary Carry): When an accumulator overflow from bit 3 to bit 4 occurs during an addition, this bit is set to "1".

F_0 (User Flag): With the proper instruction, this flag can be user-designated; the F_0 flag can also be checked from the MPU as bit 2 of the Status Register.

BS (Bank Select): With the proper instruction, the BS flag indicates selection of a Register Bank. When set to "0", Register Bank 0 is selected; when set to "1", Register Bank 1 is selected. Refer to the RAM memory map that follows.

Stack Register (8-Level Capability)

The Stack Register has 16 bytes of memory area in the built-in RAM. The stack Register consists of eight levels, that is, a stack level consists of two bytes as shown in the following diagram.

	MSB	LSB	
SP-3			
SP-2	PC7–4	PC3–0	A set of 2 bytes
SP-1	PSW7-4	PC10-8	
SP			←This level will be used at the next sub-routine call or interrupt. Stack position SP = 00001 $SP_2SP_1SP_0$
SP+1			

↑
RAM
Address

SP (Stack Pointer): In the above figure, "SP" indicates an address of Stack Pointer to be used for the next sub-routine call or interrupt. "SP" is given as an 8-bit code from the lower three bits of Status Register as follows:

$SP = 00001\underbrace{SP_2SP_1SP_0}$
→ Status Register Bits 0 to 2.

PC_n (Program Counter): In the above figure, "PC_n" indicates the content of the n-th bit in the Program Counter.

RESIDENT DATA MEMORY MAP (RAM)

Address (Hex)		
0	R_0 Register 0	Register Bank 0
1	R_1 Register 1	
2	R_2 Register 2	
3	R_3 Register 3	
4	R_4 Register 4	
5	R_5 Register 5	
6	R_6 Register 6	
7	R_7 Register 7	
8	Stack Register (16 Bytes) (8 Level Stack)	Stack Register (16 Bytes) (8 Level Stack)
.		
.		
.	PC_L	
.	C AC F_0 BS PC_H	
.		
.		
.		
17		
18	R_0 Register 0	Register Bank 1
19	R_1 Register 1	
1A	R_2 Register 2	
1B	R_3 Register 3	
1C	R_4 Register 4	
1D	R_5 Register 5	
1E	R_6 Register 6	
1F	R_7 Register 7	
20	Working Area (224 Bytes)	
21		
22		
.		
.		
.		
FD		
FE		
FF		

Interrupt Processing

There are two types of interrupt: $\overline{\text{IBF}}$ interrupt and Timer/Counter interrupt. If an interrupt occurs when the system is in "interrupt enable" status, the interrupt flag is set as soon as the current instruction is completed and interrupt processing starts.

First, the upper four bits of the Status Word and content of the Program Counter are stored in the stack. The program then jumps to address "3" in the case of an $\overline{\text{IBF}}$ interrupt and address "7" in the case of a Timer/Counter interrupt.

After the interrupt has been processed by a user program and **a RETR (Return and Restore Status) instruction has been** executed, the Status Word and Program Counter contents stored in the stack are restored, the interrupt flag is reset, and the system is ready to accept the next interrupt request.

A Timer/Counter interrupt request occurs when the Timer/Counter overflow flag is set due to Timer/Counter overflow. However, since the Timer/Counter interrupt request is masked by the $\overline{\text{IBF}}$ interrupt request, an $\overline{\text{IBF}}$ interrupt has first priority.

The Timer/Counter interrupt is enabled after the $\overline{\text{IBF}}$ interrupt has been executed and the system is now ready to receive the next interrupt request. Operational and interrupt flowcharts are shown on the following page.

PROGRAMMING AND VERIFYING THE EPROM

The MBL8742 uses an internal 2K × 8 EPROM for program memory. A description of the pins used for programming and verifying operation of the EPROM are repeated here for user convenience. Procedural steps for programming and verification follow the pin functions.

Pin Descriptions

Symbol	Function
XTAL1 & XTAL2	Input clock signal (1-to-3MHz)
$\overline{\text{RESET}}$	Initializes internal registers. Input address data to the data bus is internally latched on the rising edge of $\overline{\text{RESET}}$.
T0	When T0 is Low, program mode is selected. When T0 is High, verify mode is selected.
EA	When 18-volts is applied to this pin, the program and verify modes are enabled.
Bus (D7-D0)	Lower 8-bits for address and data inputs in the program mode; data output in the verify mode.
P22–P20	Upper address inputs.
V_{DD}	+5-volt power supply.
PROG	Input programming pulses.
A0 & $\overline{\text{CS}}$	Clamp both of these inputs low.

Programming Procedures

Step 1: Initialize circuits as follows.

- Apply +5V to V_{CC}, V_{DD}, T0 and EA pins. Let Bus (D7–D0) and PROG pins float.
- Apply 0V to $\overline{\text{RESET}}$, A0, and $\overline{\text{CS}}$ pins.
- Use internal oscillator or an external source to generate a 1-to-3MHz clock.

Step 2: Select program mode by setting T0 to 0V.

Step 3: Set EA to 18V to enable program or verify mode.

Step 4: Input address as follows.

- Bus (D7–D0): 8 low-order bits
- P22 to P20: 3 high-order bits

Step 5: Set $\overline{\text{RESET}}$ to +5V to internally latch address inputs.

Step 6: Input write data to bus.

Step 7: Turn on programming power supply and set V_{DD} to 21-volts.

Step 8: Apply 0-volts to the PROG pin and then apply a programming pulse of 18-volts for 50-milliseconds. Again apply 0-volts to the pin and then let it float.

Step 9: Turn off programming power supply (V_{DD} from 21V to 5V) and let Bus (D7–D0) float.

Step 10: Select verify mode by setting T0 to 5V.

Step 11: Read and verify bus data. If data cannot be verified, repeat steps 2 through 10.

Step 12: Set $\overline{\text{RESET}}$ to 0V. If all desired addresses haven't been written yet, repeat steps 4 through 11.

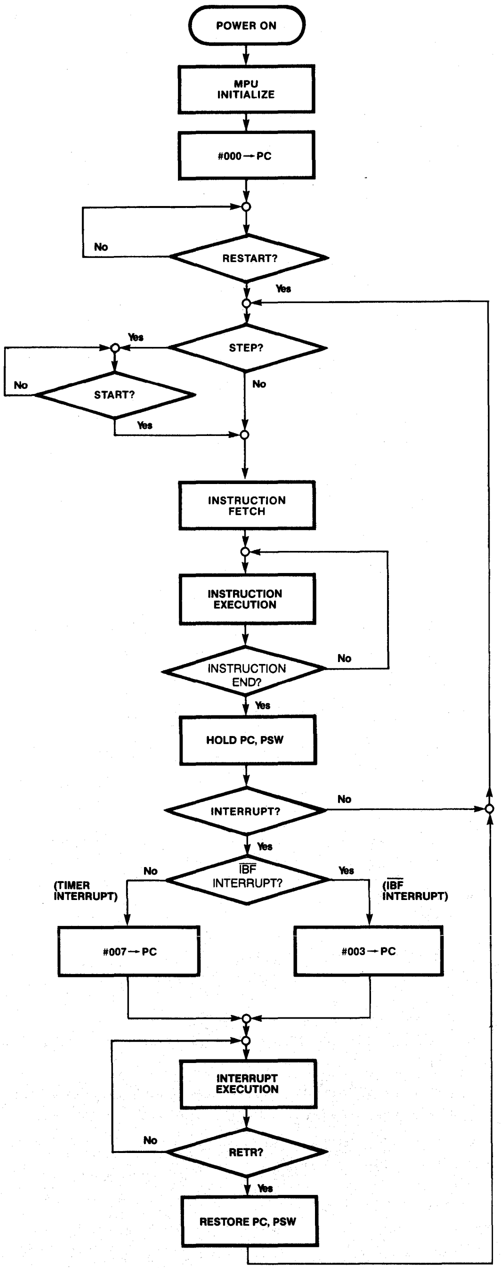
Step 13: Set EA to 5V to terminate programming procedure.

ERASING THE EPROM

Data written into the EPROM can be erased by applying ultraviolet light rays with a wavelength of 2537 angstroms. With UV light source directly above the transparent lid at a distance of 2-to-3 centimeters. The time for complete erasure is between 15-and-20 minutes for most commercial lamps. The recommended amount of UV radiation is 10Wsec/cm^2; the luminous intensity on the package surface is designed to be approximately 12000uW/cm^2.

If the package surface is soiled by grease, adhesives, or other light inhibitors, the erasing time will increase. Before attempting to erase data, it is recommended that surfaces be cleaned with alcohol or some other detergent that will not damage the package.

OPERATIONAL FLOWCHART



INTERRUPT FLOWCHART

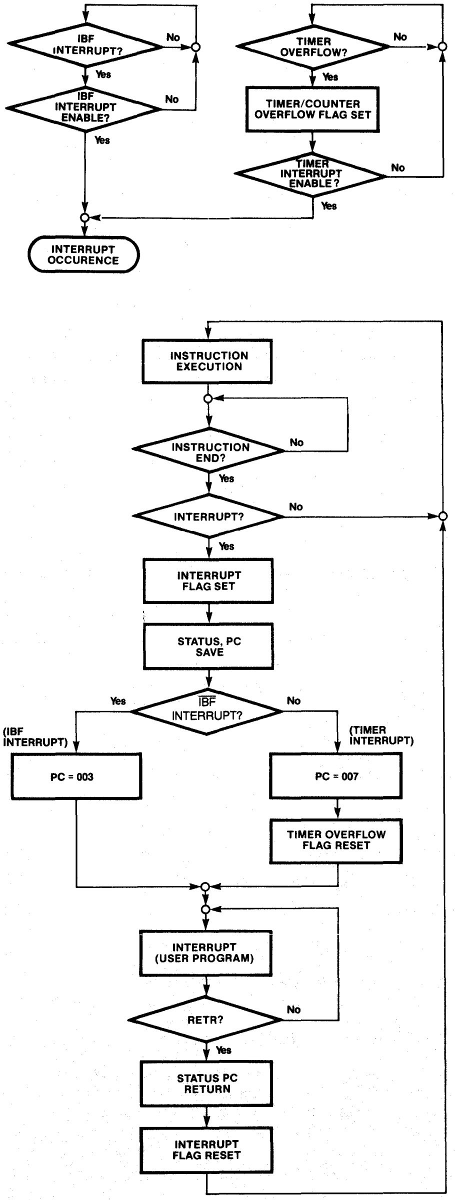
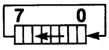
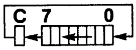
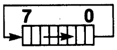
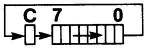


Table 2. Instruction Set Summary

ACCUMULATOR INSTRUCTIONS

Operation	Mnemonic	OP code	Byte	Cycle	Flag		Remarks
					C	AC	
Add register to A	ADD A, Rr	6X[3]	1	1	★[2]	★[2]	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	★[2]	★[2]	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	★[2]	★[2]	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	★[1]	★[2]	(A) ← (A) + data
Add register to A with Carry	ADDC A, Rr	7X[3]	1	1	★[1]	★[2]	(A) ← (A) + (Rr) + (C)
Add data memory to A with Carry	ADDC A, @R0	70	1	1	★[1]	★[2]	(A) ← (A) + ((R0)) + (C)
	ADDC A, @R1	71	1	1	★[1]	★[2]	(A) ← (A) + ((R1)) + (C)
Add immediate to A with Carry	ADDC A, #data	13	2	2	★[1]	★[2]	(A) ← (A) + data + (C)
AND register to A	ANL A, Rr	5X[3]	1	1	-	-	(A) ← (A) AND (Rr)
AND data memory to A	ANL A, @R0	50	1	1	-	-	(A) ← (A) AND ((R0))
	ANL A, @R1	51	1	1	-	-	(A) ← (A) AND ((R1))
AND immediate to A	ANL A, #data	53	2	2	-	-	(A) ← (A) AND data
OR register to A	ORL A, Rr	4X[3]	1	1	-	-	(A) ← (A) OR (Rr)
OR data memory to A	ORL A, @R0	40	1	1	-	-	(A) ← (A) OR ((R0))
	ORL A, @R1	41	1	1	-	-	(A) ← (A) OR ((R1))
OR immediate to A	ORL A, #data	43	2	2	-	-	(A) ← (A) OR data
Exclusive OR register to A	XRL A, Rr	DX[3]	1	1	-	-	(A) ← (A) XOR (Rr)
Exclusive OR data memory to A	XRL A, @R0	D0	1	1	-	-	(A) ← (A) XOR ((R0))
	XRL A, @R1	D1	1	1	-	-	(A) ← (A) XOR ((R1))
Exclusive OR immediate to A	XRL A, #data	D3	2	2	-	-	(A) ← (A) XOR data
Increment A	INC A	17	1	1	-	-	(A) ← (A) + 1
Decrement A	DEC A	07	1	1	-	-	(A) ← (A) – 1
Clear A	CLR A	27	1	1	-	-	(A) ← 0
Complement A	CPL A	37	1	1	-	-	(A) ← ($\overline{A}$)
Decimal Adjust A	DA A	57	1	1	★	-	Note 2
Swap digits of A	SWAP A	47	1	1	-	-	(A7-4) ⇄ (A3-0)
Rotate A Left	RL A	E7	1	1	-	-	
Rotate A Left through Carry	RLC A	F7	1	1	★[1]	-	
Rotate A Right	RR A	77	1	1	-	-	
Rotate A Right through Carry	RRC A	67	1	1	★[1]	-	

INPUT/OUTPUT INSTRUCTIONS

Operation	Mnemonic	OP code	Byte	Cycle	C	AC	Remarks
Input port to A	IN A, P1	09	1	2	-	-	(A) ← (P1)
	IN A, P2	0A	1	2	-	-	(A) ← (P2)
Output A to port	OUTL P1, A	39	1	2	-	-	(P1) ← (A)
	OUTL P2, A	3A	1	2	-	-	(P2) ← (A)
AND immediate to port	ANL P1, #data	99	2	2	-	-	(P1) ← (P1) AND data
	ANL P2, #data	9A	2	2	-	-	(P2) ← (P2) AND data
OR immediate to port	ORL P1, #data	89	2	2	-	-	(P1) ← (P1) OR data
	ORL P2, #data	8A	2	2	-	-	(P2) ← (P2) OR data
Input DBB to A, clear IBF	IN A, DBB	22	1	1	-	-	(A) ← (DBB), (IBF) ← 0
Output A to DBB, set OBF	OUT DBB, A	02	1	1	-	-	(DBB) ← (A), (OBF) ← 1
A7-4 to bits 7-4 of Status	MOV STS, A	90	1	1	-	-	(STS7-4) ← (A7-A4)

INPUT/OUTPUT INSTRUCTIONS (Continued)

Operation	Mnemonic	OP code	Byte	Cycle	Flag		Remarks
					C	AC	
Input Expander port to A	MOVD A, Pp	OX[4]	1	2	-	-	(A3-0) ← (Pp), (A7-4) ← 0
Output A to Expander port	MOVD Pp, A	3X[4]	1	2	-	-	(Pp) ← (A3-0)
AND A to Expander port	ANLD Pp, A	9X[4]	1	2	-	-	(Pp) ← (Pp) AND (A3-0)
OR A to Expander port	ORLD Pp, A	8X[4]	1	2	-	-	(Pp) ← (Pp) OR (A3-0)

DATA MOVE INSTRUCTIONS

Operation	Mnemonic	OP code	Byte	Cycle	C	AC	Remarks
Move register to A	MOV A, Rr	FX[3]	1	1	-	-	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	-	-	(A) ← ((R0))
	MOV A, @R1	F1	1	1	-	-	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	-	-	(A) ← data
Move A to register	MOV Rr, A	AX[3]	1	1	-	-	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	-	-	((R0)) ← (A)
	MOV @R1, A	A1	1	1	-	-	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX[3]	2	2	-	-	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	-	-	((R0)) ← data
	MOV @R1, #data	B1	2	2	-	-	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	-	-	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*[1]	*[1]	(PSW) ← (A)
Exchange A and register	XCH A, Rr	2X[3]	1	1	-	-	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	-	-	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	-	-	(A) ⇄ ((R1))
Exchange digit of A and data memory	XCHD A, @R0	30	1	1	-	-	(A3-0) ⇄ ((R0)3-0)
	XCHD A, @R1	31	1	1	-	-	(A3-0) ⇄ ((R1)3-0)
Move to A from current page	MOVP A, @A	A3	1	2	-	-	(A) ← ((A)) within page
Move to A from Page 3	MOVP3A, @A	E3	1	2	-	-	(A) ← ((A)) within page 3

TIMER/COUNTER INSTRUCTIONS

Operation	Mnemonic	OP code	Byte	Cycle	C	AC	Remarks
Read Timer/Counter	MOV A, T	42	1	1	-	-	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	-	-	(T) ← (A)
Start Timer	STRT T	55	1	1	-	-	
Start Counter	STRT CNT	45	1	1	-	-	
Stop Timer/Counter	STOP TCNT	65	1	1	-	-	
Enable Timer/Counter Interrupt	EN TCNTI	25	1	1	-	-	
Disable Timer/Counter Interrupt	DIS TCNTI	35	1	1	-	-	

CONTROL INSTRUCTIONS

Operation	Mnemonic	OP code	Byte	Cycle	C	AC	Remarks
Enable DMA Handshake Lines	EN DMA	E5	1	1	-	-	
Enable IBF Interrupt	EN I	05	1	1	-	-	
Disable IBF Interrupt	DIS I	15	1	1	-	-	
Enable Master Interrupts	EN FLAGS	F5	1	1	-	-	
Select register bank 0	SEL RB0	C5	1	1	-	-	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	-	-	(BS) ← 1
No Operation	NOP	00	1	1	-	-	

REGISTER INSTRUCTIONS

Operation	Mnemonic	OP code	Byte	Cycle	C	AC	Remarks
Increment register	INC Rr	1X[3]	1	1	-	-	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	-	-	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	-	-	((R1)) ← ((R1)) + 1
Decrement register	DEC Rr	CX[3]	1	1	-	-	(Rr) ← (Rr) - 1

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Remarks
SUBROUTINE INSTRUCTIONS							
Jump to Subroutine	CALL addr	%4[5]	2	2	-	-	Note 6
Return	RET	83	1	2	-	-	Note 7
Return and restore status	RETR	93	1	2	*[1]	*[1]	Note 8
FLAGS INSTRUCTIONS							
Clear Carry	CLR C	97	1	1	Z[1]	-	(C) ← 0
Complement Carry	CPL C	A7	1	1	CP[1]	-	(C) ← ($\overline{C}$)
Clear Flag 0	CLR F0	85	1	1	-	-	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	-	-	(F0) ← ($\overline{F0}$)
Clear Flag 1	CLR F1	A5	1	1	-	-	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	-	-	(F1) ← ($\overline{F1}$)
BRANCH INSTRUCTIONS							
Jump unconditional	JMP addr	%4[5]	2	2	-	-	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	-	-	Unconditional Branch (Note 9)
Decrement register and jump	DJNZ Rr, addr	EX[3]	2	2	-	-	(Rr) ≠ 0 (Note 10)
Jump on Carry = 1	JC addr	F6	2	2	-	-	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	-	-	(C) = 0
Jump on A Zero	JZ addr	C6	2	2	-	-	(A) = 0
Jump on A not Zero	JNZ addr	96	2	2	-	-	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	-	-	(T0) = H
Jump on T0 = 0	JNT0 addr	26	2	2	-	-	(T0) = L
Jump on T1 = 1	JT1 addr	56	2	2	-	-	(T1) = H
Jump on T1 = 0	JNT1 addr	46	2	2	-	-	(T1) = L
Jump on F0 = 1	JF0 addr	B6	2	2	-	-	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	-	-	(F1) = 1
Jump on Timer Flag = 1, Clear Flag	JTF addr	16	2	2	-	-	(TF) = 1
Jump on IBF Flag = 0	JNIBF addr	D6	2	2	-	-	(IBF) = 0
Jump on OBF Flag = 1	JOBF addr	86	2	2	-	-	(OBF) = 1
Jump on Accumulator Bit	JBb addr	%2[5]	2	2	-	-	(Ab) = 1

Notes:

1. Flag status
   * = Set or reset flag bit to the state it was in before instruction execution.
   Z = Reset flag bit.
   CP = Complement flag bit.
2. The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.
3. Refer to Table 3.
4. Refer to Table 4.
5. Refer to Table 5.
6. CALL addr
   ((SP)) ← (PC), (PSW7-4)
   (SP) ← (SP) + 1
   (PC10-8) ← A_H
   (PC7-0) ← A_L
7. RET
   (SP) ← (SP) - 1
   (PC) ← ((SP))
8. RETR
   (SP) ← (SP) - 1
   (PC) ← ((SP))
   (PSW7-4) ← ((SP))
9. JMPP @A
   (PC7-0) ← ((A))
10. DJNZ Rr, addr
    (Rr) ← (Rr) - 1
    if (Rr) ≠ 0 (PC7-0) ← addr
    if (Rr) = 0 Execute next instruction

Table 3. OP Code for Register Access

Mnemonic \ Rr	R0	R1	R2	R3	R4	R5	R6	R7
ADD A, Rr	68	69	6A	6B	6C	6D	6E	6F
ADDC A, Rr	78	79	7A	7B	7C	7D	7E	7F
ANL A, Rr	58	59	5A	5B	5C	5D	5E	5F
DEC Rr	C8	C9	CA	CB	CC	CD	CE	CF
DJNZ Rr, addr	E8	E9	EA	EB	EC	ED	EE	EF
INC Rr	18	19	1A	1B	1C	1D	1E	1F
MOV A, Rr	F8	F9	FA	FB	FC	FD	FE	FF
MOV Rr, A	A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data	B8	B9	BA	BB	BC	BD	BE	BF
ORL A, Rr	48	49	4A	4B	4C	4D	4E	4F
XCH A, Rr	28	29	2A	2B	2C	2D	2E	2F
XRL A, Rr	D8	D9	DA	DB	DC	DD	DE	DF

Bit	7	6	5	4	3	2	1	0
						r2	r1	r0

Table 4. OP Codes for Expander Port Access

Mnemonic \ Rr	P4	P5	P6	P7
ANLD Pp, A	9C	9D	9E	9F
MOVD A, Pp	0C	0D	0E	0F
MOVD Pp, A	3C	3D	3E	3F
ORLD Pp, A	8C	8D	8E	8F

Bit	7	6	5	4	3	2	1	0
							p1	p0

Table 5. OP Codes for JMP, CALL, and JBb

	First Byte									Second Byte								
	Bit	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0
JMP		A_H			0	0	1	0	0		A_L							
CALL		A_H			1	0	1	0	0		A_L							
JBb		B_b			1	0	0	1	0		A_L							

A_H = Address A_{10}, A_9, A_8 **A_L** = Address A_7 to A_0 **Bb** = b^{th} bit of accumulator

INSTRUCTION CODES

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUT DBB,A	◥ ADD A, #	◥ JMP 0 x x	EN I		DEC A		◤ IN A, P1	◤ IN A, P2		◤ MOVD A, P4	◤ MOVD A, P5	◤ MOVD A, P6	◤ MOVD A, P7
1	INC @R0	INC @R1	◥ JB0 addr	◥ ADDC A, #	◥ CALL 0 x x	DIS I	◥ JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A, @R0	XCH A, @R1	IN A, DBB	◥ MOV A, #	◥ JMP 1 x x	EN TCNTI	◥ JNT0 addr	CLR A	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
3	XCHD A, @R0	XCHD A, @R1	◥ JB1 addr		◥ CALL 1 x x	DIS TCNTI	◥ JT0 addr	CPL A		◤ OUTL P1, A	◤ OUTL P2, A		◤ MOVD P4, A	◤ MOVD P5, A	◤ MOVD P6, A	◤ MOVD P7, A
4	ORL A, @R0	ORL A, @R1	MOV A, T	◥ ORL A, #	◥ JMP 2 x x	STRT CNT	◥ JNT1 addr	SWAP A	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5	ANL A, @R0	ANL A, @R1	◥ JB2 addr	◥ ANL A, #	◥ CALL 2 x x	STRT T	◥ JT1 addr	DA A	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6	ADD A, @R0	ADD A, @R1	MOV T, A		◥ JMP 3 x x	STOP TCNT		RRC A	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
7	ADDC A, @R0	ADDC A, @R1	◥ JB3 addr		◥ CALL 3 x x		◥ JF1 addr	RR A	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
8				◤ RET	◥ JMP 4 x x	CLR F0	◥ JOBF addr			◥ ORL P1, #	◥ ORL P2, #		◤ ORLD P4, A	◤ ORLD P5, A	◤ ORLD P6, A	◤ ORLD P7, A
9	MOV STS, A		◥ JB4 addr	◤ RETR	◥ CALL 4xx	CPL F0	◥ JNZ addr	CLR C		◥ ANL P1, #	◥ ANL P2, #		◤ ANLD P4, A	◤ ANLD P5, A	◤ ANLD P6, A	◤ ANLD P7, A
A	MOV @R0, A	MOV @R1, A		◤ MOVP A, @A	◥ JMP 5 x x	CLR F1		CPL C	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A
B	◥ MOV @R0, #	◥ MOV @R1, #	◥ JB5 addr	◤ JMPP @A	◥ CALL 5 x x	CPL F1	◥ JF0 addr		◥ MOV R0, #	◥ MOV R1, #	◥ MOV R2, #	◥ MOV R3, #	◥ MOV R4, #	◥ MOV R5, #	◥ MOV R6, #	◥ MOV R7, #
C					◥ JMP 6 x x	SEL RB0	◥ JZ addr	MOV A, PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A, @R0	XRL A, @R1	◥ JB6 addr	◥ XRL A, #	◥ CALL 6 x x	SEL RB1	◥ JNIBF addr	MOV PSW, A	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
E				◤ MOVP3 A.@A	◥ JMP 7 x x	EN DMA	◥ JNC addr	RL A	◥ DJNZ R0, addr	◥ DJNZ R1, addr	◥ DJNZ R2, addr	◥ DJNZ R3, addr	◥ DJNZ R4, addr	◥ DJNZ R5, addr	◥ DJNZ R6, addr	◥ DJNZ R7, addr
F	MOV A, @R0	MOV A, @R1	◥ JB7 addr		◥ CALL 7xx	EN FLAGS	◥ JC addr	RLC A	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7

Legend:

#	= Immediate data
□	= 1 Byte, 1 Cycle Instruction
◤	= 1 Byte, 2 Cycle Instruction
◥	= 2 Byte, 2 Cycle Instruction

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Ambient Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

Note:
Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}, V_{DD}	4.5	5.0	5.5	V
	V_{SS}		0		V
Operating Temperature	T_A	0		+70	°C

DC Characteristics

T_A = 0°C to +70°C, $V_{CC} = V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$

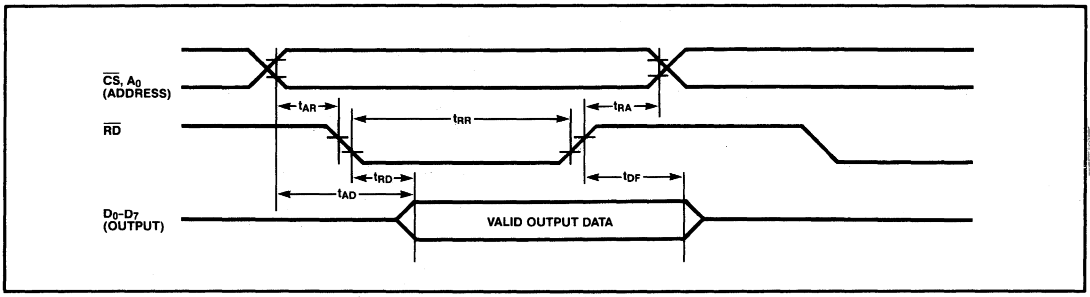
Parameter		Symbol	Test Conditions	Value		Unit
				Min	Max	
V_{DD} Supply Current		I_{DD}			20	mA
Supply Current		$I_{CC} + I_{DD}$			150	mA
Input Low Voltage	All except XTAL1, 2, $\overline{RESET}$	V_{IL}		-0.3	0.8	V
	XTAL1, 2, $\overline{RESET}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All except XTAL1, 2, $\overline{RESET}$	V_{IH}		2.0	V_{CC}	V
	XTAL1, 2, $\overline{RESET}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	D_0 to D_7	V_{OL}	I_{OL} = 2.0mA		0.45	V
	P10 to P17, P20 to P27, SYNC	V_{OL1}	I_{OL} = 1.6mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
Output High Voltage	D_0 to D_7	V_{OH}	$I_{OH} = -400\mu A$	2.4		V
	All other outputs	V_{OH1}	$I_{OH} = -50\mu A$	2.4		V
Input Leakage Current	T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, EA	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$		±10	μA
Output Leakage Current	D_0 to D_7 (High-impedance)	I_{OL}	$V_{SS} + 0.45V \leq V_{IN} \leq V_{CC}$		±10	μA
Input Low Current	P10 to P17; P20 to P27	I_{LI}	V_{IL} = 0.8V		0.5	mA
	$\overline{RESET}$, $\overline{SS}$	I_{LI1}	V_{IL} = 0.8V		0.2	mA

AC Characteristics (DBB Read Operation)

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Value		Unit
				Min	Max	
$\overline{\text{CS}}$, A0 Setup Time (to $\overline{\text{RD}}$ ↓)		t_{AR}		0		ns
$\overline{\text{CS}}$, A0 Hold Time (to $\overline{\text{RD}}$ ↑)		t_{RA}		0		ns
$\overline{\text{RD}}$ Pulse Width		t_{RR}		160		ns
Data Delay Time (from $\overline{\text{CS}}$, A0)		t_{AD}	C_L = 150pF		130	ns
Data Delay Time (from $\overline{\text{RD}}$ ↓)		t_{RD}	C_L = 150pF		130	ns
Data Floating Time (from $\overline{\text{RD}}$ ↑)		t_{DF}			85	ns
Cycle Time	MBL8742N	t_{CY}	6MHz (N-version)	2.5	15.0	μs
	MBL8742H		12MHz (H-version)	1.25	15.0	μs

Timing Diagram for Data Bus Buffer (DBB) Read Operation:

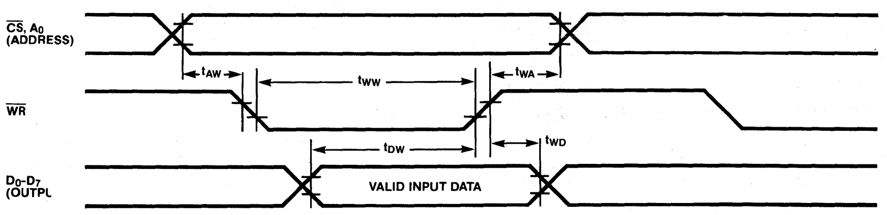


AC Characteristics (DBB Write Operation)

(T_A = 0°C to +70°C, $V_{CC} = V_{DD}$ = 5.0V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Value		Unit
			Min	Max	
$\overline{CS}$, A0 Setup Time (to $\overline{WR}$ ↓)	t_{AW}		0		ns
$\overline{CS}$, A0 Hold Time (from $\overline{WR}$ ↑)	t_{WA}		0		ns
$\overline{WR}$ Pulse Width	t_{WW}		160		ns
Data Setup Time (to $\overline{WR}$ ↑)	t_{DW}		130		ns
Data Hold Time (from $\overline{WR}$ ↑)	t_{WD}		0		ns

Timing Diagram for Data Bus Buffer (DBB) Write Operation:

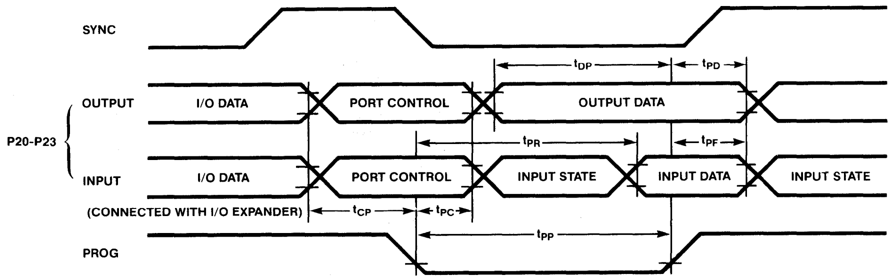


AC Characteristics (Operation with I/O Expander)

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter	Symbol	MBL8742N		MBL8742H		Unit
		Min	Max	Min	Max	
Port Control Setup Time (to PROG ↓)	t_{CP}	100		110		ns
Port Control Hold Time (from PROG ↓)	t_{PC}	60		100		ns
Input Data Delay Time (from PROG ↓)	t_{PR}		650		810	ns
Input Data Hold Time (from PROG ↑)	t_{PF}	0	150	0	150	ns
Output Data Setup Time (to PROG ↑)	t_{DP}	200		250		ns
Output Data Hold Time (from PROG ↑)	t_{PD}	20		65		ns
PROG Pulse Width	t_{PP}	700		1200		ns

Timing Diagram for Port 2 (lower 4 bits) Operation in Connection With I/O Expander:

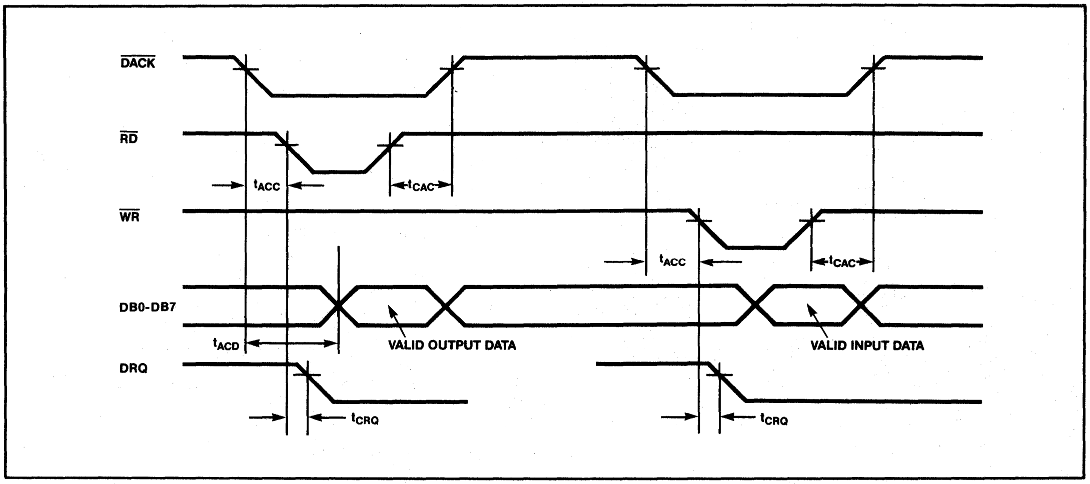


AC Characteristics (DMA Operation)

(T_A = 0°C to +70°C, $V_{CC} = V_{DD}$ = 5.0V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Value		Unit
			Min	Max	
$\overline{DACK}$ Setup Time (to $\overline{RD}$↓, $\overline{WR}$↓)	t_{ACC}		0		ns
$\overline{DACK}$ Hold Time (from $\overline{RD}$↑, $\overline{WR}$↑)	t_{CAC}		0		ns
Input Data Delay Time (from $\overline{DACK}$↓)	t_{ACD}	C_L = 150pF		130	ns
DRQ Clear Time (from $\overline{RD}$↓, $\overline{WR}$↓)	t_{CRQ}			100	ns

Timing Diagram for DMA Operation:



TEST CONDITIONS

V_{IL} = 0.8V (All except XTAL1, 2, $\overline{RESET}$)
= 0.6V (XTAL1, 2, $\overline{RESET}$)

V_{IH} = 2.0V (All except XTAL1, 2, $\overline{RESET}$)
= 3.8V (XTAL1, 2, $\overline{RESET}$)

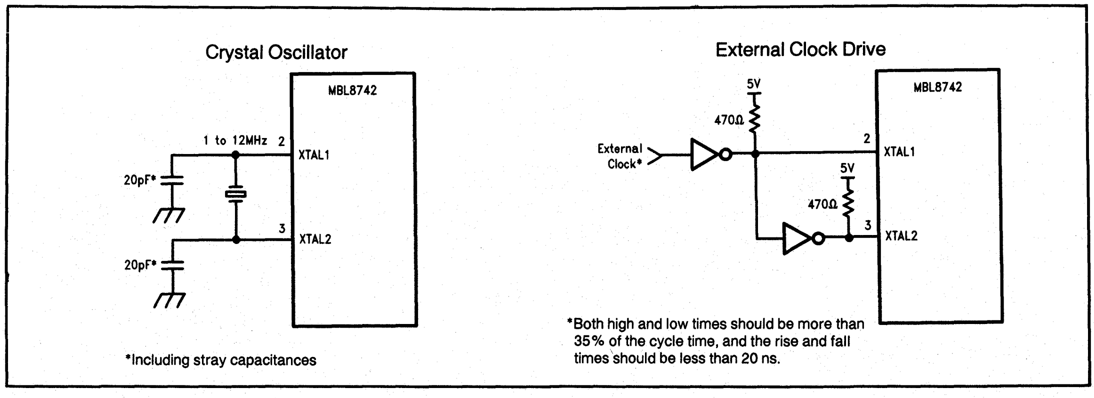
V_{OL} = 0.45V

V_{OH} = 2.4V

OUTPUT LOAD

D0 to D7: C_L = 150pF
All other outputs: C_L = 80pF

Oscillation Circuits



*Including stray capacitances

*Both high and low times should be more than 35% of the cycle time, and the rise and fall times should be less than 20 ns.

ELECTRICAL CHARACTERISTICS FOR PROGRAMMING

DC Characteristics[1,2]

(T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21 ±0.5V or 5V ±5%)

Parameter	Symbol	Value		Unit
		Min	Max	
V_{DD} Program Voltage High Level	V_{DDH}	20.5	21.5	V
V_{DD} Program Voltage Low Level	V_{DDL}	4.75	5.25	
PROG Program Voltage High Level	V_{PH}	17.5	18.5	V
PROG Program Voltage Low Level	V_{PL}	—	0.2	
EA Program/Verify Voltage High Level	V_{EAH}	17.5	18.5	V
EA Program/Verify Voltage Low Level	V_{EAL}	—	5.25	
V_{DD} High Voltage Supply Current	I_{DD}	—	30.0	mA
PROG High Voltage Supply Current	I_{PROG}	—	16.0	
EA High Voltage Supply Current	I_{EA}	—	1.0	

Notes:

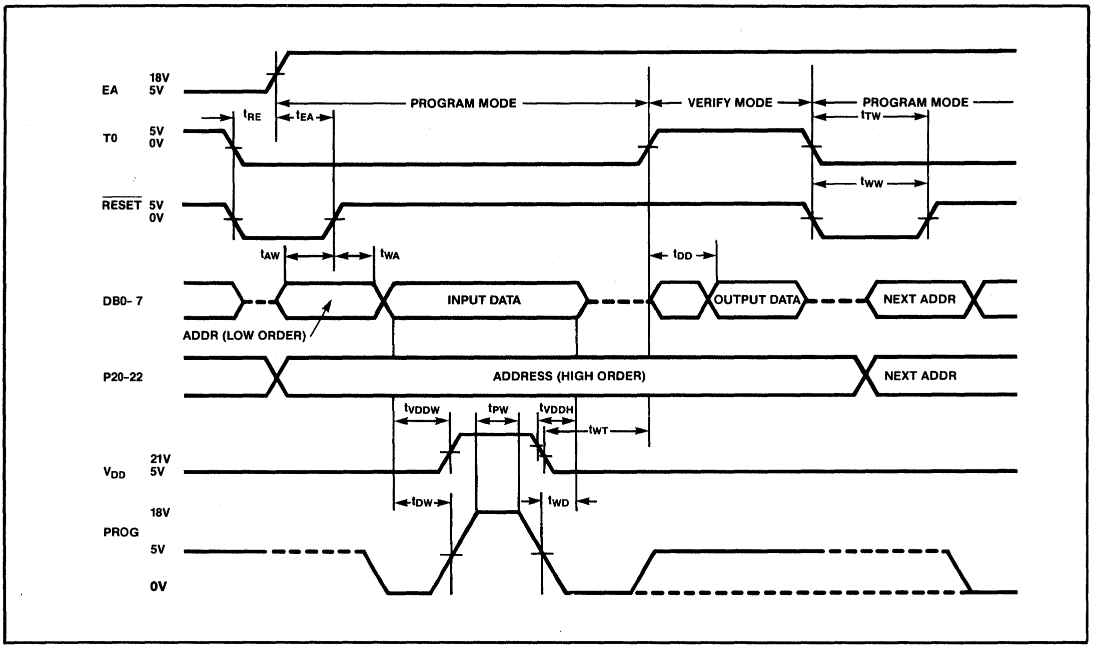
1. High Level Voltage (V_{DDH}, V_{PH}) should not be applied to V_{DD} and PROG pins unless V_{CC} = 5V ±5% and EA = 18V ±0.5V.
2. V_{DD}, PROG, and EA should not exceed the above specified range, including overshoot and undershoot.

AC Characteristics

(T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21 ±1.0V or 5V ±5%)

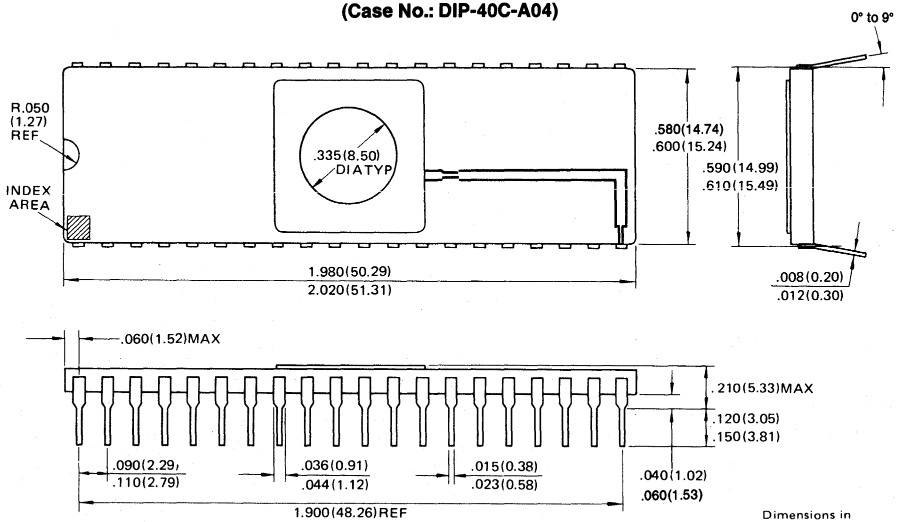
Parameter	Symbol	Value		Unit
		Min	Max	
Address setup time (before $\overline{\text{RESET}}$ ↑)	t_{AW}	$4 \cdot t_{CY}$	—	
Address hold time (after $\overline{\text{RESET}}$ ↑)	t_{WA}	$4 \cdot t_{CY}$	—	
Input data setup time (before $\overline{\text{PROG}}$ ↑)	t_{DW}	$4 \cdot t_{CY}$	—	
Input data hold time (after $\overline{\text{PROG}}$ ↓)	t_{WD}	$4 \cdot t_{CY}$	—	
$\overline{\text{RESET}}$ hold time (after EA ↓)	t_{PH}	$4 \cdot t_{CY}$	—	
V_{DD} setup time (before PROG ↑)	t_{VDDW}	$4 \cdot t_{CY}$	—	
V_{DD} hold time (before PROG ↓)	t_{VDDH}	0	—	
Program pulse width	t_{PW}	50	60	ms
TO setup time (before RESET ↑)	t_{TW}	$4 \cdot t_{CY}$	—	
TO hold time (after V_{DD} ↓)	t_{WT}	$4 \cdot t_{CY}$	—	
Data output delay time (after TO ↑)	t_{DO}	—	$4 \cdot t_{CY}$	
RESET pulse width (to Latch Address)	t_{WW}	$4 \cdot t_{CY}$	—	
V_{DD} and PROG rise/fall time	tr/tf	0.5	2.0	μs
MPU cycle time	t_{CY}	5.0	—	μs
$\overline{\text{RESET}}$ setup time (before EA ↑)	t_{RE}	$4 \cdot t_{CY}$	—	
EA setup time (before $\overline{\text{RESET}}$ ↑)	t_{EA}	10	—	ms

Timing Diagram for Programming/Verify Mode:



PACKAGE DIMENSIONS

40-Lead Ceramic (Metal Seal)
Dual In-Line Package
(Case No.: DIP-40C-A04)



Dimensions in
inches (millimeters)

Advanced Products **FUJITSU**

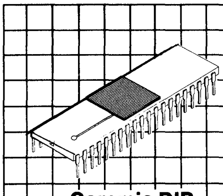
■ MB8868A
MOS Universal Asynchronous Receiver/Transmitter (UART)

October 1986
Edition 2.0

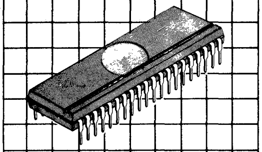
Description

The Fujitsu MB8868/A is a programmable Universal Asynchronous Receiver/Transmitter (UART), fabricated with an N-channel silicon gate MOS technology. All control pins, input pins and output pins are TTL compatible. The UART interfaces asynchronous serial data channels from terminals or other peripherals to the parallel data of a microprocessor, computer, or other terminal. Parallel data is converted by the transmitter section of the UART into a serial word consisting of the data as well as start, parity, and stop bit(s). Serial data is converted by the receiver section of the UART into parallel data. The receiver section verifies correct code transmission by parity checking and active reception of a valid stop bit. The UART can be programmed to accept word lengths of 5, 6, 7, or 8 bits. Even or odd parity can be set. Parity generation and checking can be inhibited.

One, one and one-half, or two stop bits can be set when transmitting a 5-bit code.



Ceramic DIP
DIP-40C-A01

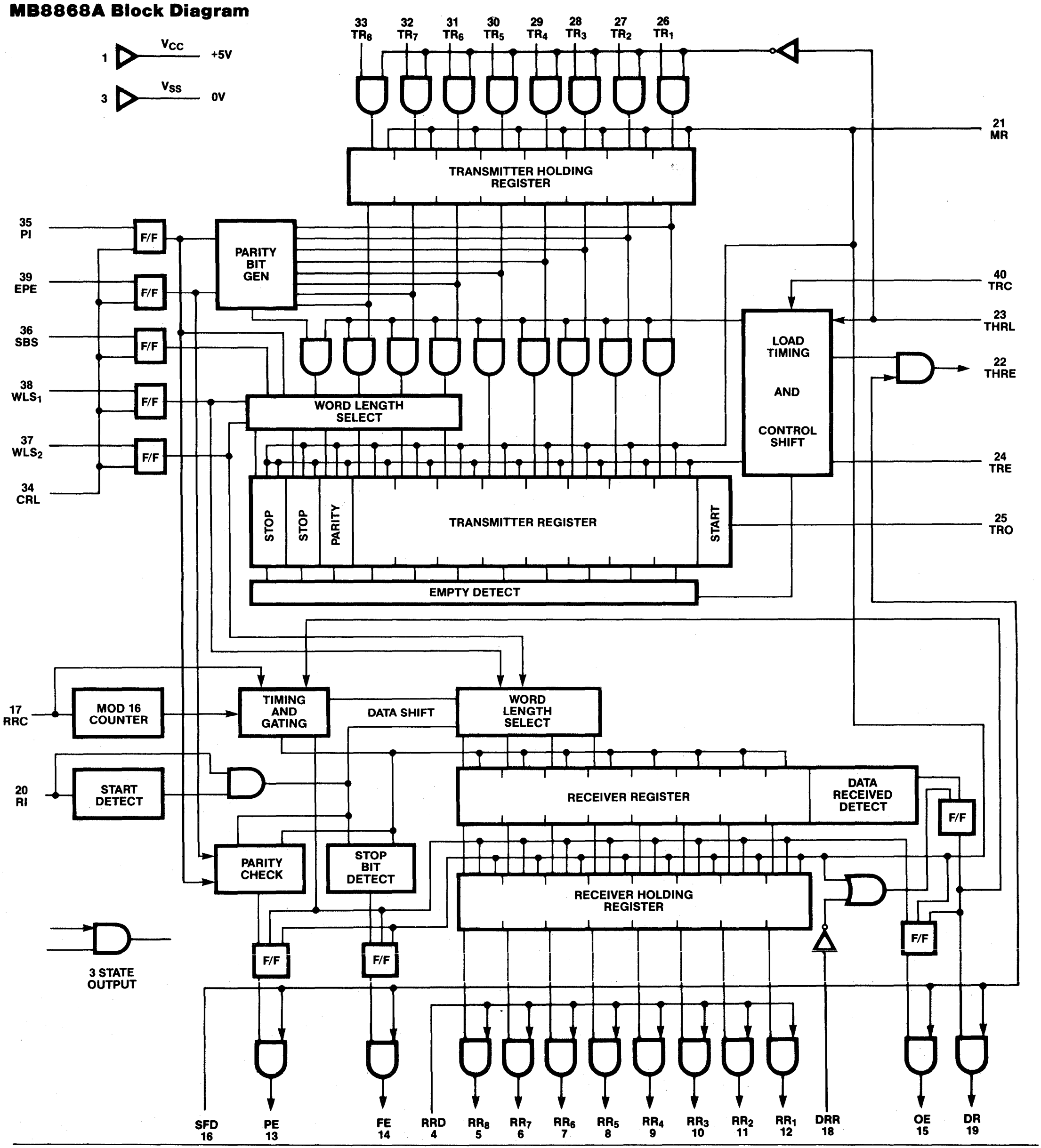


Plastic DIP
DIP-40P-M01

Features

- **Full or Half Duplex Operation**
- **Completely Programmable**
- **Start Bit Generated Automatically**
- **Data and Clock Synchronization Performed Automatically**
- **Data Received/Transmitted Status Automatically Generated**
- **Complete Static Circuity**
- **TTL Compatible I/O**
- **Three-State Output Capability**
- **Single Power Supply: +5V**
- **Standard 40-Pin Dual In-Line Package**
- **Functionally Compatible with Western Digital TR1863 and AMI S1602**

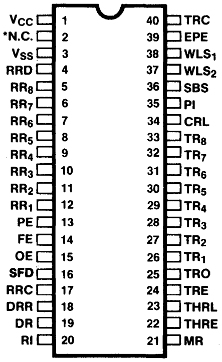
MB8868A Block Diagram



Capacitance
(T_A = 25° C, f = 1MHz, V_{IN} = 0V)

		Value		
Parameter	**Symbol**	**Typ.**	**Max.**	**Unit**
Input Capacitance for all inputs	C_{IN}	10	—	pF

Pin Assignment



* N.C. (no connection)

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to V_{SS} Pin	V_{CC}	-0.3 to +7.0	V_{DC}
Input Voltage	V_{IN}	-0.3 to +7.0	V_{DC}
Output Voltage	V_O	-0.3 to +7.0	V_{DC}
Operating Temperature	T_{OP}	0 to +70	°C
Storate Temperature	T_{stg}	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This** device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid applications of any voltages higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions

(Referenced to V_{SS})

		Value				
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Operating Temperature**
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	O°C to +70°C
	V_{SS}	0.0	0.0	0.0	V	
Logic Input High Voltage	V_{IH}	2.2	—	V_{CC}	V	
Logic Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	

DC Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Units
Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 5.25V)	I_{LI}	—	—	350	μA
Output Leakage Current for 3-State (V_{OUT} = 0V to V_{CC}, SFD = RRD = V_{IH})	I_{LZ}	-20	—	+20	μA
Output Low Voltage (I_{OL} = 1.8mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OL} = -200μA)	V_{OH}	2.4	—	—	V
V_{CC} Supply Current	I_{CC}	—	70	—	mA

AC Characteristics

(Recommended operating ranges unless otherwise noted)

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Units
Clock Frequency for RRC and TRC (Duty Cycle = 50%)	f_C	DC	—	800	kHz
CRL Pulse Width, High	t_{PWC}	200	—	—	ns
THRL Pulse Width, Low	t_{PWT}	180	—	—	ns
DRR Pulse Width, Low	t_{PWR}	180	—	—	ns
MR Pulse Width, High	t_{PWM}	150	—	—	ns
Coincidence Time (Fig. 4 and Fig. 8)	t_C	180	—	—	ns
Hold Time (Fig. 4 and Fig. 8)	t_H	20	—	—	ns
Setup Time (Fig. 4 and Fig. 8)	t_{SET}	0	—	—	ns
Propagation Delay Time, High to Low, Output (C_L = 130 pF + 1 TTL)	t_{pd0}	—	—	350	ns
Propagation Delay Time, Low to High, Output (C_L = 130 pF + 1 TTL)	t_{pd1}	—	—	350	ns

Pin Descriptions

Pin Name	Pin Number	Description
RRD	4	**Receiver Register Disconnect** A high logic level, V_{IH}, on this pin disconnects the Receiver Holding Register outputs from the data outputs RR_8-RR_1 on pins 5-12.
RR_8 thru RR_1	5, 6, 7, 8, 9, 10, 11, 12	**Receiver Holding Register Data** These are the parallel outputs from the Receiver Holding Register if the RRD input is an input low level, V_{IL}. Data is right justified for character formats of less than eight bits, with RR_1 being the least significant bit. Unused MSB's are forced to a low logic output level, V_{OL}.
PE	13	**Parity Error** This output pin goes to a high level, V_{OH}, if the received parity does not agree with that programmed by the Even Parity Enable input (pin 39). With each character transferred to the Receiver Holding Register, this output is updated. The status Flag Disconnect input (pin 16) allows additional PE lines to be tied together by providing an output disconnect capability.

Pin Descriptions
(Continued)

Pin Name	Pin Number	Description
FE	14	**Framing Error** This output pin goes to a high level, V_{OH}, if the received character has no valid Stop bit. With each character transferred to the Receiver Holding Register, this output is updated. The Status Flag Disconnect input (pin 16) allows additional FE lines to be tied together by providing an output disconnect capability.
OE	15	**Overrun Error** This output pin goes to a high level, V_{OH}, if the Data Received Flag (pin 19) is not reset before the next character is transferred to the Receiver Holding Register. The Status Flag Disconnect input (pin 16) allows additional OE lines to be tied together by providing an output disconnect capability.
SFD	16	**Status Flag Disconnect** When this input goes to a high level, V_{IH}, PEE, FE, OE, DR, and THRE outputs are disconnected allowing bus sharing capability.
RRC	17	**Receiver Register Clock** This clock input is sixteen times the desired receiver shift rate.
DRR	18	**Data Received Reset (DRR)** A low level input, V_{IL}, resets the data Received (DR) line.
DR	19	**Data Received** This output goes to a high level, V_{OH}, when an entire character has been received and transferred to the Receiver Holding Register.
RI	20	**Receiver Input** Serial input data enters on this line. It is transferred to the Receiver Register as determined by the character length, parity, and number of Stop bits. When data is not being received, this input must be at high level, V_{IH}
MR	21	**Master Reset** A high level pulse, V_{IH}, on this input will clear the internal logic. The Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, and DRR are reset. In addition, the serial output line is set to a high level, V_{OH}.
THRE	22	**Transmitter Holding Register Empty** This output goes to a high level, V_{OH}, when the Transmitter Holding Register has completed transfer of its contents to the Transmitter Register. The high level indicates that a new character may be loaded into the transmitter Holding Register.
THRL	23	**Transmitter Holding Register Load** When a low level, V_{IL}, is applied to this input, a character is loaded into the Transmitter Holding Register. This character is transferred to the Transmitter Register on a low to high level transition, as long as the Transmitter Register is not currently in the process of transmitting a character. If a character is being transmitted, the transfer from the Transmitter Holding Register is delayed until character transmission has been completed. Then, the new character is transferred simultaneously with the start of the serial transmission of the new character.
TRE	24	**Transmitter Register Empty** This output is at a high level , V_{OH}, when the Transmitter Register has completed the serial transmission of a full character including the required number of Stop bits. A high level will be maintained until the start of transmission of the next character.

Pin Descriptions
(Continued)

Pin Name	Pin Number	Description
TRO	25	**Transmitter Register Output** This output line transmits the Transmitter Register contents [Start bit, Data bits, Parity bit, and Stop bit(s)] serially. This output remains at a high level, V_{OH}, when no data is being transmitted. Therefore, the start of transmission is determined by the transition of the Start bit from a high level to a low level voltage, V_{OL}.
TR_1 thru TR_8	26, 27, 28, 29, 30, 31, 32, 33	**Transmitter Register Data Inputs** The THRL strobe loads each character on these lines into the Transmitter Holding Register. If WLS_1 and WLS_2 have selected a character of less than 8 bits, the character is then right-justified to the least significant bit, TR_1, with the excess bits not used. A high input level, V_{IH}, will cause a high output level, V_{OH}, to be transmitted.
CRL	34	**Control Register Load** When this input is at a high level, V_{IH}, the control bits (WLS_1, WLS_2, EPE, PI, SBS), are loaded into the Control Register. This input may be either strobed or hard wired to a high level.
PI	35	**Parity Inhibit** When this input is at a high level, V_{IH}, parity generation and verification circuitry are inhibited and the PE output will be held to a low level, V_{OL}. In the inhibit condition, the Stop bit(s) will follow the last data bit on transmission.
SBS	36	**Stop Bit(s) Select** A high level, V_{IH}, on this input will select two Stop bits, and a low level, V_{IL}, will select one Stop bit. If 5-bit long words are selected, a high level, V_{IH}, will generate one and one-half Stop bits.
WLS_1, WLS_2, EPE, TRC		**Word Length Select (WLS_1, WLS_2)** The state of these two inputs determines the character length (exclusive of parity) as follows:

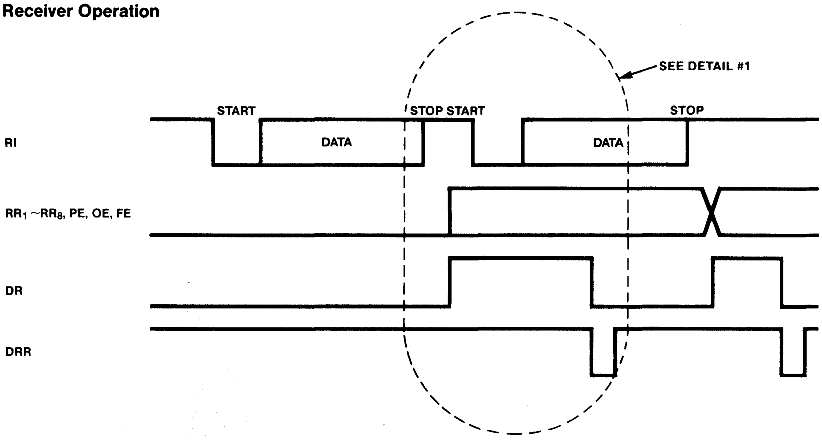
WLS_2	WLS_1	Word Length
V_{IH}	V_{IH}	8 bits
V_{IH}	V_{IL}	7 bits
V_{IL}	V_{IH}	6 bits
V_{IL}	V_{IL}	5 bits

Even Parity Enable (EPE)
A high level, V_{IH}, on this input will select even Parity, while a low level, V_{IL}, selects odd Parity.

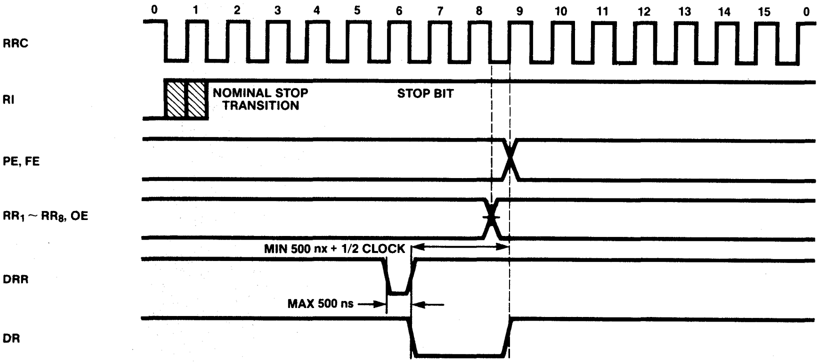
Transmitter Register Clock (TRC)
The frequency of this clock is 16 times the desired transmitter shift rate.

Timing Diagrams

Receiver Operation

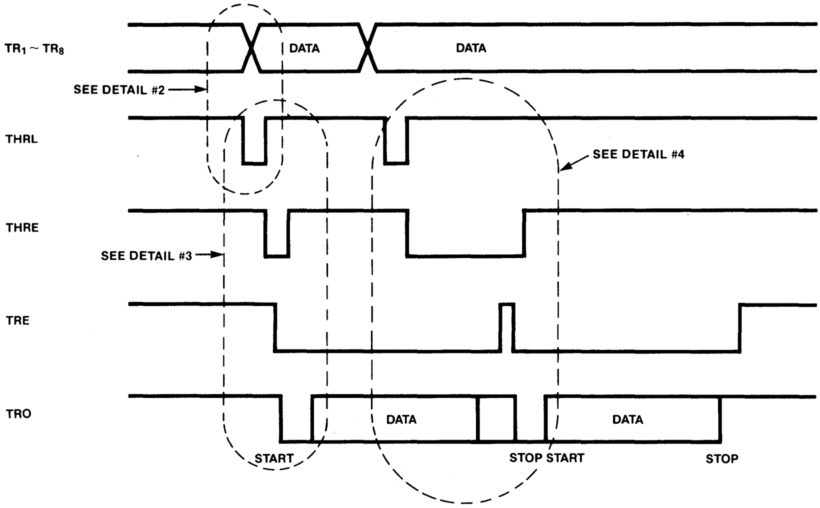


Timing for Status Flag, RR_1, thru RR_8 and DR (Detail #1)

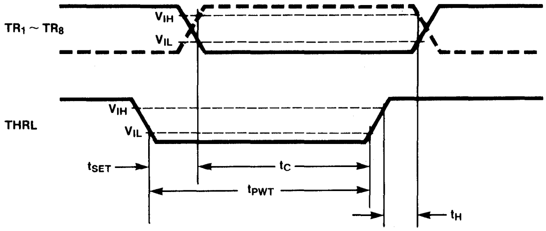


Timing Diagrams
(Continued)

Transmitter Operation

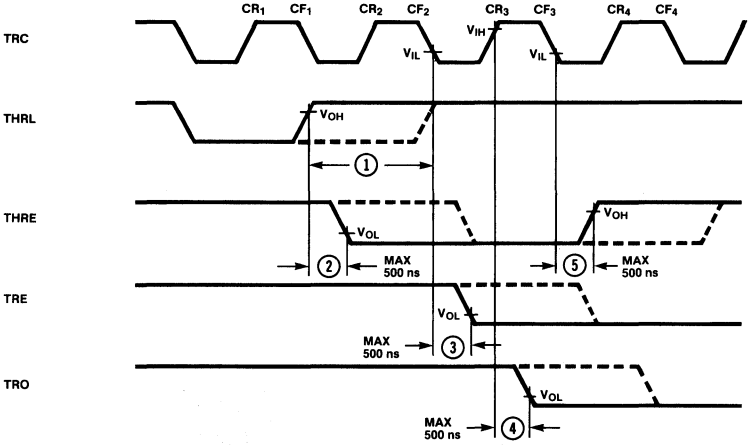


Data Input Load Cycle (Detail #2)



Timing Diagrams
(Continued)

Transmitter Output Timing (1) (Detail #3)



Notes:

① When the positive transition of THRL is ≥ 500 ns before the falling edge of TRC (CF2 in the figure), then TRE is enabled at CF2. But when 500 ns >①> 0 ns, then TRE is invalid between CF2 and CF3.

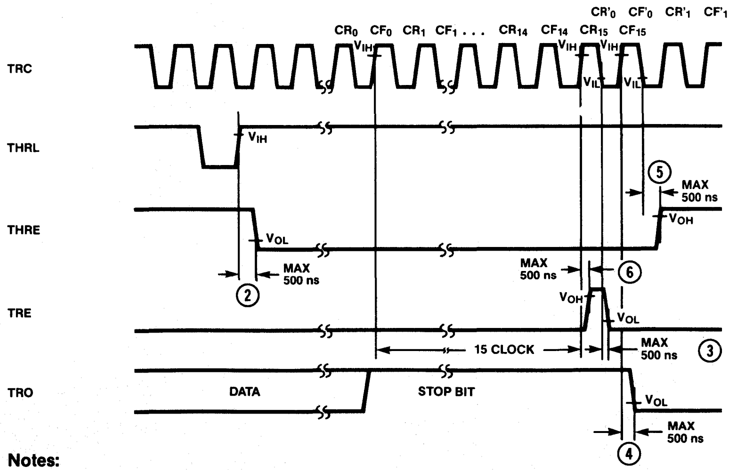
② THRE goes low during 500 ns Max. from the postive transition of THRL.

③ TRE goes low during 500 ns Max. from the first falling edge of TRC after THRE goes low with TRE high.

④ TRO goes low (START BIT) during 500 ns Max. from the first rising edge of TRC after TRE goes low.

⑤ THRE goes high during 500 ns Max. from the falling edge of TRC after Start bit is enabled.

Transmitter Output Timing (2) (Detail #4)



Notes:

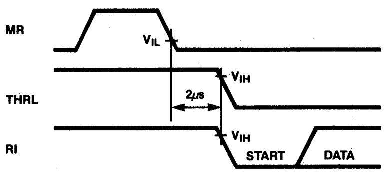
② ~ ⑤ Refer to Notes in Detail #3

⑥ TRE goes high during 500 ns Max. from the 15th rising edge of TRC after Stop bit is enabled.

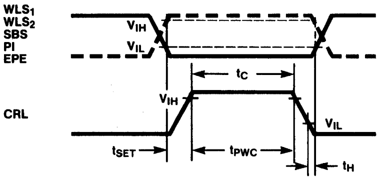
Timing Diagrams
(Continued)

Other Timing Diagrams

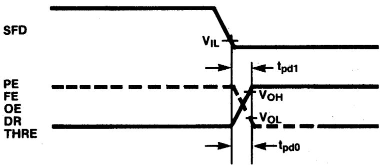
Input After Master Reset



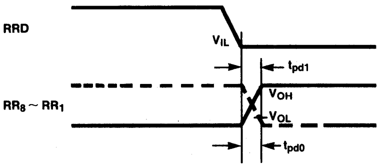
Control Register Load Cycle



Status Flag Output

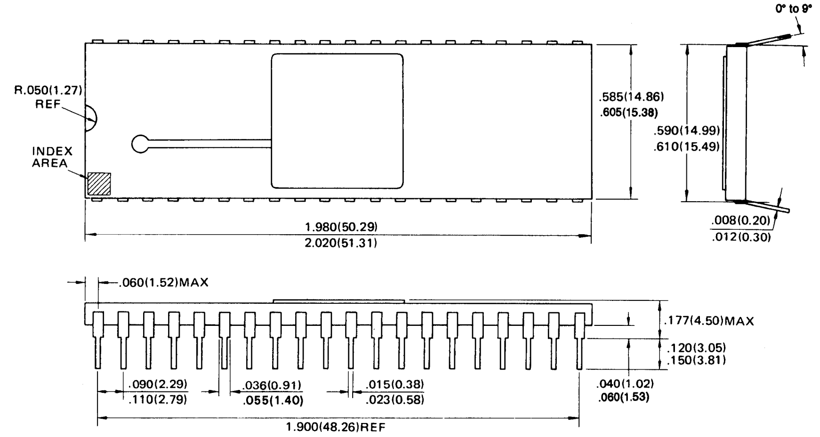


Data Output

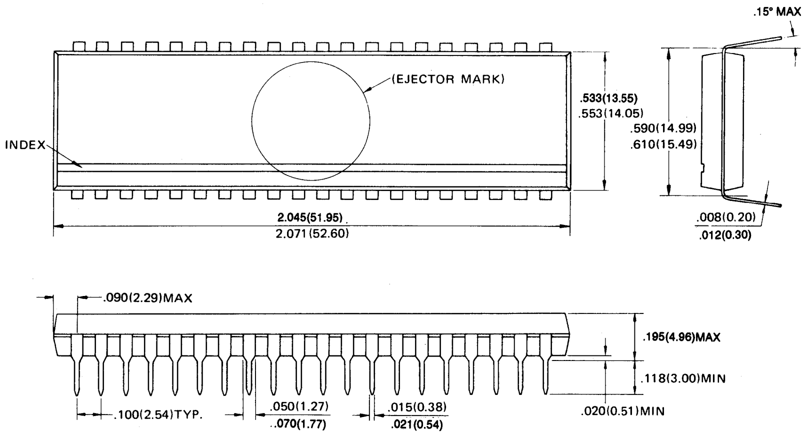


Package Dimensions
(Dimensions in
millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package DIP-40C-A01



40-Lead Plastic Dual In-Line Package DIP-40P-M01



FUJITSU

TTL TWO-PHASE CLOCK GENERATOR AND DRIVER

MB 8867
MB 8867E

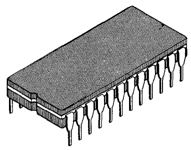
October 1982
Edition 2.0

TWO-PHASE MICROPROCESSOR CLOCK

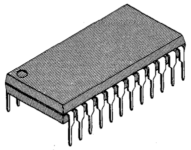
The Fujitsu MB 8867 is an advanced Microprocessor Clock Generator/Driver LSI manufactured with Fujitsu's bipolar TTL process. The circuit generates non-overlapping two-phase clock signals for the Fujitsu MBL 6800 microprocessor unit or similiar single +5 volt MPU's. Additionally, two-phase TTL clock signals synchronized with the MPU clock are provided, as well as an MPU data strobe, reset/clock controls for the memory interrupt, and an automatic power-up reset. With the MB 8867, the entire MPU timing system can be designed with one chip and a minimum of external components.

A built-in oscillator permits external timing control by a crystal; or RC network timing can be utilised for less critical applications. In the former, the internal frequency divider is rate selectable, so that the output frequency is either 1/4 or 1/16 of the source frequency.

Driver circuits are included on the MB 8867 which eliminates the need for external buffer gates and reduces system package count. Output drivers are short - circuit protected.

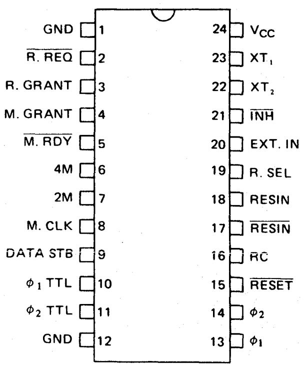


CERAMIC PACKAGE
DIP-24C-C01



PLASTIC PACKAGE
DIP-24P-M01

PIN ASSIGNMENT



- Single chip two-phase clock generator with on-chip drivers
- Short-circuit protected outputs
- Complete MPU system timing network including dynamic memory refresh
- Single +5V power supply
- Low power consumption: 450 mW typ.
- Reliable TTL process
- Two-phase TTL clock signals
- Data strobe for memory control synchronization
- Automatic power-up and manual reset
- Clock controls for memory interrupt
- Crystal or RC network frequency source
- Selectable source frequency options
- Works with high speed microprocessors
- Standard 24 pin package
- Minimum external components required

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	+7 Max.	V
Input Voltage	V_{IN}	-0.5 to +5.5	V
Output Voltage	V_O	-0.5 to +5.5	V
Operating Temperature	T_{OP}	-25 to +125	°C
Storage Temperature	T_{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

FUJITSU **MB 8867**
MB 8867E

INTRODUCTION

The MB 8867 provides the two-phase clock signal input for the MBL 6800 microprocessor or any similiar timing signal required in a microcomputer system. The IC incorporates the necessary logic to ensure that these clock signals (ϕ_1 and ϕ_2) are non-overlapping; and, additionally, the MB 8867 is designed to accomodate direct connection to high capacitive loads (typically 170 pF) without additional buffering.

Most high speed microprocessor controlled systems utilize dynamic random access memories in order to minimize system cost and power consumption. A major design problem in such systems is to provide dynamic RAM refresh timing signals synchronized with the operation of the MPU. The MB 8867 solves this problem with its refresh control pins, $\overline{\text{R. REQ}}$ and R. GRANT (Refresh Request and Refresh Grant).

In the pin description below, all TTL compatible inputs and outputs are indicated by "TTL input" or "TTL output" and later refered to in the characteristic tables by these terms.

DESCRIPTION OF PINS

XT_1, XT_2
Two pins are provided for the connection of an external crystal. The crystal selected should be either four or sixteen times the desired output clock frequency. Small picofarad capacitors are provided internally in the oscillator circuitry. However, for fine oscillation control, an additional small capacitor (3 pf to 10 pf) in series with the crystal may be used.

EXT. IN (TTL input)
This input is used for an external RC network to provide timing control when a crystal is not utilized. Note that, like the crystal source, the input frequency will be either four or sixteen times the desired output clock frequency. See the APPLICATIONS INFORMATION section of this data sheet for proper external component connection.

M. CLK (TTL output)
Provides a reference clock driver for external memory synchronous with ϕ_2. The frequency is identical to the output clock frequency (ϕ_1, ϕ_2), but is not affected by switching $\overline{\text{R. REQ}}$ (refresh cycle).

2M, 4M (TTL outputs)
2M and 4M are pulse train drivers with frequencies of two times and four times the output clock (ϕ_1, ϕ_2) frequency, respectively. When R. SEL is low, EXT. IN and 4M are in opposite phase. Therefore, ring oscillation can be generated without an external crystal by inserting an appropriate RC network between 4M and EXT. IN. See the APPLICATIONS INFORMATION section of this data sheet for circuit information.

RC
Provides automatic power-up reset function by utilizing an external RC network. $\overline{\text{RESET}}$ goes low with the rising edge of ϕ_1 when RC is less than 0.8V; $\overline{\text{RESET}}$ goes high when RC is greater than 2/3 V_{CC}. Therefore, automatic power-up reset is obtained by providing a delay slower than the rise time of V_{CC}.

$\overline{\text{INH}}$ (TTL input)
Used to control internal oscillation. The oscillator is operational when $\overline{\text{INH}}$ is brought high (open); the oscillator is inhibited when $\overline{\text{INH}}$ is brought low.

R. SEL (TTL input)
When R. SEL is high (open), the one-by-four frequency divider is operational; when R. SEL is low, the divider is bypassed. As an example, a 16MHz external time source will generate a 1MHz output clock frequency if R. SEL is high.

ϕ_1, ϕ_2
MPU output clock drivers. ϕ_1 and ϕ_2 have non-overlapping control.

ϕ_1 TTL, ϕ_2 TTL (TTL outputs)
TTL level output clock drivers synchronized with ϕ_1 and ϕ_2, respectively.

DATA STB (TTL output)
Data strobe signal for memory read and write operations. DATA STB goes high one cycle of the 4M output frequency after ϕ_2 goes high; DATA STB goes low just before ϕ_2 goes low. If $\overline{\text{M. RDY}}$ is not interrupted, DATA STB will maintain its high state during the last quarter cycle of ϕ_2.

RESIN, $\overline{\text{RESIN}}$ (TTL outputs)
Provides manual input reset. After reset, RESIN is brought low and $\overline{\text{RESIN}}$ is open. Manual reset occurs when these states are reversed. An internal flip-flop prevents switch-on chattering.

4

$\overline{\text{RESET}}$ (TTL output open-collector)
Open-collector output pin to provide the reset function.

$\overline{\text{R. REQ}}$, (TTL input) **R. GRANT** (TTL output)
These pins provide memory refresh control. $\overline{\text{R. REQ}}$ is usually kept high. To start the refresh cycle, $\overline{\text{R. REQ}}$ is brought low, and then R. GRANT goes high at the next falling edge of the memory clock. Then $\overline{\text{R. REQ}}$ is brought high, and R. GRANT will go low at the next falling edge of the memory clock. ϕ_1 will stay high and ϕ_2 will stay low during refresh. R. GRANT may be connected to the three state control of the MPU system to provide refresh for dynamic memories and DMA (Direct Memory Access) in the "cycle steal" mode.

$\overline{\text{M. RDY}}$, (TTL input) **M. GRANT** (TTL output)
Provided for low speed memory control. $\overline{\text{M. RDY}}$ is usually kept high. When $\overline{\text{M. RDY}}$ is brought low, M. GRANT goes low on the next falling edge of 4M. The high state of ϕ_2 is extended for the period that M. GRANT is low. At the same

time, the high state of M.CLK and DATA STB are maintained. This permits a long time period for memory read operations.

Vcc

Connected to the +5V supply. By-pass capacitors are recommended if the supply rail is long in order to reduce supply impedance.

GND 1, GND 2

Two ground terminals are provided in order to reduce internal impedance paths.

Fig. 1—MB 8867 BLOCK DIAGRAM

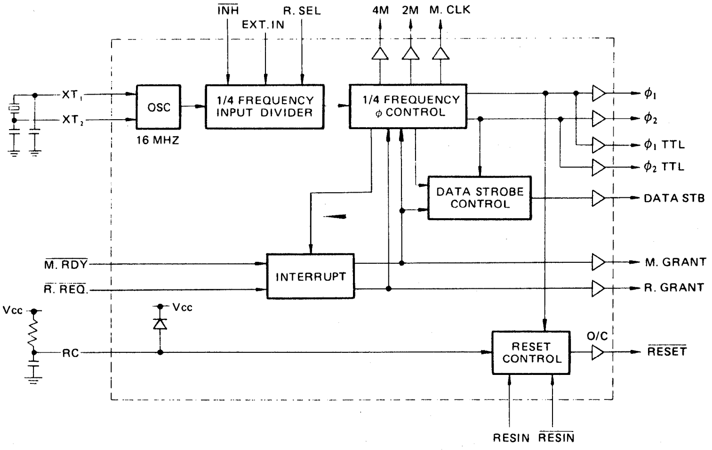
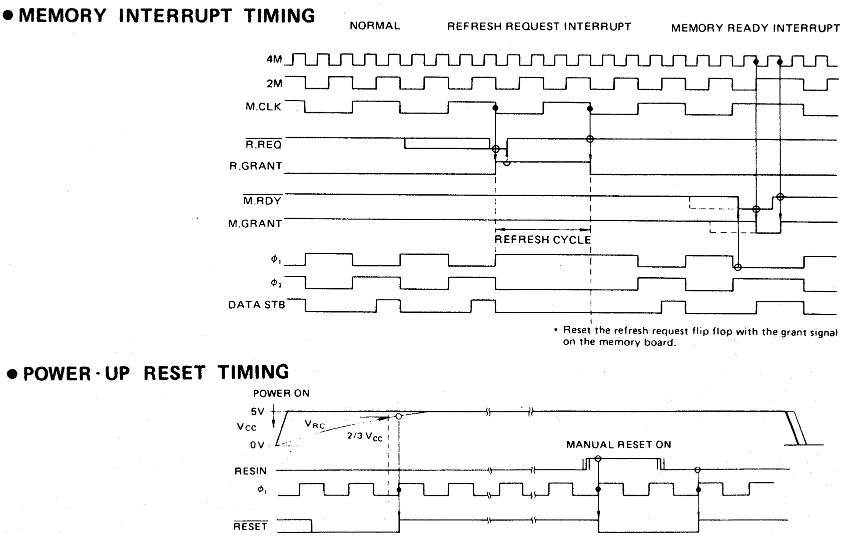


Fig. 2—SYSTEM TIMING DIAGRAM



GUARANTEED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit	Operating Temperature
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
Input High Voltage (TTL inputs)	V_{IHT}	2			V	
Input High Voltage (RC)	V_{IHR}	4.5			V	

DC CHARACTERISTICS *

(Full Guaranteed Operating Ranges unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Output High Voltage					
ϕ_1, ϕ_2 (I_{OH}=-0.2mA, V_{CC}=5.25V)	V_{OH}	4.95			V
TTL outputs except $\overline{\text{RESET}}$ (I_{OH}=-0.4mA, V_{CC}=4.75V)		2.4			V
Output Low Voltage					
ϕ_1, ϕ_2 (I_{OL}=1.8mA, V_{CC}=4.75V)	V_{OL}			0.3	V
TTL inputs (I_{OL}=16mA, V_{CC}=4.75V)				0.4	V
Input Clamp Diode Voltage TTL inputs (I_{IC}=-12mA, V_{CC}=4.75V)	V_{IC}			1.5	V
Input High Current					
EXT IN (V_{CC}=5.25V, V_{IN}=2.4V)	I_{IH}			40	μA
$\overline{\text{R.REQ}}$, $\overline{\text{M.RDY}}$, RESIN $\overline{\text{RESIN}}$, R.SEL, $\overline{\text{INH}}$ (V_{CC}=4.75V, V_{IN}=2.4V)		-100			μA
RC (V_{CC}=5.25V, V_{IN}=5.25V)				10	μA
Input Low Current					
EXT IN (V_{CC}=5.25V, V_{IN}=0.4V)	I_{IL}			-1.6	mA
$\overline{\text{R.REQ}}$, $\overline{\text{M.RDY}}$, RESIN, $\overline{\text{RESIN}}$ (V_{CC}=5.25V, V_{IN}=0.4V)				-3.2	mA
R.SEL, $\overline{\text{INH}}$ (V_{CC}=5.25V, V_{IN}=0.4V)				-4.8	mA
Power Supply Current					
(V_{CC}=4.75V, XT_2=0V)	I_{CC}	60			mA
(V_{CC}=5.25V, XT_2=0V)				160	mA
Output High Current $\overline{\text{RESET}}$ (V_{CC}=4.5V, V_{OH}=5.5V)	I_{OH}			250	μA
Output Short Circuit Current					
ϕ_1, ϕ_2 (V_{OL}=0V, V_{CC}=5.25V)	I_{OS}	-33		-100	mA
TTL inputs except $\overline{\text{RESET}}$ (V_{OL}=0V, V_{CC}=5.25V)		-18		-55	mA

* Unused terminals are left open.

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges unless otherwise noted.)

Parameter		Symbol	Value			Unit	Remarks
			Min.	Typ.	Max.		
Cycle Time	MB 8867	T_C	0.5		10	μs	Fig. 3 Fig. 4
	MB 8867E		0.666				
ϕ_1 Pulse Width (ϕ_1)	MB 8867	$PW\phi_1$	$\frac{Tc}{2}-70$			ns	Fig. 3
	MB 8867E		$\frac{Tc}{2}-100$				
ϕ_2 Pulse Width (ϕ_2)	MB 8867	$PW\phi_2$	$\frac{Tc}{2}-50$			ns	Fig. 4
	MB 8867E		$\frac{Tc}{2}-100$				
Rise Time (ϕ_1, ϕ_2)		$t_{r\phi}$		20	40	ns	Fig. 3
Fall Time (ϕ_1, ϕ_2)		$t_{f\phi}$		15	30	ns	Fig. 4
ϕ_1 to ϕ_2 Delay Time (ϕ_1, ϕ_2)		td_1	5	20	30	ns	Fig. 3
ϕ_2 to ϕ_1 Delay Time (ϕ_1, ϕ_2)		td_2	5	20	30	ns	Fig. 4
Pulse Width ($\overline{\text{M.RDY}}$=$\overline{\text{INH}}$=R.SEL=HIGH)	(4M)	PW_4	$\frac{Tc}{8}-30$	$\frac{Tc}{8}$		ns	Fig. 3 Fig. 5
	(2M)	PW_2	$\frac{Tc}{4}-30$	$\frac{Tc}{4}$		ns	
	(M.CLK)	PW_M	$\frac{Tc}{2}-30$	$\frac{Tc}{2}$		ns	Fig. 3 Fig. 6
	(DATA STB)	PW_D	$\frac{Tc}{4}-30$	$\frac{Tc}{4}$		ns	
4M to M.GRANT Delay Time		t_{4G}			50	ns	Fig. 3
4M to M.CLK Delay Time		t_{4MC}		15	30	ns	Fig. 5
M.CLK to ϕ_1 Delay Time		t_{M_1}	5	20	60	ns	Fig. 3 Fig. 6
M.CLK to ϕ_2 Delay Time		t_{M_2}	15	40	80	ns	
M.CLK to DATA STB Delay Time		t_{MD}	$\frac{Tc}{4}-30$		$\frac{Tc}{4}+15$	ns	
$\overline{\text{M.CLK}}$ to R.GRANT Delay Time		t_{MG}			50	ns	
$\overline{\text{M.RDY}}$ Enable Time		t_{EM}	50			ns	Fig. 3
$\overline{\text{M.RDY}}$ Disable Time		t_{DM}	50			ns	Fig. 5
$\overline{\text{R.REQ}}$ Enable Time		t_{ER}	50			ns	Fig. 3
$\overline{\text{R.REQ}}$ Disable Time		t_{DR}	50			ns	Fig. 6

Fig. 3—AC TEST CONDITIONS

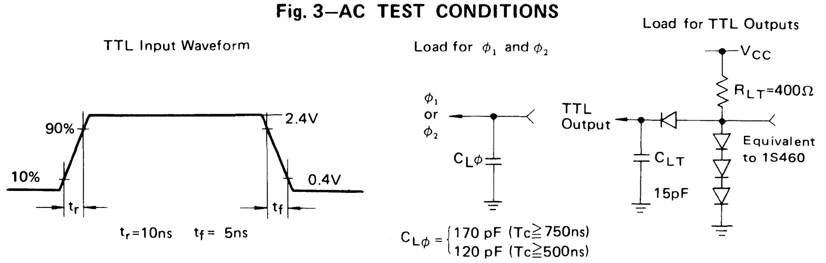


Fig. 4—TIMING DIAGRAM (1)

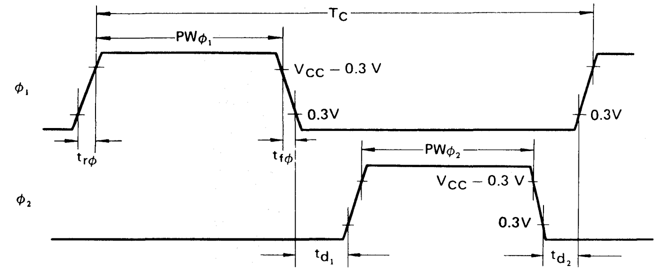


Fig. 5—TIMING DIAGRAM (2)

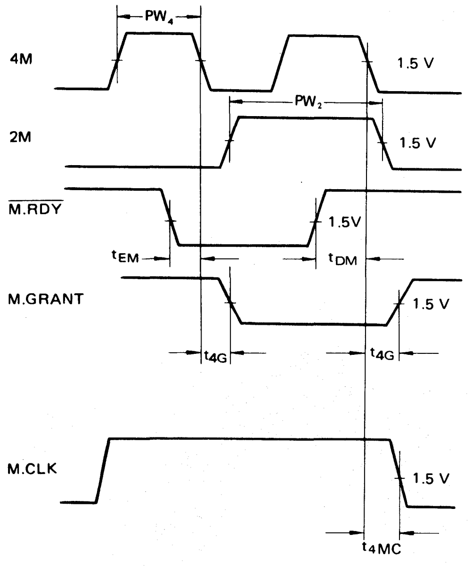
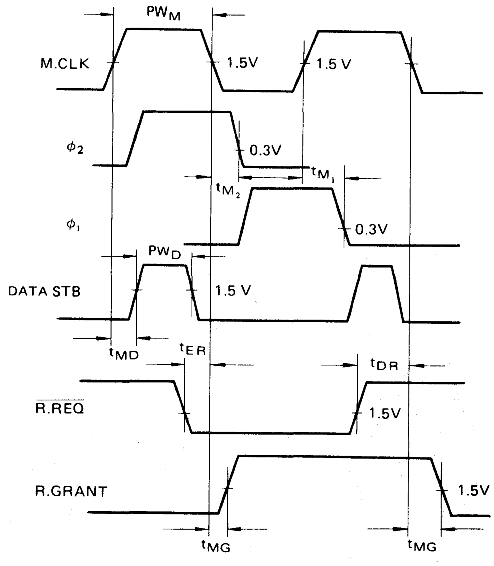


Fig. 6—TIMING DIAGRAM (3)



TYPICAL CHARACTERISTICS CURVES

Fig. 7 – I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

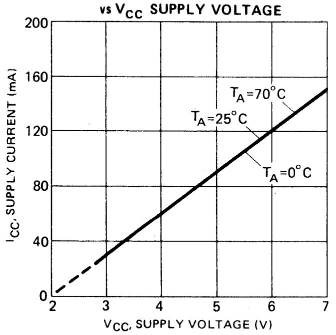
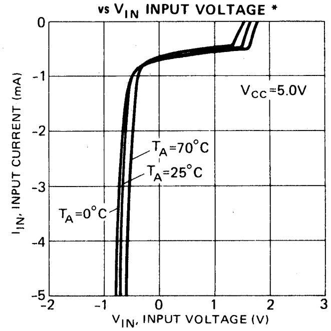


Fig. 8 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE *



* except inputs with pull-up resistor

Fig. 9 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE(TTL OUTPUTS)

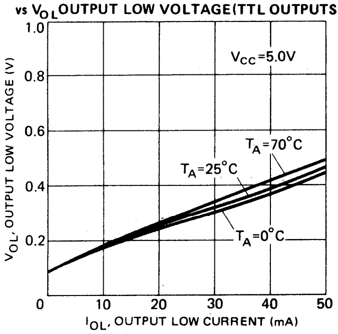


Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE(TTL OUTPUTS)

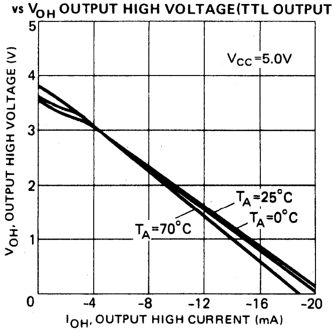


Fig. 11 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE(ϕ OUTPUTS)

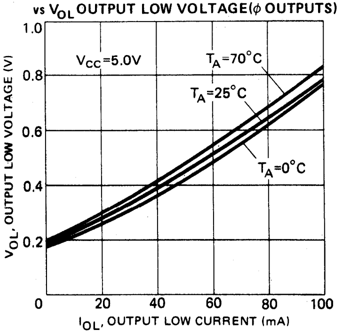


Fig. 12 – ϕ_1, ϕ_2 CLOCK PULSE WIDTH vs T_C CYCLE TIME

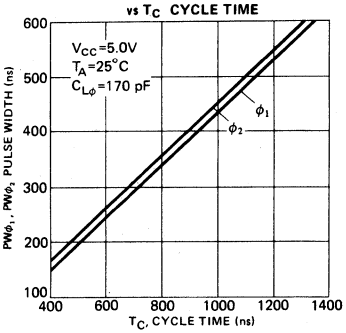


Fig. 13 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE (ϕ OUTPUTS)

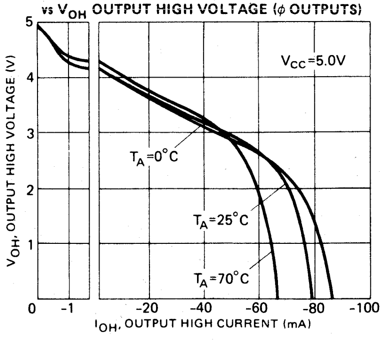
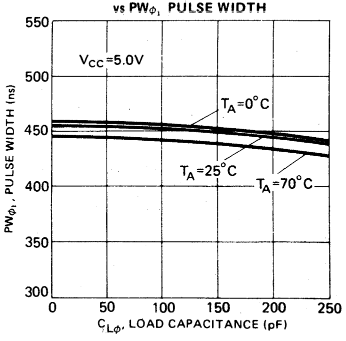


Fig. 14 – $C_{L\phi}$ LOAD CAPACITANCE vs $PW\phi_1$ PULSE WIDTH



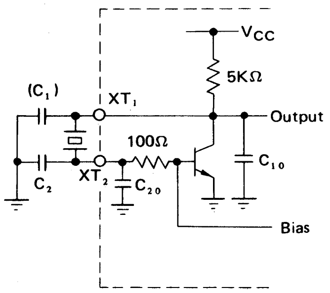
APPLICATIONS INFORMATION

1. Crystal Oscillator:
The crystal oscillator circuitry is shown in Fig. 15. Oscillations between the serial (f_0) and parallel (f_∞) resonant frequency of the crystal can be generated. Pico farad capacitors (C_{10}, C_{20}) are diffused on-chip. Therefore, oscillation can be generated by simply connecting an external capacitor ($C_2 \sim 50_pF$) from XT_2 to ground. Normally, a crystal with a resonant frequency of four or sixteen times the desired output clock driver frequency is used. The selection depends on whether the R. SEL pin is high (16X) or low (4X).

External crystal specifications:

Oscillator Frequency	22 MHz max.
Load Capacitance	10 ~ 30 pF
Equivalent Resistance	75 ohms max.
Resonant Power	4 mW max.

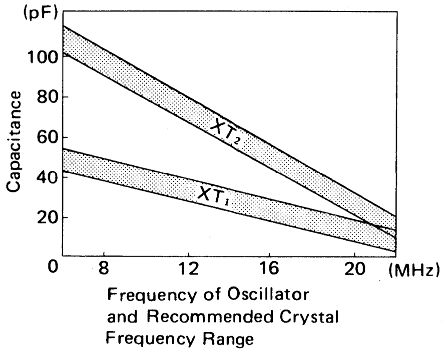
Fig. 15—Oscillation Circuitry



Typical Frequency of Crystal Oscillator

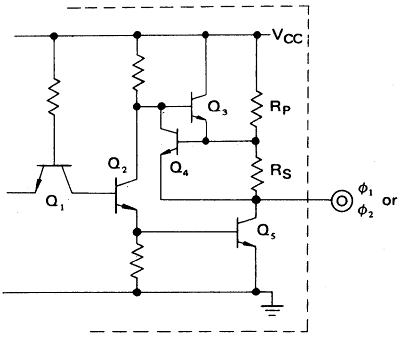
Clock Frequency (MHz)	Cycle Time (ns)	Inherent Frequency of Crystal Oscillator (MHz)	
		R.SEL=H	R.SEL=L
1.00	1000	16.00	–
1.33	750	21.33	–
2.00	500	–	8.00

Fig. 16—Standard Capacitance for Crystal Oscillator



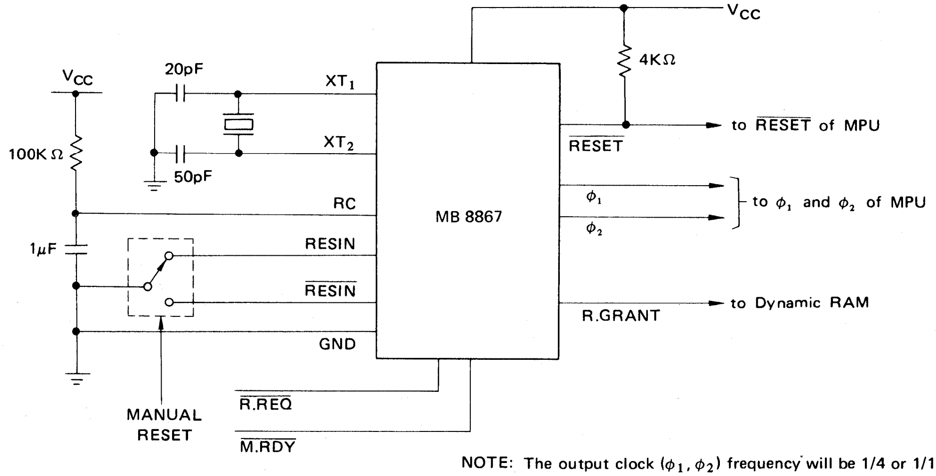
2. ϕ_1, ϕ_2 Clock Driver Circuit
The output clock driver circuit is shown in Fig. 17.
These circuits are designed to drive capacitive loads with a high amplitude pulse train. The pull-up resistor R_p has a nominal value of 500 ohms, and is on-chip in order to swing ϕ_1, ϕ_2 up to V_{CC}. When ϕ_1, ϕ_2 are grounded, R_s (10 ohms) and Q_4 protect the output driver Q_3.

Fig. 17—Clock Driver Circuitry



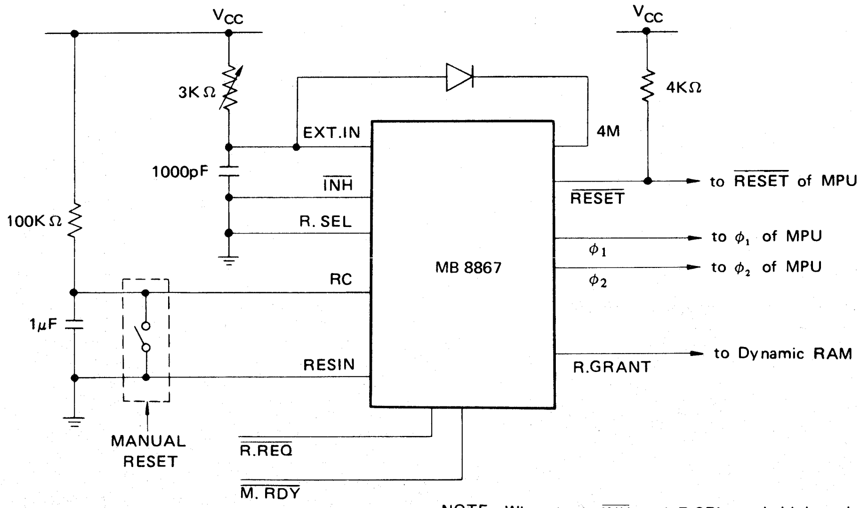
3. Input Controls
All input controls ($\overline{INH}$, R. SEL, $\overline{R. REQ}$, $\overline{M. RDY}$, RESIN, $\overline{RESIN}$) are TTL compatible. To simplify system packaging, all these pins have internal pull-up resistors so that they may be left open (unconnected) if desired.

Fig. 18–CLOCK GENERATION USING CRYSTAL


V_CC
4KΩ
V_CC
20pF
XT1
XT2
100KΩ
50pF
RC
1μF
RESIN
$\overline{\text{RESIN}}$
GND
MB 8867
to $\overline{\text{RESET}}$ of MPU
$\overline{\text{RESET}}$
φ1
φ2
to φ1 and φ2 of MPU
R.GRANT
to Dynamic RAM
MANUAL RESET
$\overline{\text{R.REQ}}$
$\overline{\text{M.RDY}}$

NOTE: The output clock (ϕ_1, ϕ_2) frequency will be 1/4 or 1/16 of the crystal frequency depending upon whether R.SEL is high or low.

Fig. 19–CLOCK GENERATION USING EXTERNAL "RC" NETWORK



NOTE: When both $\overline{\text{INH}}$ and R.SEL are held low, the circuit between EXT. IN and 4M forms a five stage serial invertor. The osillation frequency of this ring oscillator is controlled by the external 3K ohm resistor.

APPLICATIONS INFORMATION (cont'd)

Fig. 20—REFRESH CONTROL APPLICATION

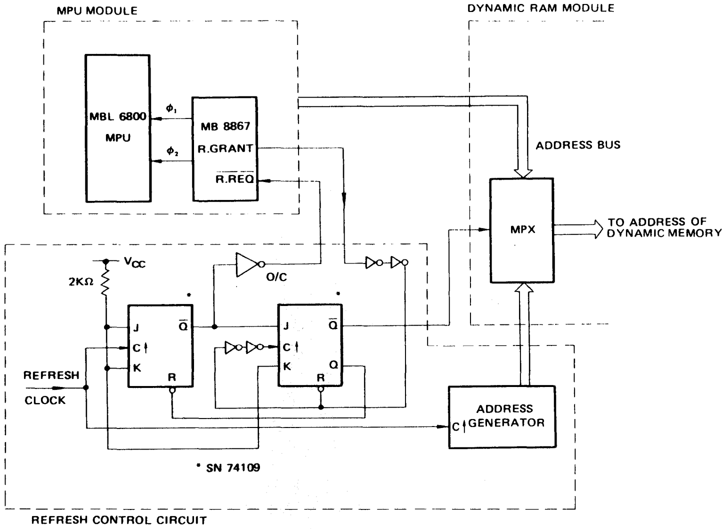
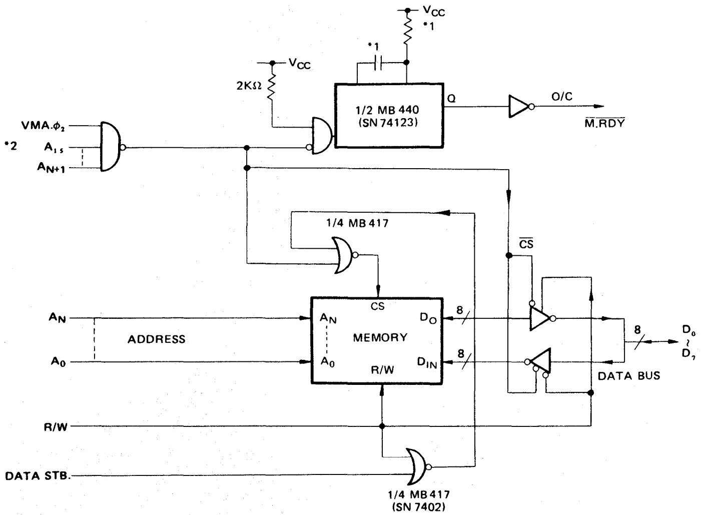


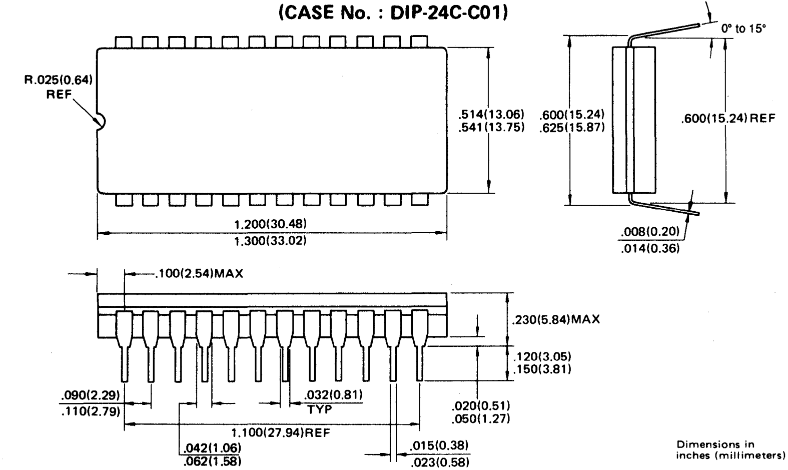
Fig. 21—LOW SPEED MEMORY APPLICATION



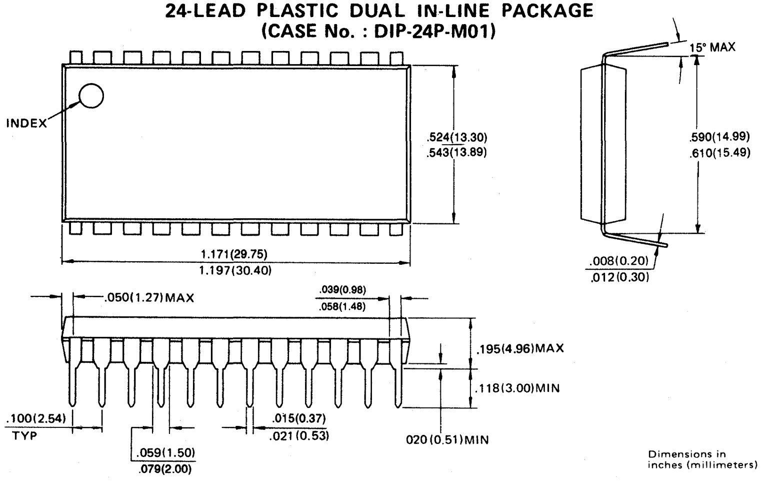
NOTE: *1. Values depend upon memory speed. For 1 μs cycle time, use 100 pF and 25KΩ.
*2. Inverter for address selection may be used.

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE (CASE No. : DIP-24C-C01)



24-LEAD PLASTIC DUAL IN-LINE PACKAGE (CASE No. : DIP-24P-M01)



SELECTOR GUIDE

ANALOG-TO-DIGITAL CONVERTERS

Device Number	Description	Resolution (bits)	Linearity (%)	Analog Input Voltage Range (V)	Conversion Speed	Supply Voltage (V)	Max. Supply Current (mA)	I/O Level	Package	Alternate Source
MB4052[1]	Bipolar 4-ch. 8-bit A/D Converter: Successive approximation technique, Serial output	8	±0.19	3 Modes: 0 to 0.625, 0 to 2.5, 0 to 10	100 µs/ ch Max	3.5–6.0 or 8.0–18	30 at V_{CC} = 6V	TTL/ CMOS, Open Collector	DIP-16C-C02 DIP-16P-M02	-
MB4053[2]	Bipolar 6-ch. A/D Converter Subsystem: Single slope method, Pulse width output, scale correction	-	±0.2	0 to (V_{CC}−2), 5.25 Max	350 µ/ ch Max	4.75 to 15	10	TTL	DIP-16C-C02 DIP-16P-M01 FPT-16P-M01	µA 9708
MB4056[3]	Bipolar 8-channel, successive approximation technique, Serial output	6	0.19	0 to 1.25; 0 to 5	100 µ/ channel max	4.75 to 18	40	TTL	DIP-20P-M01	-
MB4063[2]	MB4053 with on-chip voltage divider	-	±0.2	0 to (V_{CC}−2), 5.25 Max	350 µs/ ch Max	-	-	TTL	DIP-16C-C02 DIP-16P-M01 FPT-16P-M01	-
MB40547-7[3] -8[3]	Bipolar High Speed 1-ch. 8-bit A/D Converter: Fully-parallel comparison method	8 8	±0.4 ±0.2	V_{CC} to (V_{CC}−2)	20 MSPS	−5.2 ±5%	−280	10K ECL	DIP-24C-A01	-
MB40576[3]	Bipolar High Speed 1-ch. 6-bit A/D Converter: Fully-parallel comparison method	6	±0.8	V_{CC} to (V_{CC}−2) 1V Width	20 MSPS	+5.0 ±5%	80	TTL	DIP-16P-M04	-

DIGITAL-TO-ANALOG CONVERTERS

MB4072[2]	8-bit High Speed Multiplying D/A Converter: High-Z open-collector outputs	8	±0.2	−10 to +18 (V_S = ±15V)	150 ns	±4.5 to ±18	3.8 for V_S^+ = 15V −7.8 for V_S^- = −15V	Any	DIP-16C-C02 DIP-16P-M02 FPT-16P-M02	DAC-08
MB40748-8[3] -9[3]	10-bit High Speed D/A Converter	10	±0.2 ±0.1	0 to −1	30 MSPS	−5.2 ±5%	−90	10K ECL	DIP-24C-A01	-
MB40776[3]	6-bit High Speed D/A Converter: Suitable for digital TV	6	±0.8	V_{CC} to (V_{CC} −1)	20 MSPS	+5 ±5%	65	TTL	DIP-16P-M04	-
MB40778[3]	8-bit High Speed D/A Converter: Suitable for digital TV	8	±0.2	V_{CC} to (V_{CC} −1)	30 MSPS	+5 ±5%	75	TTL	DIP-18P-M01	-
MB40788[3]	10-bit Ultra High Speed D/A Converter: Pin compatible with MB40748	10	±0.2	0 to −1	125 MSPS	−5.2 ±5%	−135	10K ECL	DIP-24C-A01	-

Notes:

1. T_A = −30°C to +85°C
2. T_A = −40°C to +85°C
3. T_A = 0°C to +70°C

FUJITSU

CMOS PERIPHERALS

SOON TO BE AVAILABLE

INTRODUCTION

The MB892xx series of CMOS peripherals are presently being developed with engineering samples already available on all of the devices. This CMOS family of peripherals is specifically aimed at reducing system power consumption. The advanced information provided in this document represents the functional design targets of Fujitsu, and may change without notice. For the most current parametric data and other technical information, the user should contact the nearest Fujitsu Sales Office—refer to the back of this Data Book.

FUJITSU

DMA CONTROLLER

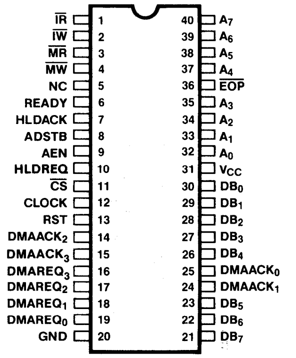
MB89237A

April 1986

DESCRIPTION

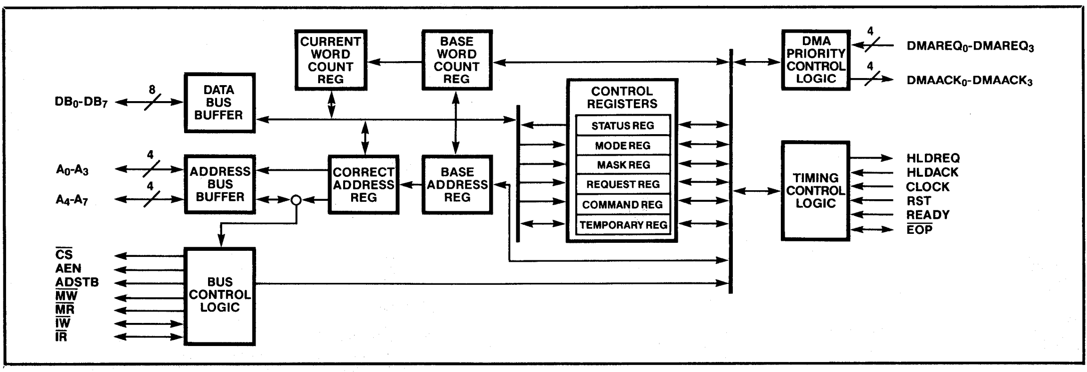
The Fujitsu MB89237A Direct Memory Access (DMA) Controller performs memory-to-memory and memory-to-I/O data transmissions with virtually no control burden on the CPU. The device can handle up to four DMA channels and is functionally compatible with the Intel 8237A NMOS device. The MB89237A is fabricated in CMOS and is housed in a 40-pin plastic DIP. The MB89237 is an ideal choice for applications where minimum control overhead is required and data throughput is of primary importance.

PIN CONFIGURATION



Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



FUJITSU

SERIAL DATA TRANSMITTER/ RECEIVER

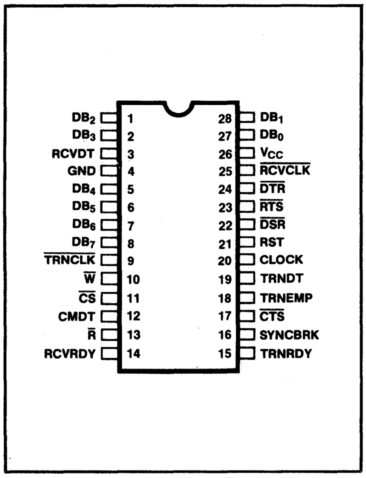
MB89251A

April 1986

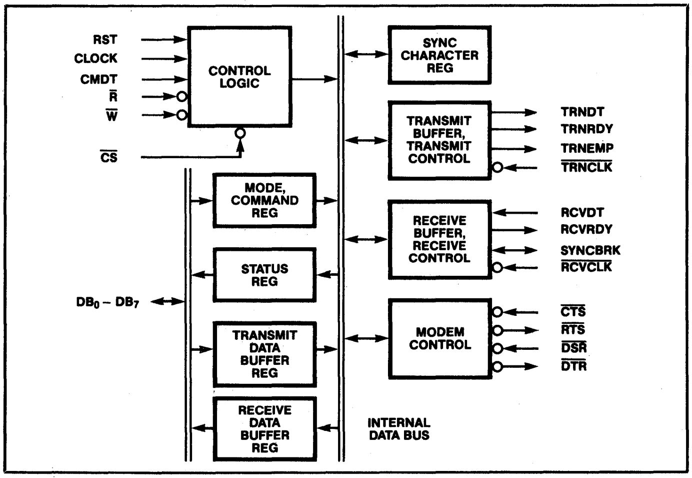
DESCRIPTION

The Fujitsu MB89251A Serial Data Transmitter/Receiver provides a duplex communications link between serial-data peripherals and the master processing system. The MB89251A supports both synchronous and asynchronous modes of operation and provides data transfer rates of up to 240K-bps. The MB89251A is fabricated in CMOS and is housed in a 28-pin plastic DIP. The device is functionally compatible with the Intel 8251A NMOS device.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

PROGRAMMABLE TIMER

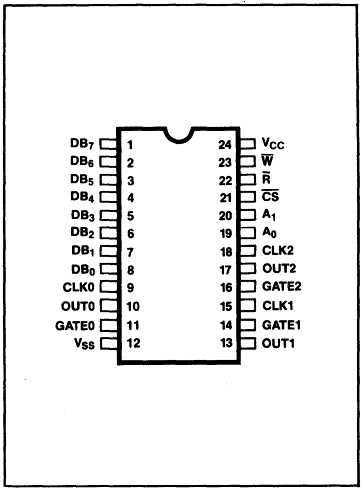
MB89254

April 1986

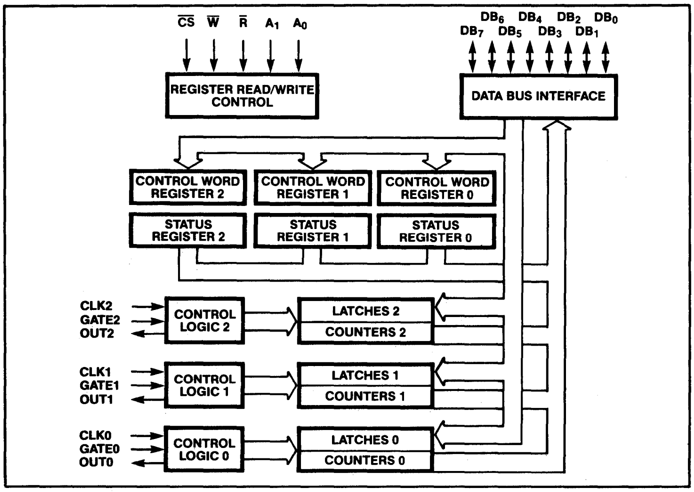
DESCRIPTION

The Fujitsu MB89254 Programmable Timer provides three totally independent timer channels. The user can select one of six operating modes for each channel and a variety of output waveforms (pulse, squarewave, etc). Under program direction, the timer serves as a "special-effects" generator and can be used for flag control, special system-control functions, and other supervisory chores. The MB89254 is fabricated in CMOS and is housed in a 24-pin plastic DIP. The device is functionally compatible with the Intel 8254 NMOS device.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

PARALLEL DATA I/O INTERFACE

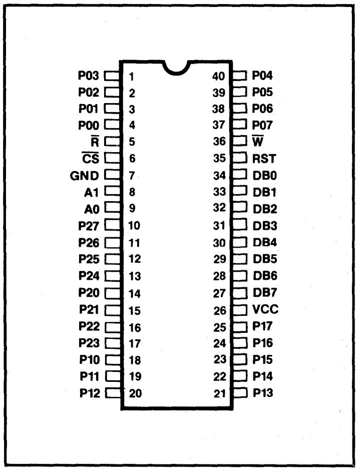
MB89255A

April 1986

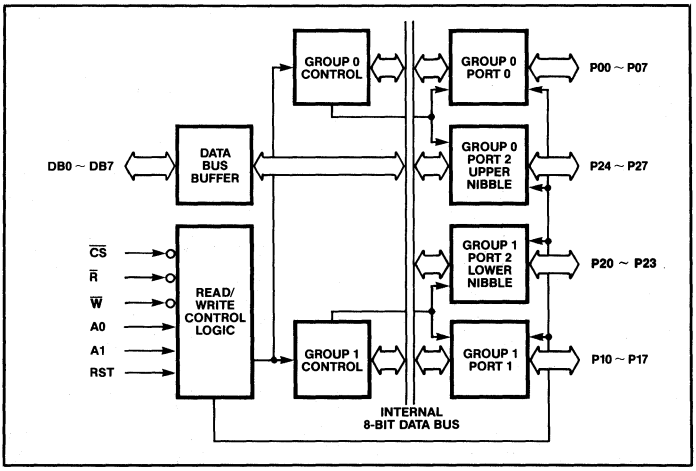
DESCRIPTION

The Fujitsu MB89255A Parallel Data I/O Interface provides an 8-bit bi-directional data-bus port and three 8-bit parallel I/O ports. Two of the I/O ports provide data transfers in byte segments whereas the other port is split with the upper and lower nibbles being transferred by separate busses. Thus, the MB89255A can be easily interfaced to hybrid 4-bit/8-bit systems. The user can choose either of three operating modes and can set or reset the state of each port bit. The MB89255A is fabricated in CMOS and is housed in a 40-pin plastic DIP. The device is functionally compatible with the Intel 8255A NMOS device.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

INTERRUPT CONTROLLER

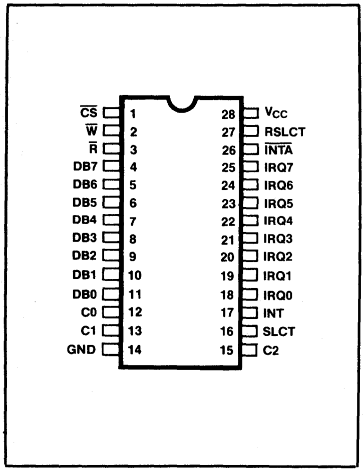
MB89259A

April 1986

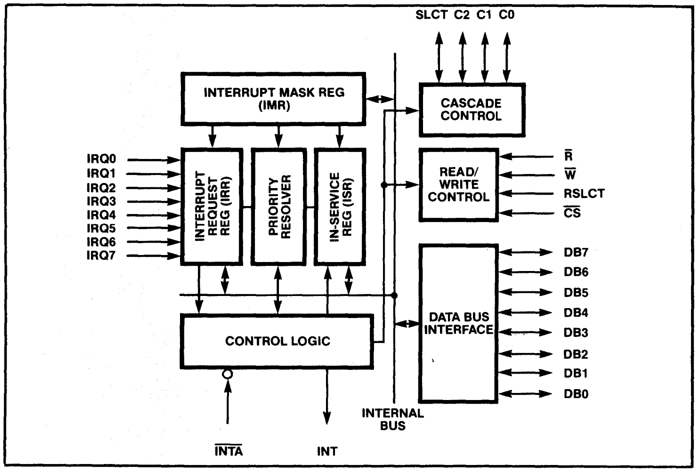
DESCRIPTION

The Fujitsu MB89259A Interrupt Controller is capable of prioritizing eight interrupt inputs and, in a cascade configuration, up to 64 interrupts can be handled without excessive delay. Each interrupt input is identified by a programmed vector that corresponds to the active input. The user can program the device for edge or level triggering to activate the interrupt. The MB89259A is fabricated in CMOS and is housed in a 28-pin plastic DIP. The device is functionally compatible with the Fujitsu MBL8259A NMOS device and the Intel 8259A NMOS device.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

ADDRESS LATCHES

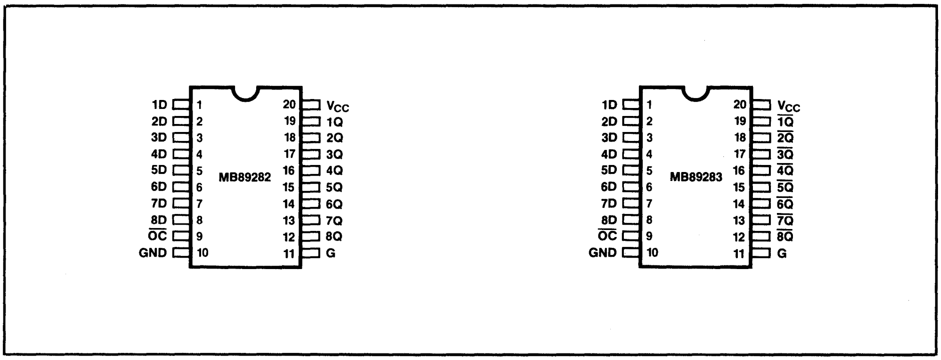
MB89282 MB89283

April 1986

DESCRIPTION

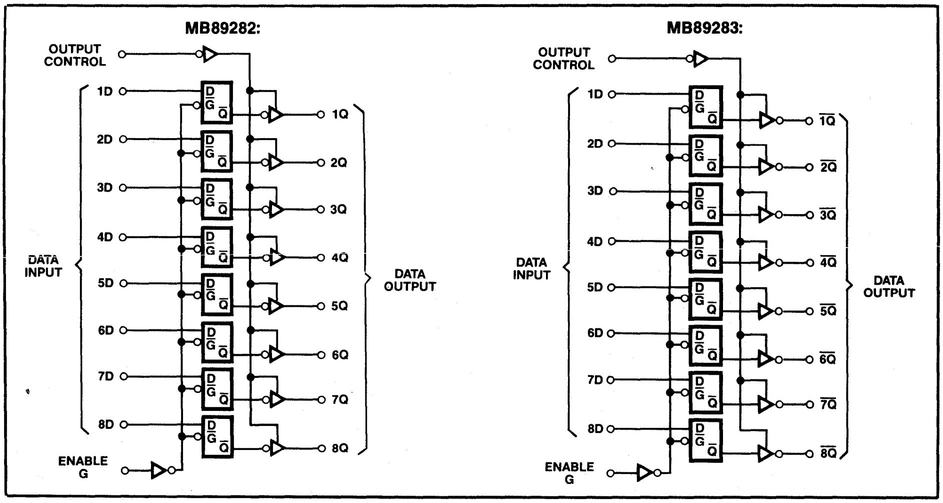
Both the Fujitsu MB89282 and MB89283 are 8-bit address latches. The MB89282 provides non-inverted outputs and those of the MB89283 are inverted. The devices are fabricated in CMOS and are housed in a 20-pin plastic DIP. The address latches are functionally compatible with the Fujitsu bipolar MBL8282/MBL8283 devices and the Intel bipolar 8282/8283 devices.

PIN CONFIGURATIONS



These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

BLOCK DIAGRAMS



FUJITSU

CLOCK GENERATOR

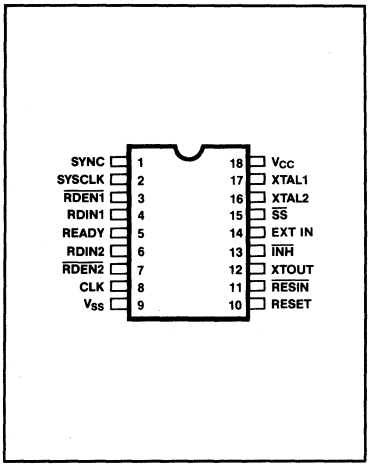
MB89284A

April 1986

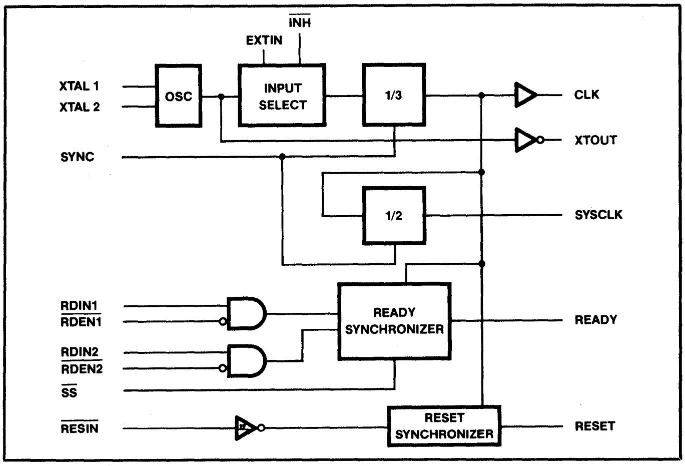
DESCRIPTION

The Fujitsu MB89284A Clock Generator generates a system clock and provides ready and reset signals for the MBL8086, MBL8088, and MBL8089 microprocessors. The device is fabricated in CMOS and is housed in a 20-pin plastic DIP. The MB89284A is functionally compatible with the Fujitsu bipolar MBL8284A device and the Intel bipolar 8284A.

PIN CONFIGURATION


SYNC 1
SYSCLK 2
$\overline{\text{RDEN1}}$ 3
RDIN1 4
READY 5
RDIN2 6
$\overline{\text{RDEN2}}$ 7
CLK 8
V_{SS} 9
18 V_{CC}
17 XTAL1
16 XTAL2
15 $\overline{\text{SS}}$
14 EXT IN
13 $\overline{\text{INH}}$
12 XTOUT
11 $\overline{\text{RESIN}}$
10 RESET

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

DATA BUS TRANSCEIVERS

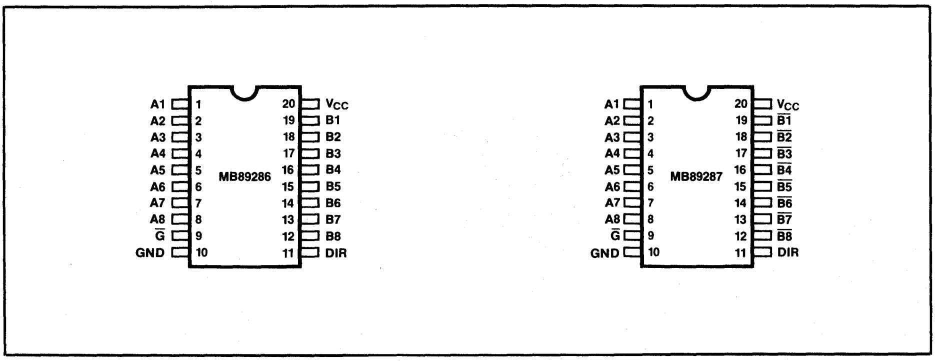
MB89286 MB89287

April 1986

DESCRIPTION

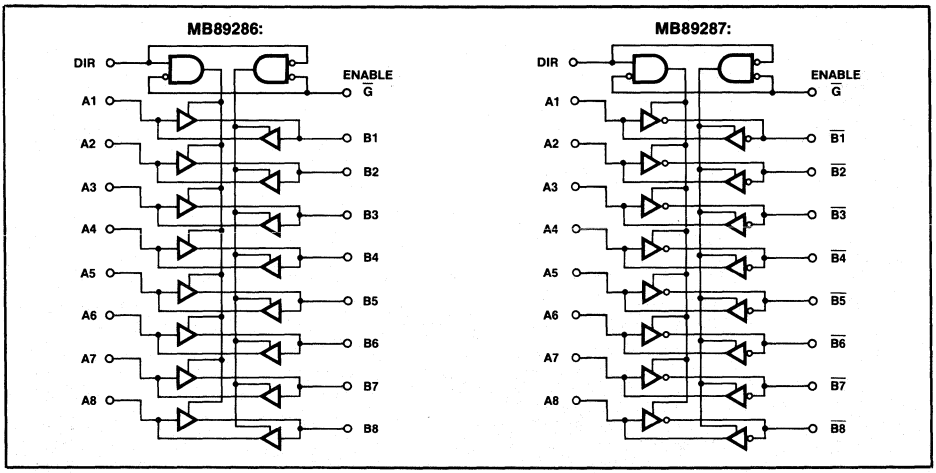
The Fujitsu MB89286/MB89287 Data Bus Transceivers serve as buffers between the local data bus of the processor and the system data bus. Outputs of the MB89286 are non-inverting whereas, for the MB89287, the outputs are inverted. Both devices are fabricated in CMOS and each is housed in a 20-pin plastic DIP. The bus transceivers are functionally compatible with the Fujitsu bipolar MBL8286/MBL8287 devices and the Intel bipolar 8286/8287 devices.

PIN CONFIGURATIONS



These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

BLOCK DIAGRAMS



FUJITSU

BUS CONTROLLER

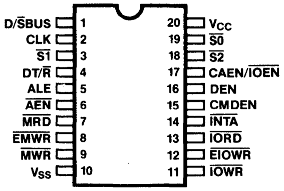
MB89288

April 1986

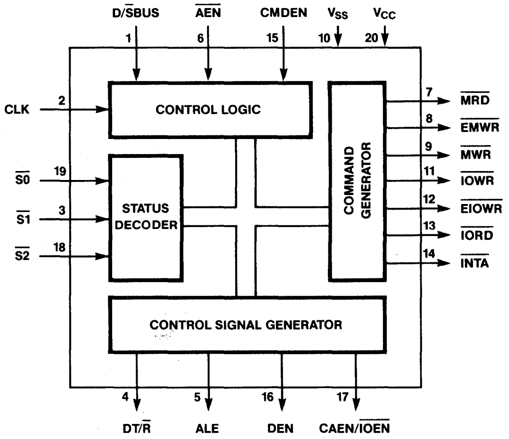
DESCRIPTION

The Fujitsu MB89288 Bus Controller receives and decodes status signals from either of several microprocessors (MBL8086, MBL8088, MBL8089, MBL80186, or MBL80188) and provides command/control signals to memory and I/O devices. The MB89288 controller is fabricated in CMOS and is housed in a 20-pin plastic DIP. The MB89288 is functionally compatible with the Fujitsu bipolar MBL8288 bus controller and the Intel bipolar 8288 device.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

BUS ARBITER

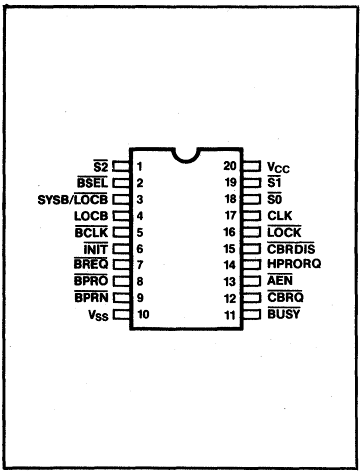
MB89289

April 1986

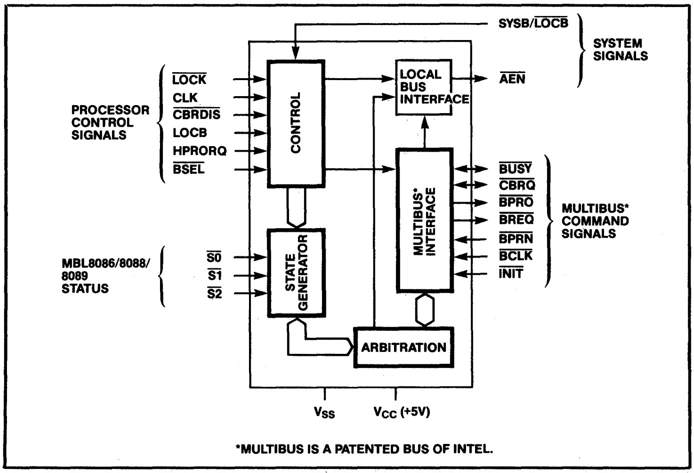
DESCRIPTION

The Fujitsu MB89289 Bus Arbiter is designed for use in multi-processor systems where conflicts of bus-access are likely to occur. When multiple bus masters request simultaneous access to the system bus, the MB89289 monitors these requests, assigns priorities, and grants access in an orderly manner. The MB89289 bus arbiter is fabricated in CMOS and is housed in a 20-pin plastic DIP. The MB89289 is functionally compatible with the Fujitsu bipolar MBL8289 arbiter and the Intel bipolar 8289 device.

PIN CONFIGURATION



BLOCK DIAGRAM



*MULTIBUS IS A PATENTED BUS OF INTEL.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Section 5

Local Area Network (LAN) Products

FUJITSU

ETHERNET ENCODER / DECODER

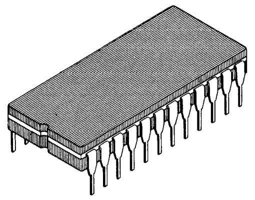
MB 502A

October 1983
Edition 2.0

ETHERNET ENCODER/DECODER

The Fujitsu MB 502A is an Ethernet* Encoder/Decoder designed to meet all the requirements of the Ethernet Blue Book specification and fabricated with high-speed ECL and Schottky TTL technology.

The encoder converts serial binary data into complementary Manchester code. The decoder converts Manchester code into binary data and synchronous clock signals. The decoding method is a digital phase locked loop with dual bandwidth which allows both fast lock-on and a small amount of jitter. Typical acquisition is eight bits or better. A key feature of the decoder design is its capability to recover distorted input signals. The MB 502A is packaged in a 24-pin ceramic standard DIP.

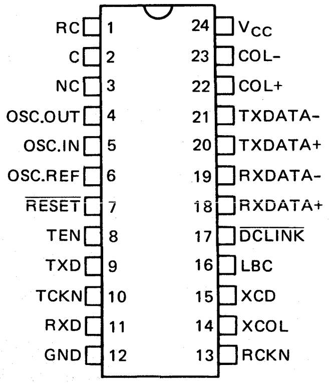


CERAMIC PACKAGE
DIP-24C-C01

FEATURES

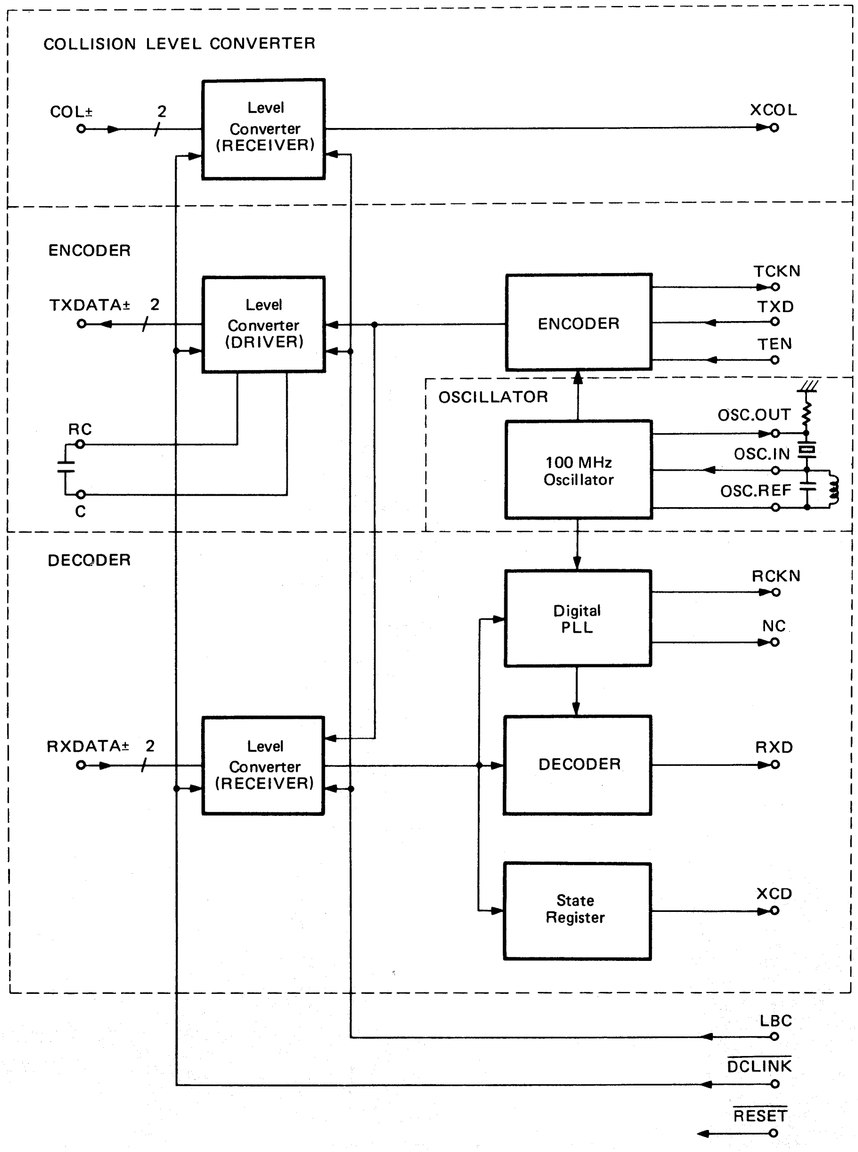
- Full Ethernet compatibility
- Manchester encode and decode
- Level conversion: transceiver level to/from TTL level
- Carrier detection
- Large distortion recovery: ±20 ns
- Dual bandwidth phase locked loop: allows fast acquisition
- Loopback "CONFIDENCE" test feature
- Built-in clock generator
- Small external parts count: all passive external components
- High-speed ECL and Schottky TTL technology
- Single power supply: +5V
- Low power dissipation: 750mW typ.
- 24-pin standard Dual In-line Ceramic Package

PIN ASSIGNMENT



*Ethernet is a trade mark of Xerox Corp. U.S.A.

Fig. 1 BLOCK DIAGRAM



PIN ASSIGNMENT TABLE

Group	Pin Number	Symbol	Pin Name	I/O	Level	Function
Power Group	12	GND	Power supply	I		Ground
	24	V_{CC}		I		+5V DC power supply
Cable Group	18 19	RXDATA+ RXDATA-	Receive data pair	I I	ECL differential	Interfacing to receive pair of the transceiver cable.
	20 21	TXDATA+ TXDATA-	Transmit data pair	O O	ECL differential	Interfacing to transmit pair of the transceiver cable.
	22 23	COL+ COL-	Collision presence pair	I I	ECL differential	Interfacing to collision presence pair of the transceiver cable.
EDLC Group	8	TEN	Transmit encode enable	I	TTL	Input for encoding and TXDATA± enable.
	9	TXD	Transmit serial data	I	TTL	Input for transmit data to be encoded onto the Ethernet coax.
	10	TCKN	Transmit data clock	O	TTL	Stable 10MHz clock output for transmit bit stream.
	11	RXD	Receive serial data	O	TTL	Output of received and decoded bit stream.
	13	RCKN	Receive data clock	O	TTL	Clock output to strobe RXD.
	14	XCOL	Collision presence	O	TTL	Duplication of the collision presence pair (COL±).
	15	XCD	Receive carrier detect	O	TTL	Carrier detect function of the decoder.
	16	LBC	Loopback command	I	TTL	Input to command the MB502A to operate in loopback mode.
Oscillator Group	4 5 6	OSC. OUT OSC. IN OSC. REF	Oscillator pins	O I O	ECL	Pins for direct connection of discrete oscillator components.
Others	1 2	RC C	Capacitor pins	– –	ECL –	Pins for direct connection of a capacitor.
	3	NC	Non-connection (PLL test)	O	ECL	Output pin for PLL testing purpose only.
	7	$\overline{\text{RESET}}$	FF test	I	TTL	Input pin to initialize flip-flops for testing purpose only.
	17	$\overline{\text{DCLINK}}$	DC/AC coupling select for transceiver pairs	I	TTL	Input to select DC/AC coupling of transceiver cable pairs.

FUNCTIONAL DESCRIPTION

The MB 502A has five major functions; encode, decode, collision, master clock generation and loopback.

ENCODE

The encoder section of the MB 502A is a simple circuit which performs an appropriate exclusive-OR between the transmit clock and transmit data using latches to reduce the skew of TXDATA± outputs. The encoder sends the transmit clock (TCKN) to the Data Link controller. Then an encode enable signal (TEN) and data (TXD) are returned from the Data Link controller.

DECODE

The decoder performs three functions. First, it decodes data using the differential receive inputs (RXDATA+ and RXDATA-) of the transceiver cable. Next is the carrier detect function. The carrier is derived from the receive inputs and passed to the Data Link controller from the XCD output. The last function is the stripping of the first several bits (eight bits maximum) of the packet. This is not a part of the Ethernet Physical Layer specification. The receive clock (RCKN) is actually inhibited for 6 or 7 clock cycles to allow the PLL (phase locked loop) to gain acquisition. This function was designed into the Encoder/Decoder because the EDLC (Ethernet Data Link Controller, MB 8795B) is a byte oriented device, and the function is more appropriately provided in the Encoder/Decoder which is bit oriented.

The decoder PLL has excellent distortion handling capability. It is designed to recover ± 20ns exercised.

COLLISION

The collision detect inputs (COL+ and COL-) are simply converted to a TTL level signal (XCOL). The latching and timing functions for this signal are provided in the EDLC (MB 8795B).

MASTER CLOCK GENERATION

The oscillator generates and supplies a 100MHz master clock signal to the encoder and decoder.
Discrete oscillator components such as a crystal may be directly connected to the provided oscillator pins.
The oscillation frequency must be 100MHz with a tolerance of less than ±0.01% to meet the Ethernet specification because one tenth of the oscillation frequency is the transmit bit rate.

LOOPBACK

A loopback input is provided to allow all encoding and decoding functions to be exercised without using the transceiver cable. During loopback operation, the encoded data is routed internally to the decoder, the transmit outputs are idle, and the receive and collision inputs are ignored.

SIGNAL PIN DESCRIPTION

CABLE GROUP

RXDATA± (receive serial data pair, inputs)

These are the inputs to the decoder. They receive Manchester coded signals which the transceiver encounters on the Ethernet coax.
The input circuit is a differential receiver and can receive voltages of 0 to V_{CC}. The differential receiver has two operation modes; DC coupled operation and AC coupled operation, which are selected by $\overline{\text{DCLINK}}$ input.
In DC coupled operation ($\overline{\text{DCLINK}}$ is low), the differential threshold is typically 0V. The differential input voltage of more than 0.2V is regarded as high level and the differential input voltage of less than -0.2V is regarded as low level.
In AC coupled operation ($\overline{\text{DCLINK}}$ is high), the differential threshold is typically -0.2V. A differential input voltage of more than -0.05V is regarded as high level and a differential input voltage of less than -0.4V is regarded as low level.
The receiver circuit is designed to supply a high level to the decoder when RXDATA+ and RXDATA- are not receiving data but are just short-circuited through a transformer coil or left unconnected. However, when RXDATA± are receiving data, the differential threshold is typically 0V to minimize receiving distortion.

TXDATA± (transmit data pair, outputs)

These are the outputs of the encoder. They transmit Manchester coded signals to the transceiver.
The driver output circuit is an emitter-follower and requires a pull-down resistor (270Ω typ.). It can drive a transceiver cable differential impedance of 78Ω.

The differential transmitter outputs (TXDATA+ and TXDATA-) also have the ability to emulate a transformer drive. This is actually implemented to reduce the current involved in a transformer termination of the transmit outputs in the transceiver which has a DC resistance of zero ohms. After the encoding function stops, the transmitter outputs gradually return to a 0V differential between the two output wires. The returning time is determined by an external capacitor connected between the RC and C pins.

COL± (collision presence pair, inputs)

This pair of signals indicates the presence of a collision generated by the transceiver.
The input circuit is a differential receiver and can receive voltages of 0V to V_{CC}. The differential receiver has two operation modes; DC coupled operation and AC coupled operation, which are selected by $\overline{\text{DCLINK}}$ input.
In DC coupled operation ($\overline{\text{DCLINK}}$ is low), the differential threshold is typically 0V. A differential input voltage of more than 0.2V is regarded as high level and a differential input voltage of less than -0.2V is regarded as low level.
In AC coupled operation ($\overline{\text{DCLINK}}$ is high), the differential threshold is typically -0.2V. A differential input voltage of more than -0.05V is regarded as high

level and a differential input voltage of less than -0.4V is regarded as low level.
The receiver circuit is designed to supply a high level to the level converter when COL+ and COL- are not receiving data but are just short-circuited through a transformer coil or left unconnected.
Unlike RXDATA±, the differential threshold is set to -0.2V even when COL± are receiving data.

EDLC GROUP

TEN (transmit encode enable, input)
This is an input to the on-chip Manchester encoder and enables TXDATA pair. Input high enables TXDATA pair; input low makes TXDATA pair idle (high).

TXD (transmit serial data, input)
This is an input to the on-chip Manchester encoder and provides data to be encoded.
Serial binary data must be supplied to this input synchronously with the falling edge of TCKN (transmit data clock).
This input is enabled when TEN (transmit encode enable) is high.

TCKN (transmit data clock, output)
10MHz clock output for the transmit serial binary data. This is stable one-tenth of the master clock frequency. See TXD (transmit serial data) description.

RXD (receive serial data, output)
This is an output of the on-chip Manchester decoder and provides decoded data from Ethernet coax to a Data Link controller.
This output is synchronous with the falling edge of RCKN (receive data clock).

RCKN (receive data clock, output)
Clock output to strobe RXD (receive serial data). See RXD (receive serial data) description.
At the beginning of a packet, RCKN is inhibited for 6 or 7 clock cycles to allow the PLL to gain acquisition. And at the end of a packet, RCKN is inhibited for 1 clock cycle.
During idle state, this output generates a 10MHz clock signal.

XCOL (collision presence, output)
This is a TTL duplication of the collision presence pair (COL±). The transceiver connected to Ethernet coax supplies a high level or differential voltage of 0V to COL ± when collision is not seen on the coax. It supplies a 10MHz square wave signal to COL ± when collision is detected. Accordingly, XCOL outputs high level when collision is not seen and outputs a 10MHz square wave signal during collision presence.

XCD (receive carrier detect, output)
This output provides carrier detect function of the Manchester decoder. This signal is used by a Data Link controller receiver as a data acquisition enable signal and by a Data Link controller transmitter as transmition permission information.
Output is low when the Ethernet coax is idle.

LBC (loopback command, input)
High level input to this pin dictates loopback mode operation. During the loopback mode operation,
XCOL output is high level,
TXDATA+ output is high level,
RXDATA± inputs are ignored
and the data supplied to TXD (transmit serial data) when TEN (transmit encode enable) is high is encoded, supplied to the Manchester decoder through the internal route and output from RXD (receive serial data), RCKN (receive data clock) and XCD (receive carrier detect).

OSCILLATOR GROUP

OSC.OUT, OSC.IN AND OSC.REF (oscillator pins)
A 100MHz crystal is to be placed between OSC.IN and OSC.OUT.
An LC tank circuit is to be placed between OSC.IN and OSC.REF to assure start-up in the proper harmonic of the crystal.
OSC.OUT is an emitter-follower output and requires a pull-down resistor (330Ω typ.). A phase adjusting capacitor is to be placed in parallel with the pull-down resistor to make the delay through the oscillator close to 10ns to increase the efficiency of the crystal.

As a design recommendation, connection wires should be as short as possible.

OTHERS

RC and C (capacitor pins)
A capacitor placed between these pins provides the timing for the transformer emulation of the transmit pair.
In AC coupled operation ($\overline{\text{DCLINK}}$ is high), after data transmission, TXDATA- goes high with rise time determined by the time-constant of the internal resistor and the connected capacitor. When a 470pF capacitor is connected, the rise time of TXDATA- is typically 0.8μs (20% to 80%).

Because pin C is connected to V_{CC} on chip, DC voltage must never be supplied to this pin.

$\overline{\text{DCLINK}}$ (DC/AC coupling select for transceiver pair)
This input is to select DC/AC coupling of transceiver cable pairs. Low level selects DC coupling. High level selects AC coupling and makes both TXDATA+ and TXDATA- high during idle state to prevent the transformer from saturation.
See CABLE GROUP description.

This pin must be stuck at high or low level. It may be connected directly to V_{CC} or ground.

$\overline{\text{RESET}}$ (FF testing purpose only)
This input pin is to initialize flip-flops for testing purposes only and must be connected to V_{CC} or stuck at high level in a normal operation.

NC (non-connection)
This output pin is for testing purposes only and must be left open in a normal operation.

ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to 7.0	V
TTL Level Input Voltage	V_{ITTL}	-0.3 to 7.0	V
Receiver Input Voltage	V_{IR}	-0.3 to V_{CC} + 0.3	V
Driver Output Voltage	V_{ODV}	V_{CC}(max)	V
Driver Output Current	I_{ODV}	-40.0 to 0	mA
Oscillator Input Voltage	V_{IOSC}	V_{CC}-4 to V_{CC}, and more than -0.3	V
Oscillator Output Current	I_{OOSC}	-20.0 to 0	mA
Operating Temperature	T_{OP}	-25 to 100	°C
Storage Temperature	T_{STG}	-65 to 125	°C

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as destailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value	Operating Temperature
Supply Voltage		V_{CC}	5.0V ± 5%	0°C to +70°C
TTL High Level Output Current		I_{OH}	-0.4 mA to 0 mA	
TTL Low Level Output Current		I_{OL}	0 mA to 8 mA	
Receiver Input Voltage		V_{IR}	0V to V_{CC}	
Driver Terminator		R_{LD}	270Ω	
Differential Load		R_{DLD}	78Ω	
Oscillator Terminator		R_{LOSC}	330Ω and 33pF parallel*	
Crystal for Oscillator		f_{XTAL}	100 MHz ± 0.01%**	
Capacitor placed between C and RC pins		C_{TX}	470pF	
LC Tank Constant	Inductance	L_{OSC}	0.15 μH	
	Capacitance	C_{OSC}	33pF*	

* The values of the oscillator capacitors may have to be tuned for a particular components layout. Both capacitors should be adjusted for maximum voltage at OSC.IN.
However, once the correct values are determined for that layout, any more tuning will not be necessary for each board.

** 5th overtone series resonant.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
			V_{CC}(V)	min.	typ.	max.	
High Level Input Voltage*1	V_{IH}			2.0			V
Low Level Input Voltage*1	V_{IL}					0.8	V
Input Clamp Voltage*1	V_{IC}	I_{IL} = -18mA	4.75	-1.5			V
High Level Output Voltage*2	V_{OH}	I_{OH} = -0.4mA	4.75	2.7			V
Low Level Output Voltage*2	V_{OL}	I_{OL} = 8mA	4.75			0.5	V
High Level Input Current*1	I_{IH}	V_{IH} = 2.7V	5.25			20	μA
Low Level Input Current*1	I_{IL}	V_{IL} = 0.4V	5.25	-100			μA
Output Short Current*2	I_{OS}	V_O = 0V	5.25	-100		-20	mA
High Level Differential Input Voltage*3	V_{IHD}	$V_{IR+} - V_{IR-}$ $\overline{\text{DCLINK}}$ = 0V		0.2			V
Low Level Differential Input Voltage*3	V_{ILD}	$V_{IR+} - V_{IR-}$ $\overline{\text{DCLINK}}$ = 0V				-0.2	V
High Level Differential Input Voltage*4	V_{IHD}	$V_{IR+} - V_{IR-}$ $\overline{\text{DCLINK}}$ = 4.5V		-0.05			V
Low Level Differential Input Voltage*4	V_{ILD}	$V_{IR+} - V_{IR-}$ $\overline{\text{DCLINK}}$ = 4.5V				-0.4	V
High Level Differential Input Voltage*5	V_{IHD}	$V_{IR+} - V_{IR-}$ $\overline{\text{DCLINK}}$ = 4.5V		0.2			V
Low Level Differential Input Voltage*5	V_{ILD}	$V_{IR+} - V_{IR-}$ $\overline{\text{DCLINK}}$ = 4.5V				-0.2	V
High Level Input Current*3	I_{IHR}	V_{IR} = 5.25V $\overline{\text{DCLINK}}$ = 0V	5.25			0.7	mA
Low Level Input Current*3	I_{ILR}	V_{IR} = 0V $\overline{\text{DCLINK}}$ = 0V	5.25	-1.5			mA

Note: 1: Applicable to TTL input pins. (TEN, TXD, LBC, $\overline{\text{DCLINK}}$ and $\overline{\text{RESET}}$)
2: Applicable to TTL output pins. (TCKN, RXD, RCKN, XCOL and XCD)
3: Applicable to COL± and RXDATA±.
4: Applicable to RXDATA± while XCD output is low (idle state) and COL±.
5: Applicable to RXDATA± while XCD output is high.

DC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
			V_{CC}(V)	min.	typ.	max.	
High Level Output Voltage *1	V_{OHTX}		5.0		4.1		V
Low Level Output Voltage *1	V_{OLTX}		5.0		3.3		V
High Level Differential Output Voltage *1	V_{OHD}	$V_{O+} - V_{O-}$ $\overline{\text{DCLINK}} = 0V$		0.55		1.0	V
Low Level Differential Output Voltage *1	V_{OLD}	$V_{O+} - V_{O-}$ $\overline{\text{DCLINK}} = 0V$		-1.0		-0.55	V
Oscillator Reference Voltage *2	V_{BB}		5.0		3.7		V
High Level Input Current *3	I_{IHO}	$V_{IH} = 4.1V$	5.0			150	μA
High Level Output Voltage *4	V_{OHO}	OSC.IN is open	5.0		4.15		V
Low Level Output Voltage *4	V_{OLO}	$V_{IOSC} = 4.1V$	5.0		3.3		V
RC Internal Resistor	R_{RC}	$V_{RC} = 0.5V$	0.5	25	50	100	kΩ
Power Supply Current	I_{CC}	All signal pins are open.	5.25			220	mA

Note: 1: Applicable to TXDATA±.
These pins are connected to ground through 270Ω resistor. And 78Ω resistor is placed between these pins.
2: Applicable to OSC.REF.
3: Applicable to OSC.IN.
4: Applicable to OSC.OUT.
This pin is connected to ground through a 330Ω resistor.

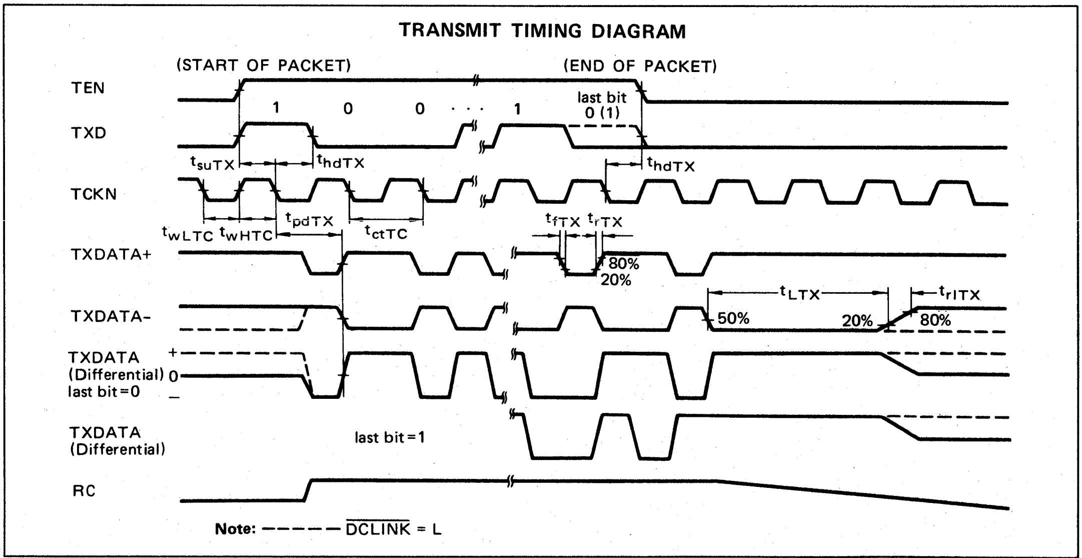
AC CHARACTERISTICS

TRANSMIT TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition		Value			Unit
			Fig.	min.	typ.	max.	
TCKN Cycle Time	t_{ctTC}		2, 3	99.99	100.00	100.01	ns
TCKN Low Time	t_{wLTC}		2, 3	40	50		ns
TCKN High Time	t_{wHTC}		2, 3	40	50		ns
TXDATA± Encode Time	t_{pdTX}		2, 3 5, 6		95		ns
TXDATA± Output Rise Time	t_{rTX}		5, 6		2.0		ns
TADATA± Output Fall Time	t_{fTX}		5, 6		2.0		ns
TXDATA– Low Level Hold Time	t_{LTX}	C_{TX} = 470pF $\overline{DCLINK}$ = V_{CC}	5, 6		3		μs
TXDATA– Idling Rise Time	t_{rITX}	C_{TX} = 470pF (20% ~ 80%) $\overline{DCLINK}$ = V_{CC}	5, 6		0.8		μs
TXD, TEN Setup Time	t_{suTX}		4	20			ns
TXD, TEN Hold Time	t_{hdTX}		4	0			ns

TRANSMIT TIMING DIAGRAM



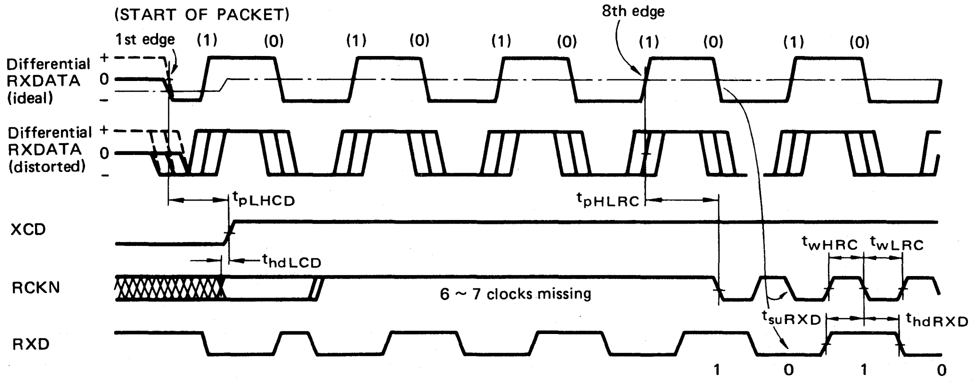
AC CHARACTERISTICS (Cont'd)

RECEIVE TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition		Value			Unit
			Fig.	min.	typ.	max.	
RCKN Cycle Time in Idle	t_{ctRC}		2, 3	99.99	100.00	100.01	ns
RCKN Low Time	t_{wLRC}		2, 3	35	50		ns
RCKN High Time	t_{wHRC}		2, 3	35	50		ns
RCKN Delay Time	t_{pHLRC}		2, 3, 7		120		ns
XCD ON Delay Time	t_{pLHCD}		2, 3, 7		80	110	ns
XCD OFF Delay Time	t_{pHLCD}		2, 3, 7		230		ns
XCD Low Hold Time	t_{hdLCD}		2, 3	0	10		ns
XCD High Hold Time	t_{hdHCD}		2, 3		120		ns
XCD Low Setup Time	t_{suLCD}		2, 3		80		ns
RXD Setup Time	t_{suRXD}		2, 3	20	60		ns
RXD Hold Time	t_{hdRXD}		2, 3	10	20		ns

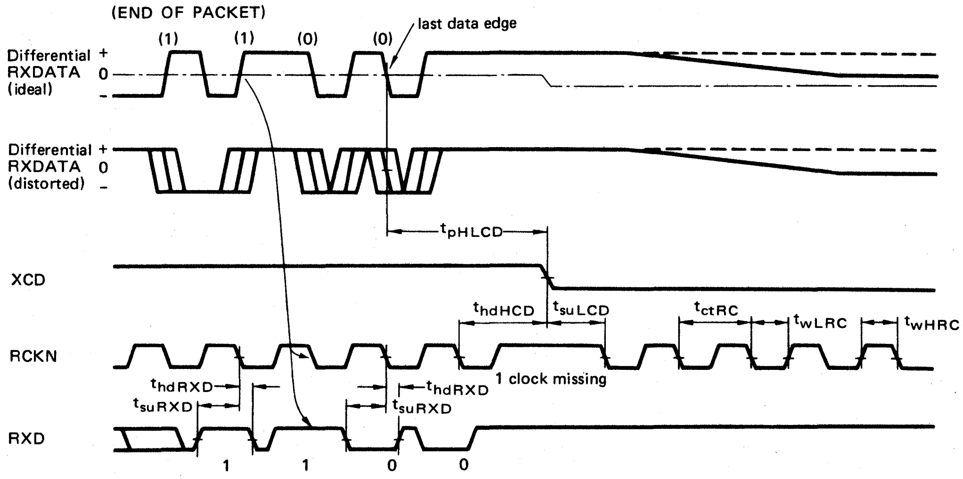
RECEIVE TIMING DIAGRAM



Note: —·— Threshold manipulation in AC coupled operation
– – – – – DC coupled operation

AC CHARACTERISTICS (Cont'd)

RECEIVE TIMING DIAGRAM (Cont'd)



Note: ——-—— Threshold manipulation in AC coupled operation
– – – – – DC coupled operation

AC CHARACTERISTICS (Cont'd)

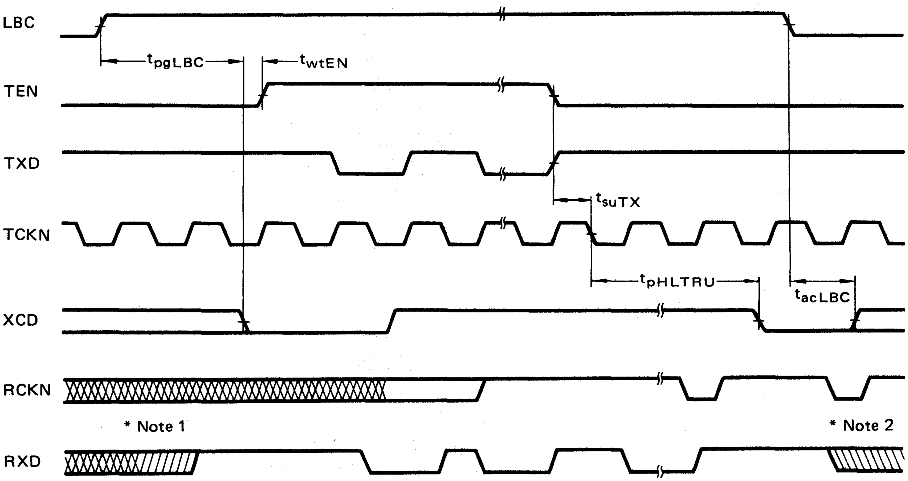
LOOPBACK TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition		Value			Unit
			Fig.	min.	typ.	max.	
LBC Receiving Data Purge Time	t_{pgLBC}		2, 3, 4		230		ns
LBC Receiving Data Accept Time	t_{acLBC}		2, 3, 4		80		ns
DATA Through Time	t_{pHLTRU}		2, 3, 4		280		ns
TEN Wait Time	t_{wtEN}		2, 3, 4	0			ns

In Loopback mode operation, COL± and RXDATA± inputs are ignored, TXDATA+ and XCOL are high level and XCD, RCKN and RXD functions are in the same manner as a normal receive operation.

LOOPBACK TIMING DIAGRAM



Note 1: When RXDATA± are receiving a packet at LBC rising, the received data is not complete.
Note 2: When RXDATA± are receiving a packet at LBC falling, the packet may not be decoded correctly.

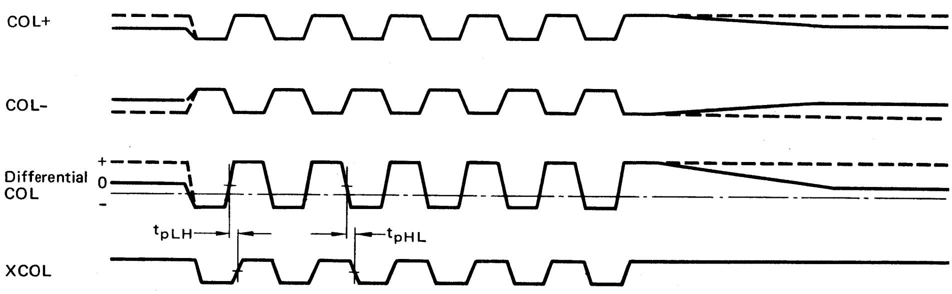
AC CHARACTERISTICS (Cont'd)

COLLISION TIMING

(Recommended operating conditions unless otherwise noted. V_{CC}=5.0V)

Parameter	Symbol	Condition		Value			Unit
			Fig.	min.	typ.	max.	
COL to XCOL Propagation Delay Time	t_{pLH}	$\overline{\text{DCLINK}}$ = 0V	2, 3, 7		9	30	ns
COL to XCOL Propagation Delay Time	t_{pHL}	$\overline{\text{DCLINK}}$ = 0V	2, 3, 7		11	30	ns

COLLISION TIMING DIAGRAM

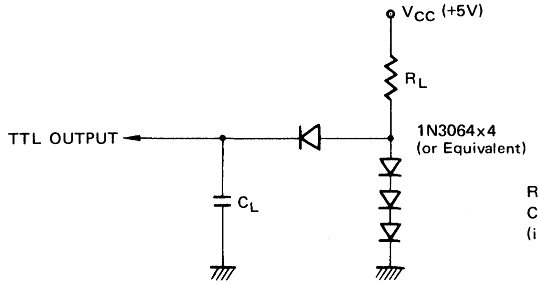


Note: —·— Threshold manipulation in AC coupled operation
– – – – – DC coupled operation

AC CHARACTERISTICS (Cont'd)

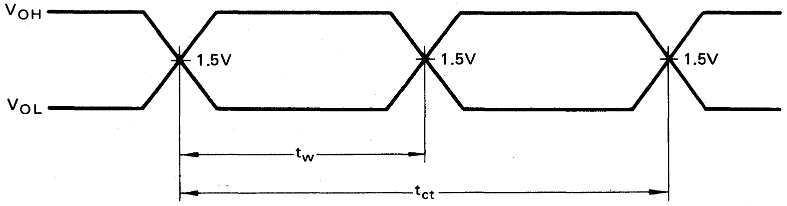
AC TEST CONDITIONS

Fig. 2 TTL OUTPUT LOAD CIRCUIT



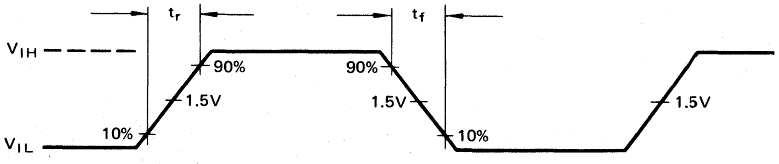
RL = 2kΩ
C_L = 15pF
(including jig capacitance)

Fig. 3 TTL OUTPUT WAVEFORM



Threshold voltage = 1.5V

Fig. 4 TTL INPUT WAVEFORM



V_{IH} = 3V, V_{IL} = 0V
$t_r = t_f$ = 10ns
Threshold voltage = 1.5V

AC CHARACTERISTICS (Cont'd)

AC TEST CONDITIONS (Cont'd)

Fig. 5 TXDATA± OUTPUT LOAD CIRCUIT

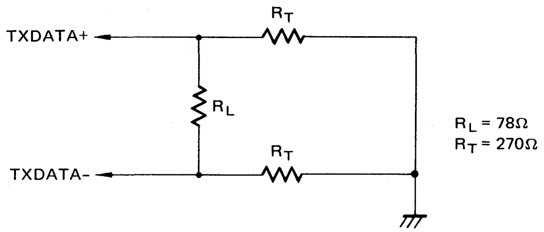


Fig. 6 TXDATA± OUTPUT WAVEFORM

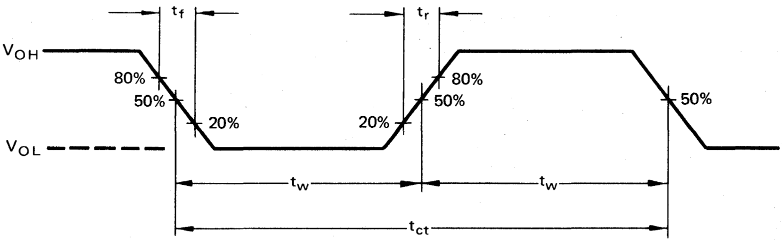
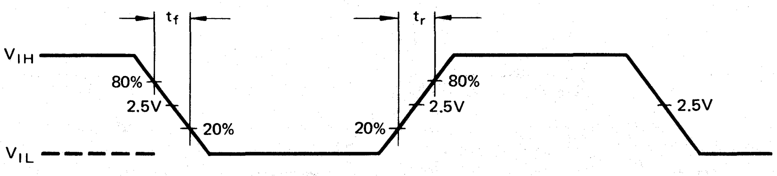


Fig. 7 RXDATA+, COL+ INPUT WAVEFORM



V_{IH} = 3.5V, V_{IL} = 1.5V
t_r= t_f = 2.0ns

RXDATA-, COL- Input voltage = 2.5V (DC)
$\overline{\text{DCLINK}}$ = 0V (DC coupling)

TYPICAL CHARACTERISTICS CURVES

Fig. 8

TXDATA±
Output Voltage vs. Output Current

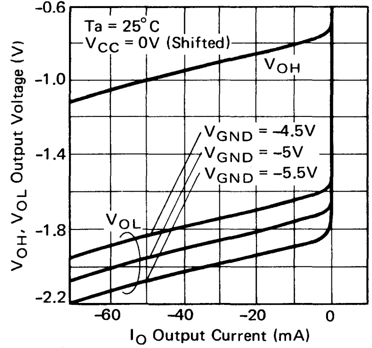


Fig. 9

RXDATA±, COL±
Input Current vs. Input Voltage

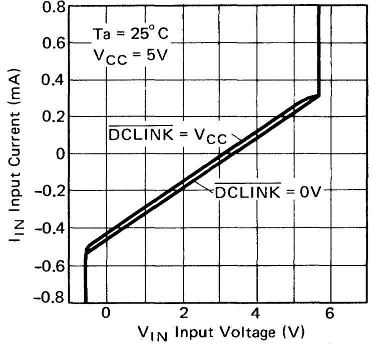


Fig. 10

TTL-OUTPUT
High Level Output Current vs.
High Level Output Voltage

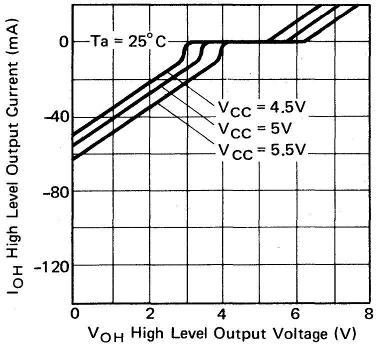


Fig. 11

TTL-OUTPUT
Low Level Output Current vs.
Low Level Output Voltage

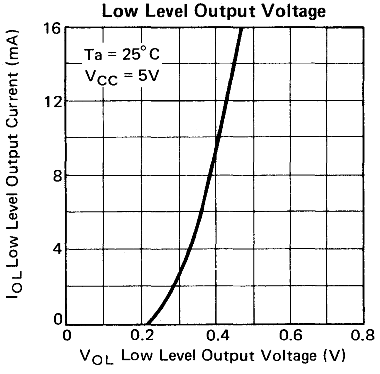


Fig. 12

TTL-INPUT
Input Current vs. Input Voltage

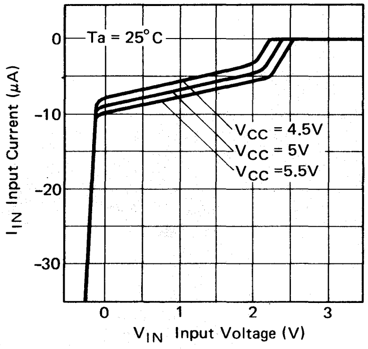


Fig. 13

OSC.IN
Input Current vs. Input Voltage

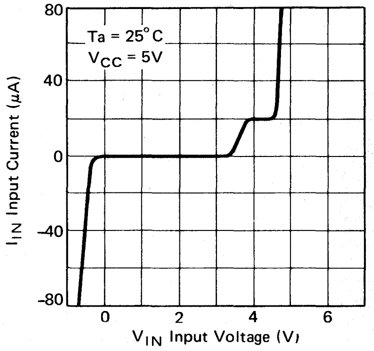


Fig. 14
COL± to XCOL TRANSFER (Receiver Threshold)
Output Voltage vs. Differential Input Voltage

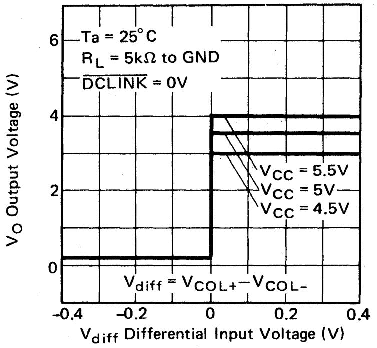


Fig. 15
COL± to XCOL TRANSFER (Receiver Threshold)
Output Voltage vs. Differential Input Voltage

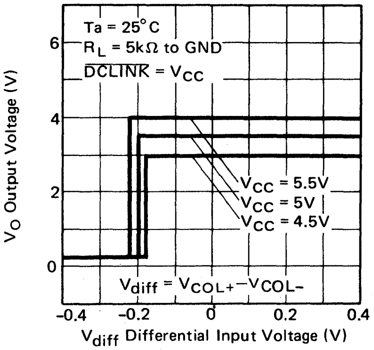


Fig. 16
TTL-INPUT THRESHOLD
TTL Input Threshold vs. Power Supply Voltage

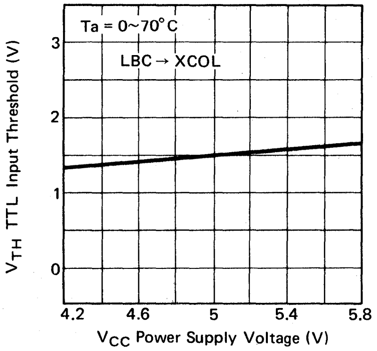


Fig. 17
RC to TXDATA- TRANSFER
Output Voltage vs. RC Input Voltage

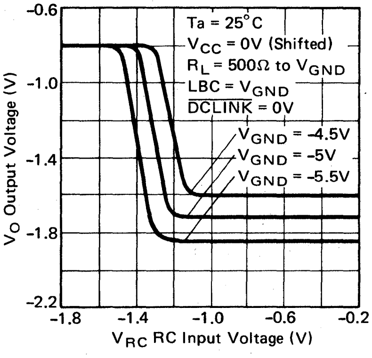


Fig. 18
TXDATA- LOW LEVEL HOLD TIME
TXDATA- Low Level Hold Time
TXDATA- Idling Rise Time **vs. RC Capacitance**

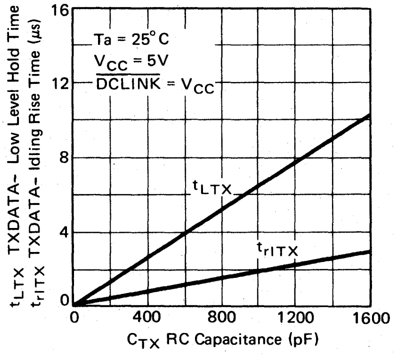
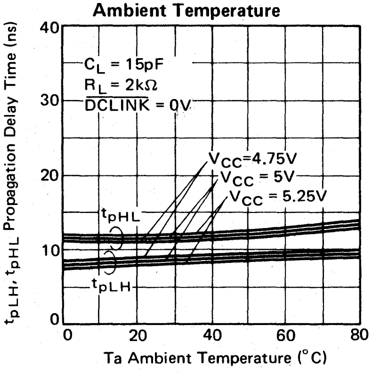
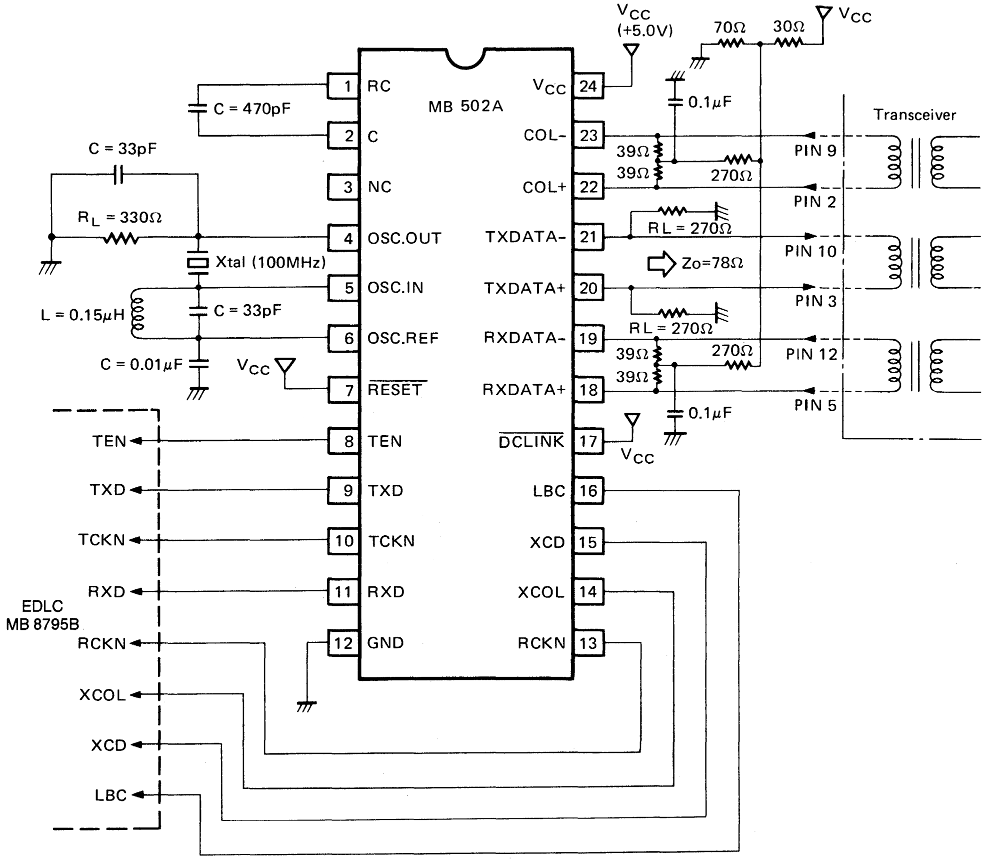


Fig. 19
COL± to XCOL PROPAGATION DELAY TIME
Propagation Delay Time vs.
Ambient Temperature



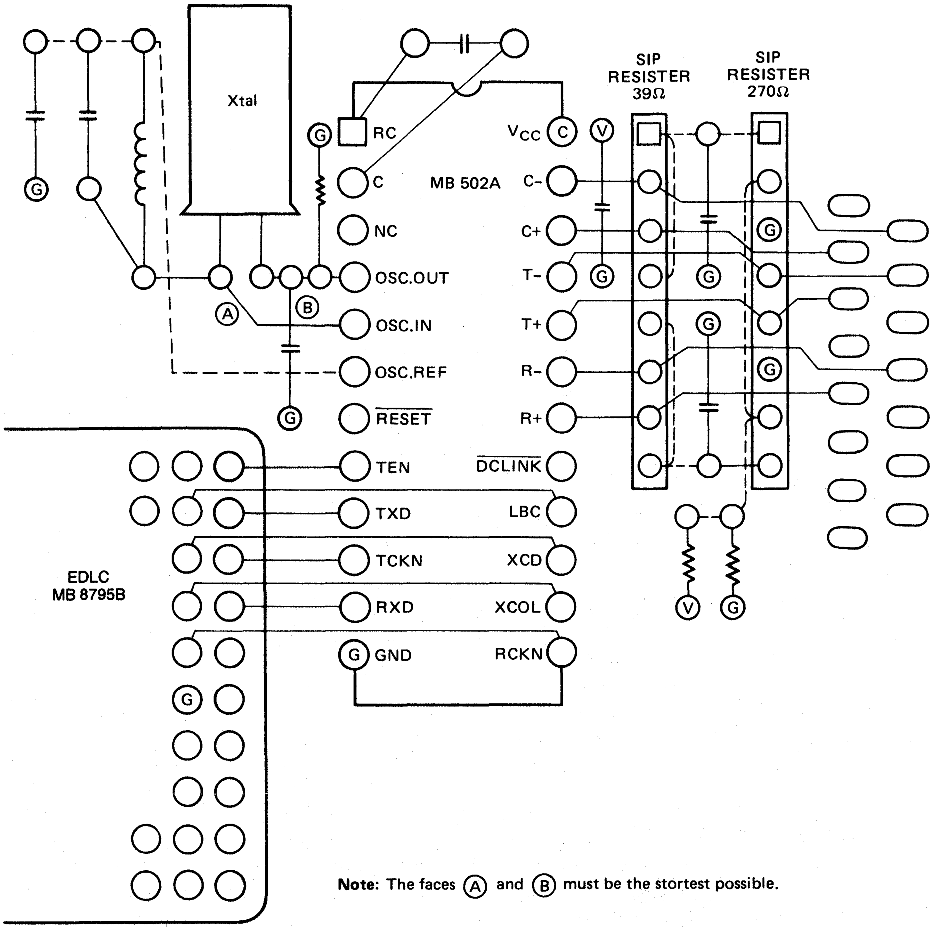
APPLICATION INFORMATION

Fig. 20 TYPICAL APPLICATION CIRCUIT



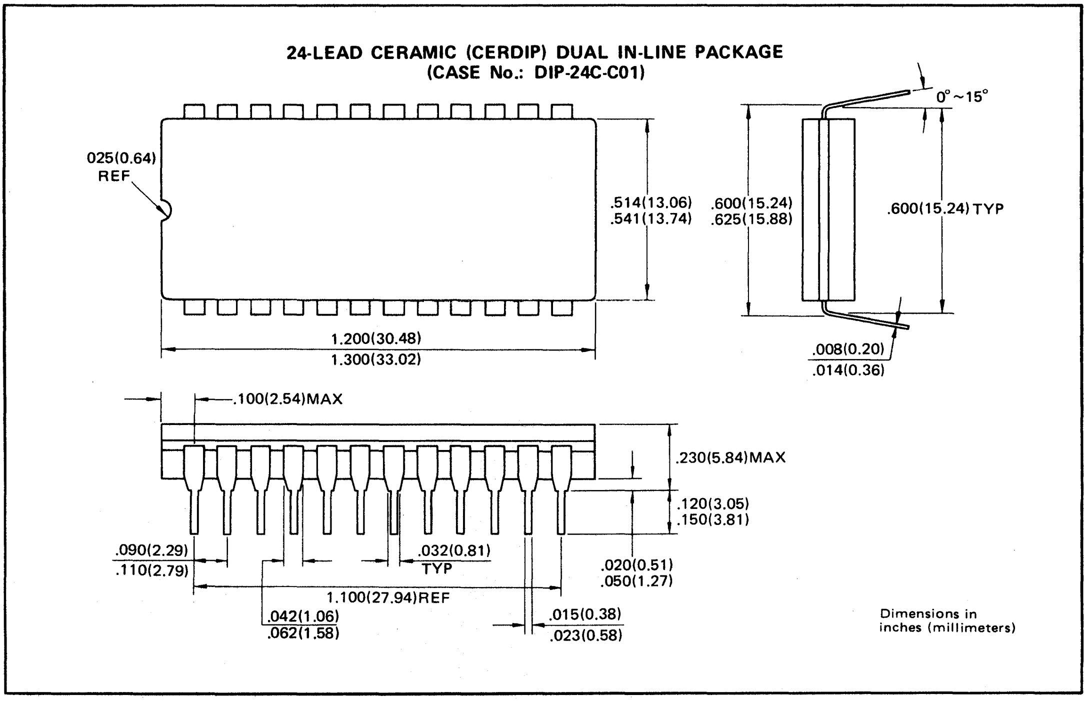
Note: 39Ω resistors must be balanced less than 1%.

Fig. 21 TYPICAL COMPONENT LAYOUT



Note: The faces Ⓐ and Ⓑ must be the stortest possible.

PACKAGE DIMENSIONS



Preliminary

Advanced Products

FUJITSU

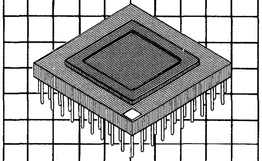
MB8795B
Ethernet Data Link Controller

Description

The Fujitsu MB8795B Ethernet Data Link Controller (EDLC) manufactured with Fujitsu's Advanced CMOS Technology, is designed for Ethernet* Local Area Network Systems and to be used with Fujitsu's MB502A Ethernet Encoder/Decoder (EED).

The MB8795B EDLC provides the user with a low power implementation of the Data Link Layer of the Ethernet Blue Book Specification. High throughput is possible via the separate data ports, while low cost implementations are also possible by tying the ports together.

The host system communicates with the MB8795B EDLC using the command and status registers accessed through the control port. Functions provided include complete transmit and receive control, and interrupt masking.



Ceramic Package
PGA-64C-A02

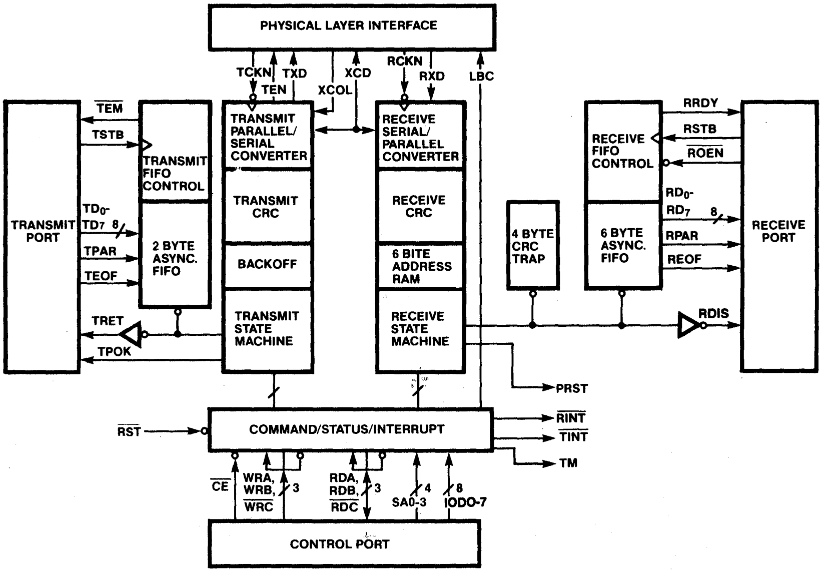
Features

- **Implementing Ethernet Blue Book Specification**
- **Function to generate and remove preamble and CRC**
- **Conversion between serial and parallel Data**
- **Four modes of address recognition**

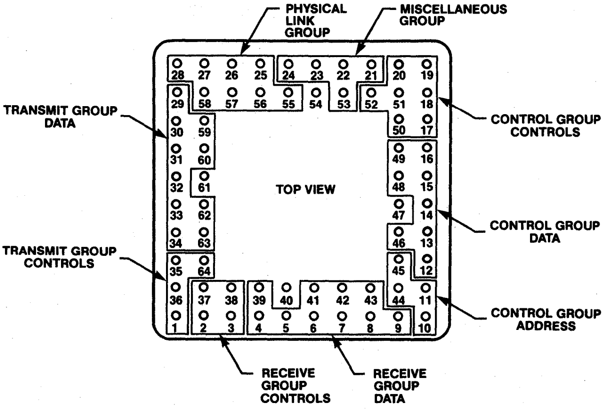
  Accept no packet, Physical Address/Multicast-group Address/Broadcast Address, Physical Address/Multicast Address, Accept all packets
- **Random exponential backoff to recover from collisions**
- **Three separate data ports providing flexible interface; Transmit, Receive, Control Ports**
- **Optional parity check on transmit byte stream**
- **Odd parity generated for receive byte stream**
- **Low power, advanced silicon gate CMOS technology**
- **Space saving 64-pin pin grid array package**

Note: *Ethernet is a trademark of Xerox Corp.

Block Diagram



Pin Assignment



Pin Assignment
(Continued)

PIN No.	I/O	Pin Name	PIN No.	I/O	Pin Name	PIN No.	I/O	Pin Name	PIN No.	I/O	Pin Name
1	O	$\overline{\text{TEM}}$	17	I	$\overline{\text{WRC}}$	33	I	TD2	49	I/O	IOD6
2	O	RRDY	18	I	WRB	34	I	TD0	50	I	RDA
3	I	RSTB	19	I	$\overline{\text{CE}}$	35	O	TPOK	51	I	RDB
4	O	RD0	20	I	WRA	36	I	TSTB	52	I	$\overline{\text{RDC}}$
5	O	RD2	21	O	$\overline{\text{TINT}}$	37	O	RDIS	53	I	$\overline{\text{RST}}$
6	O	RD3	22	O	$\overline{\text{RINT}}$	38	I	$\overline{\text{ROEN}}$	54	V_{SS}	GND
7	O	RD5	23	O	PRST	39	O	RD1	55	I	RCKN
8	O	RD7	24	O	TM	40	V_{SS}	GND	56	I	XCOL
9	O	RPAR	25	I	RXD	41	O	RD4	57	I	XCD
10	I	SA1	26	I	TCKN	42	O	RD6	58	O	LBC
11	I	SA3	27	O	TXD	43	O	REOF	59	I	TEOF
12	I/O	IOD0	28	O	TEN	44	I	SA0	60	I	TD6
13	I/O	IOD2	29	I	TPAR	45	I	SA2	61	V_{DD}	V_{CC}
14	I/O	IOD3	30	I	TD7	46	I/O	IOD1	62	I	TD3
15	I/O	IOD5	31	I	TD5	47	V_{DD}	V_{CC}	63	I	TD1
16	I/O	IOD7	32	I	TD4	48	I/O	IOD4	64	O	TRET

Absolute Maximum Ratings

		Value		
Rating	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	GND - 0.3*	7.0	V
Input and Output Voltage	V_I, V_{OUT}	GND - 0.3*	V_{CC} + 0.3*	V
Storage Temperature	T_{STG}	-55	150	°C
Operating Temperature	T_{OP}	0	70	°C

Note: *0.3 V is for stable state. For transit state, 0.5 V is allowed. (20 to 30 nsec.)

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Capacitance
(T_A = 25°C, V_{CC} = V_I = GND = 0V, f = 1 MHZ

		Value			
Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}			8	pF
Output Capacitance	C_{OUT}			8	pF
Bus Capacitance	$C_{I/O}$			12	pF

Recommended Operating Conditions

		Value			
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_{OP}	0		70	°C

DC Characteristics

		Value			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current (For Stable State; V_{IH} = V_{CC}, V_{IL} = GND)	I_{CC}	0		0.1	mA
Output High Voltage (I_{OH} = -0.4mA)	V_{OH}	4.0		V_{CC}	V
Output Low Voltage (I_{OL} = 2mA)	V_{OL}	GND		0.4	V
Input High Voltage	V_{IH}	2.2			V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current (V_I = 0V to V_{CC})	I_{LI}	-10		10	μA
Input Leakage Current for Bus Pins (V_I = 0V to V_{CC})	I_{LZ}	-40		40	μA

AC Characteristics

Control Register Read Timing

		Value			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Read Pulse Width	t_{RW}	35			ns
Read Address Pulse Width	t_{RAW}	35			ns
Read Access Time (C_L = 80 pF)	t_{RA}			110	ns
Read Address Access Time (C_L = 80 pF)	t_{RAA}			150	ns
Read Turn-off Delay Time (C_L = 80 pF)	t_{RZ}	10			ns
Read Address Turn-off Delay Time (C_L = 80 pF)	t_{RAZ}	20			ns
Address Register Read Access Time (C_L = 80 pF)	t_{ARRA}			300	ns
Address Register Read Address Turn-off Delay Time (C_L = 80 pF)	t_{ARRAZ}	20			ns
Address Register Read Address Setup Time	t_{ARRAS}	15			ns
Address Register Read Address Hold Time	t_{ARRAH}	90			ns

Control Register Write Timing

		Value			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Write Pulse Width	t_{WW}	35			ns
Write Address Set-up Time	t_{WAS}	30			ns
Write Data Set-up Time	t_{WDS}	15			ns
Write Address Hold Time	t_{WAH}	40			ns
Write Data Hold Time	t_{WDH}	80			ns
Test Pin Delay Time (CL = 50 pF)	t_T			150	ns
Transmit Status Register Reset Delay Time (C_L = 50 pF)	t_{TS}			150	ns
Receive Status Register Reset Delay Time (C_L = 50 pF)	t_{RS}			150	ns
Reset Register Reset Delay Time (C_L = 50 pF)	t_R			220	ns

AC Characteristics
(Continued)

Transmit Timing

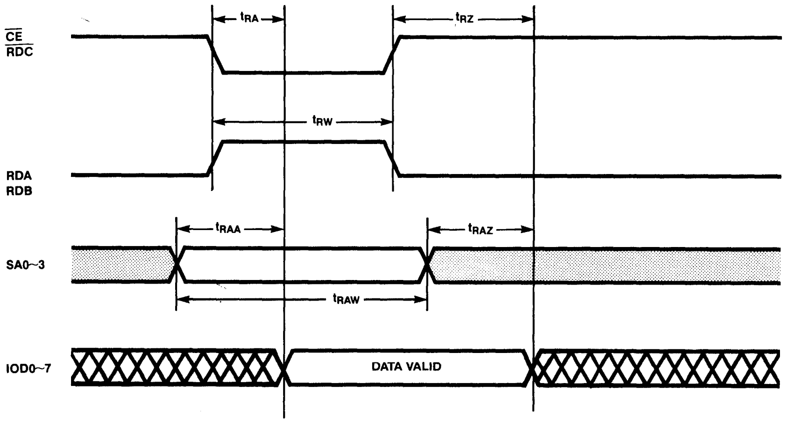
Parameter	Symbol	Value Min.	Typ.	Max.	Unit
TSTB Pulse Width	t_{TSTBW}	35			ns
TCKN Pulse Width	t_{TCKNW}	35			ns
TCKN Frequency	f_{TCKN}			10.2	MHz
Transmit Data Set-up Time	t_{TDS}	20			ns
Transmit Data Hold Time	t_{TDH}	25			ns
$\overline{\text{TEM}}$ Delay Time High (C_L = 50 pF)	t_{TEMH}			100	ns
$\overline{\text{TEM}}$ Delay Time Low (C_L = 50 pF)	t_{TEML}			150	ns
TEM Delay Time Low (Sync.) (C_L = 50 pF)	t_{TEMLS}			170	ns
TEN Delay Time (C_L = 50 pF)	t_{TEN}			55	ns
TXD Delay Time (C_L = 50 pF)	t_{TXD}			70	ns
TPOK Delay Time (C_L = 50 pF)	t_{TPOK}			150	ns
$\overline{\text{TRET}}$ Delay Time (C_L = 50 pF)	t_{TRET}			140	ns
TINT Delay Time (Transmit) (C_L = 50 pF)	t_{TINTT}			160	ns

Receive Timing

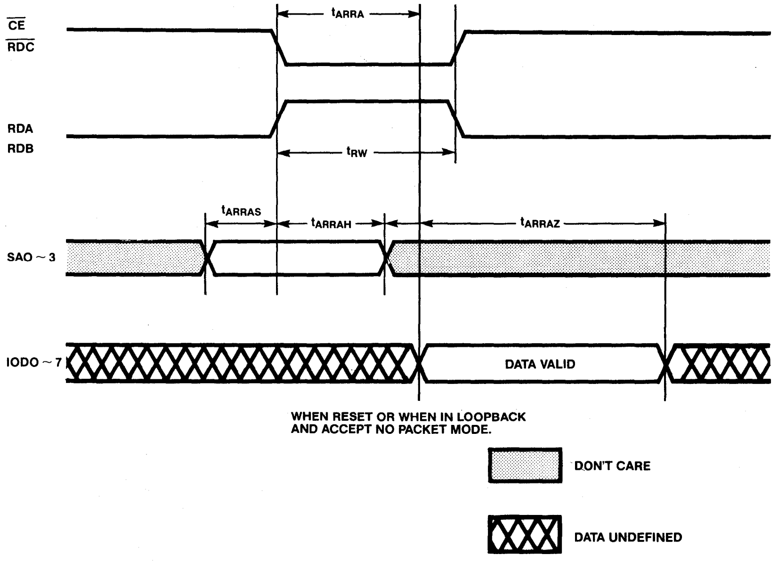
Parameter	Symbol	Value Min.	Typ.	Max.	Unit
RCKN Pulse Width	t_{RCKNW}	35			ns
RCKN Frequency	f_{RCKN}			10.2	MHz
$\overline{\text{RSTB}}$ Pulse Width	t_{RSTBW}	35			ns
ROEN Pulse Width	t_{ROENW}	35			ns
Receive Data Set-up Time	t_{RDS}	20			ns
Receive Data Hold Time	t_{RDH}	10			ns
RRDY Delay Time High (Sync.) (C_L = 50 pF)	t_{RRDYHS}			650	ns
Receive Data Delay Time (Sync.) (C_L = 50 pF)	t_{RDDS}			650	ns
RRDY Delay Time High (C_L = 50 pF)	t_{RRDYH}			100	ns
RRDY Delay Time Low (C_L = 50 pF)	t_{RRDYL}			65	ns
Receive Data Delay Time (C_L = 50 pF)	t_{RD}	10		100	ns
$\overline{\text{ROEN}}$ Access Time (C_L = 50 pF)	t_{ROENA}			80	ns
ROEN Turn-off Delay Time (C_L = 50 pF)	t_{ROENZ}	10			ns
RDIS Delay Time (C_L = 50 pF)	t_{RDIS}			120	ns
$\overline{\text{PRST}}$ Delay Time (C_L = 50 pF)	t_{PRST}			120	ns
$\overline{\text{RINT}}$ Delay Time (C_L = 50 pF)	t_{RINT}			160	ns
TINT Delay Time (Rcv) (C_L = 50 pF)	t_{TINTR}			190	ns

Timing Diagram

Control Register Read
Registers 0~7, F



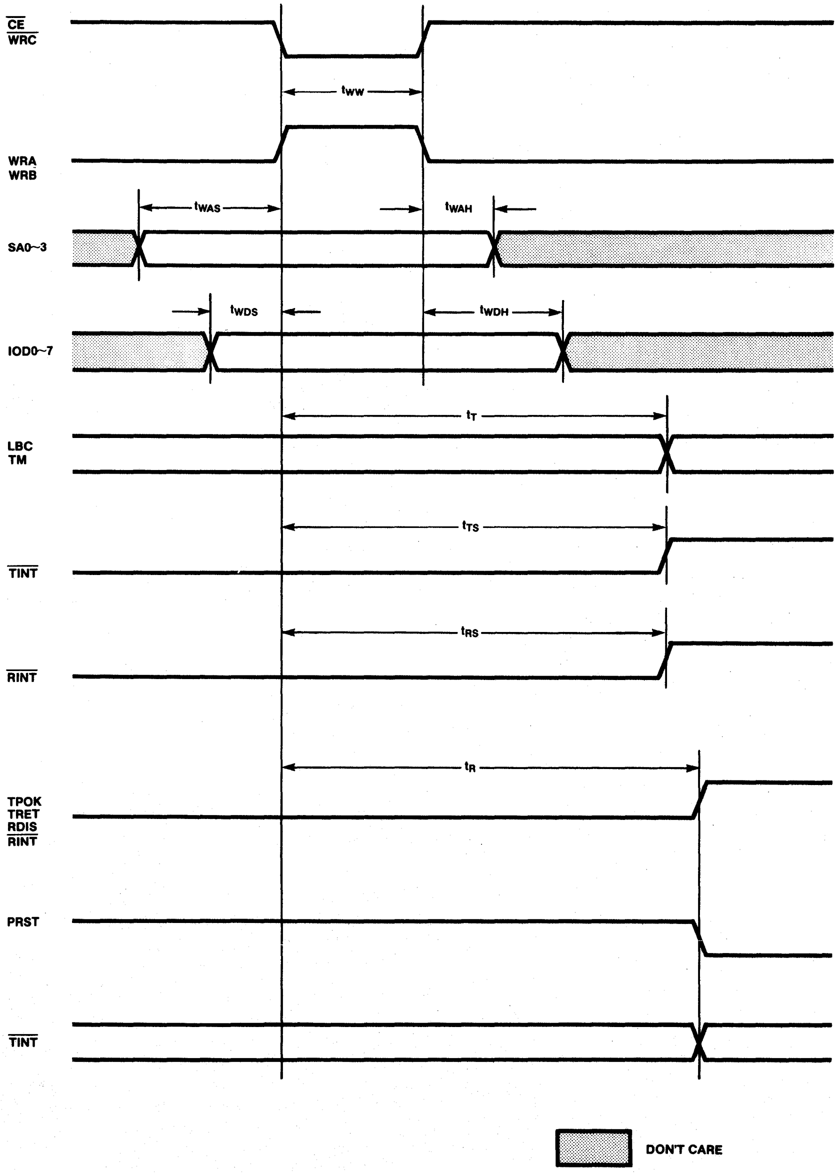
Address Registers 8~D



WHEN RESET OR WHEN IN LOOPBACK
AND ACCEPT NO PACKET MODE.

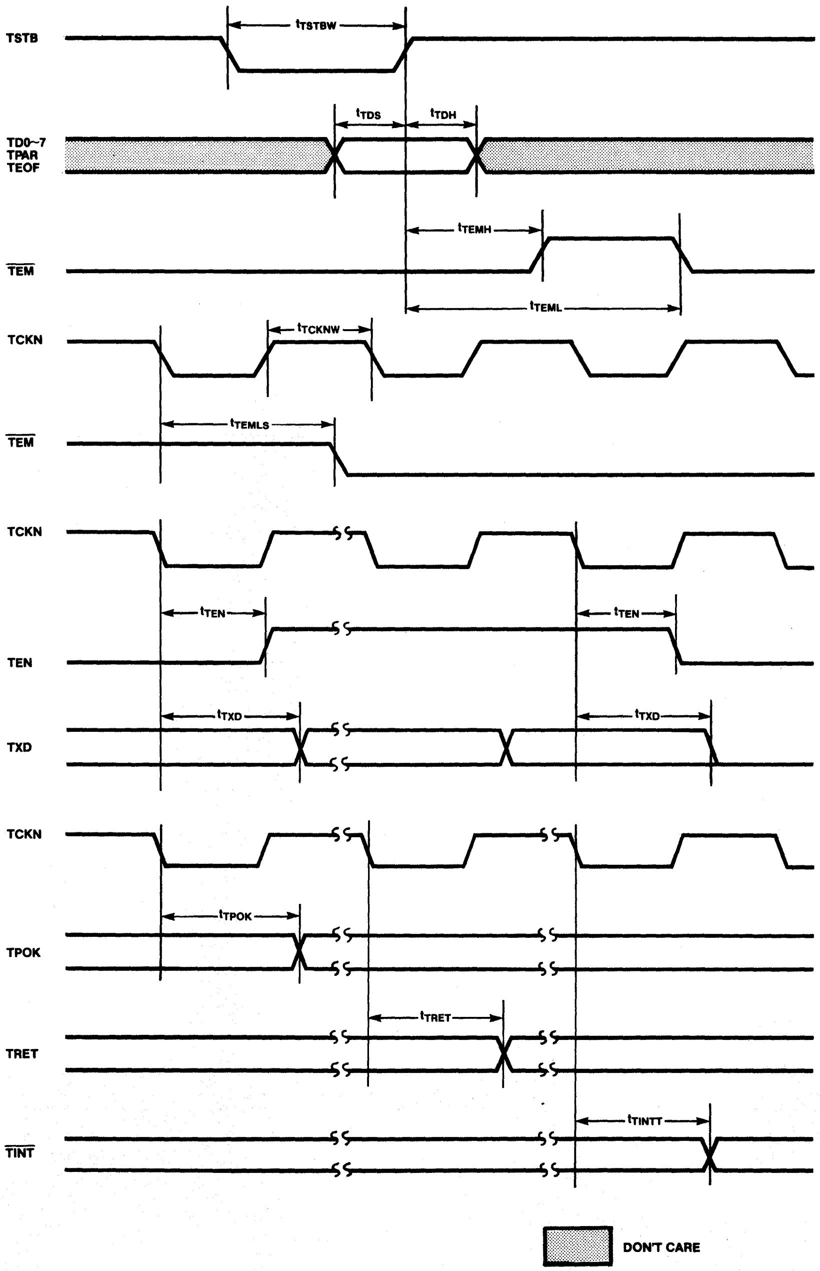
Timing Diagram
(Continued)

Control Register Write



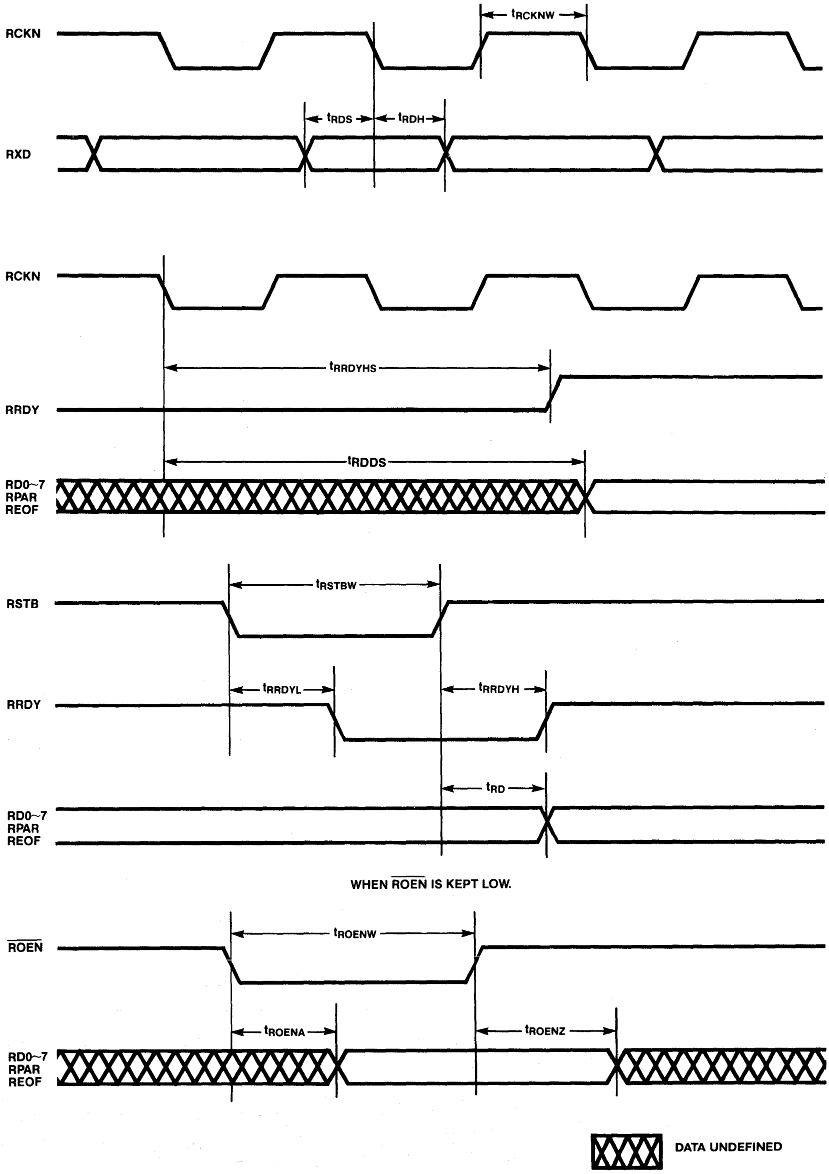
Timing Diagram
(Continued)

Transmit



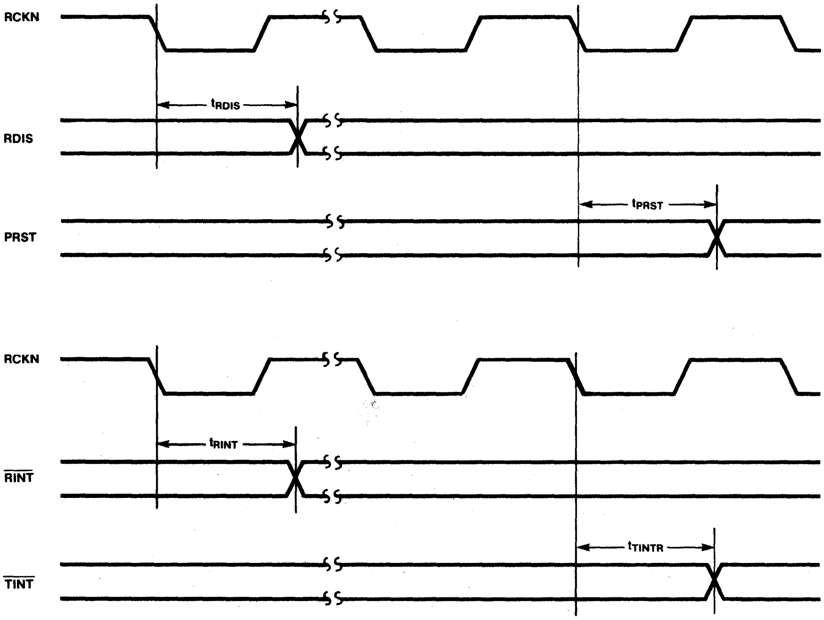
Timing Diagram
(Continued)

Receive



Timing Diagram
(Continued)

Receive (Continued)



Functional Description

The MB8795B EDLC is designed as two distinct sections, a transmitter and a receiver. Each section provides a small amount of asynchronous buffering, provisions for byte parity (which can be ignored), preamble generation/stripping, CRC generation/checking, and conversion between serial and parallel data. In addition, the transmitter provides contention resolution by means of binary exponential backoff. Finally, the receiver provides various modes of address recognition.

Transmitter

The block diagram on page 2 shows the various functions the transmitter performs.

Asynchronous FIFO

A two-byte FIFO provides a minimum amount of elastic buffering for the transmit byte data. Two signals are used for the byte controls. The first signal, TEM, indicates that the input register is full. The second signal, TSTB, is the input register data strobe. On the rising edge of this strobe input, the eight data bits, the parity bit and the 'end of frame' (TEOF) bit are latched into the input register. Strobes are ignored while the register is full.

The TRET signal indicates that a collision has occurred and that the packet in progress should be restarted. The buffer management would typically flush any buffers and reset its pointers to the beginning of the packet. Note that on the block diagram the asynchronous FIFO is cleared by this signal.

The TPOK signal indicates that successful transmission of the packet has been completed and the transmitter is ready for the next packet. This signal goes high when transmission of the packet is complete.

Note: The TPOK signal remains low long enough after the last byte is strobed into the FIFO, so the FIFO can be emptied and the CRC appended. Therefore the buffer management must remain prepared to reset its pointers in the case of a late collision.

Transmit Parallel/Serial Conversion

This section has a shift register for parallel to serial data conversion, a preamble generator, and a sychronization circuit for the collision and carrier detect signals. Also included is the optional 'ODD' parity check that is performed on the byte data supplied to the CRC generator. The parity check provides added security against internal chip failures due to undetected bad data transmissions.

Transmit CRC

The 32-bit CRC generator as defined in the Ethernet Specification.

Backoff

A pseudo-random number generator (17-bits), clocked at the bit rate so that distances between stations becomes part of the randomizing function, is sampled at the time of collision and counted down at the slot-time rate (512-bits) defined in the Ethernet specification, which provides a binary exponential backoff from collisions.

Transmitter State Machine

The state machine provides the major sequencing of events for the transmitter including idle, preamble, data, CRC, interframe gap, jam, and backoff. It also provides indicators for various error conditions.

Receiver

Refer to the block diagram for the relation of the sections. (See page 2).

Asynchronous FIFO

A six byte FIFO is provided so that when in diagnostic mode a minimum size packet (6 byte destination address and 4 byte CRC) can be received even in systems where the buffer management is half duplex. The data, parity and 'end of frame' bit are tri-stated with signal ROEN, a low true enable. The 'receive byte ready' (RRDY) indicates a byte is available to the host system. RSTB is a low true clock whose falling edge causes RRDY to be false and whose rising edge causes the data in the register to be removed. See the timing charts for further clarification.

CRC Trap

All received bytes are delayed by four bytes so that the last bytes of the received packet (CRC) can be removed. After four bytes are received the trap will put one byte into the asynchronous FIFO for each subsequent byte received, thereby always maintaining four bytes in the trap. At the 'end of frame' the four bytes in the trap are the CRC and they are never put into the asynchronous FIFO.

Receive Serial/Parallel Conversion

This section has a shift register for data serial to parallel conversion, a circuit to recognize the end of preamble, and an odd parity check circuit.

Receive CRC

The 32-bit CRC checking register and comparison logic as described in the Ethernet specification.

6 Byte Address RAM

A 48-bit storage RAM used for comparing with the Destination Address Field of the incoming packets (the first 48 bits after the preamble).

Receiver State Machine

The state machine provides the major sequencing through the receiver states including idle, address recognition, data, and holding as a discarded packet completes. It also provides indicators of various error conditions.

Functional Description
(Continued)

Command/Status/Interrupt

This section has fifteen registers, a register address decoder, and gating for interrupt conditions. Each register is one byte length. The host system communicates with the MB8795B EDLC using these registers accessed through the control port. Interrupt conditions are defined by setting the registers of Transmit Marks and Receive Masks.

Register Description

The Register in the MB8795B EDLC can be accessed via the control port with their address assigned by the signals SA0-3. (SA0 represents the LSB of the address.) The address signals SA0-3 are activated by both the chip enable signal $\overline{\text{CE}}$ and, write signals WRA, WRB, WRC, or, read signals RDA, RDB, RDC. A brief description of each register is given in the table below.

Register Description

			7	6	5	4	3	2	1	0
0	XMIT STATUS	RD	RDY For PKT	NET BUSY	XMIT RECVD	SHORTED	UNDERFLOW	COLL	16 COLL	PAR ERR
		WR	—	—	—	—	CLR UNDERFLOW	CLR COLL	CLR 16 COLL	CLR PAR ERR
1	XMIT MASKS	RD/WR	MASK STATUS 7	—	MASK STATUS 5	—	MASK STATUS 3	MASK STATUS 2	MASK STATUS 1	MASK STATUS 0
2	REC STATUS	RD	PKT OK	—	—	RESET PKT	SHORT PKT	ALIGN ERR	CRC ERR	OVERFLOW ERR
		WR	CLR PKT	—	—	—	CLR ERR	CLR ERR	CLR ERR	CLR ERR
3	REC MASKS	RD/WR	MASK STATUS 7	—	—	MASK STATUS 4	MASK STATUS 3	MASK STATUS 2	MASK STATUS 1	MASK STATUS 0
4	TMODE + COLL ATTEMPT	RD/WR	3	2	1	0	IGNORE PARITY	TM	LBC	DISABLE CONTNT
			Collision Attempts, Read Only							
5	RMODE	RD/WR	TST CRC	—	—	ADD SIZE	ENA SHORT PKT	ENA RST	ADD ENA1	ADD ENA0
6	RESET	Write Only	RESET	—	—	—	—	—	—	—
7	TDR1	Read Only	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0

Register Description
(Continued)

				7	6	5	4	3	2	1	0
48-Bit Ethernet Address	8	NODE IDO	RD/WR	8th BIT A.P.	7th BIT A.P.	6th BIT A.P.	5th BIT A.P.	4th BIT A.P.	3rd BIT A.P.	2nd BIT A.P.	1st BIT A.P.*
				First Byte After Preamble							
	9	NODE ID1	RD/WR	16th BIT A.P.	15th BIT A.P.	14th BIT A.P.	13th BIT A.P.	12th BIT A.P.	11th BIT A.P.	10th BIT A.P.	9th BIT A.P.
				Second Byte After Preamble							
	A	NODE ID2	RD/WR	24th BIT A.P.	23rd BIT A.P.	22nd BIT A.P.	21st BIT A.P.	20th BIT A.P.	19th BIT A.P.	18th BIT A.P.	17th BIT A.P.
				Third Byte After Preamble							
	B	NODE ID3	RD/WR	32nd BIT A.P.	31st BIT A.P.	30th BIT A.P.	29th BIT A.P.	28th BIT A.P.	27th BIT A.P.	26th BIT A.P.	25th BIT A.P.
				Fourth Byte After Preamble							
	C	NODE ID4	RD/WR	40th BIT A.P.	39th BIT A.P.	38th BIT A.P.	37th BIT A.P.	36th BIT A.P.	35th BIT A.P.	34th BIT A.P.	33rd BIT A.P.
				Fifth Byte After Preamble							
	D	NODE ID5	RD/WR	48th BIT A.P.	47th BIT A.P.	46th BIT A.P.	45th BIT A.P.	44th BIT A.P.	43rd BIT A.P.	42nd BIT A.P.	41st BIT A.P.
				Sixth Byte After Preamble							
	E	(RESERVED)		—	—	—	—	—	—	—	—
	F	TDR2	Read Only	—	—	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

*Multicast bit

Register Description
(Continued)

Transmit Status—Address 00H

This register indicates the status of the transmitter.

Bit 7

Read—Ready for Packet—A copy of the Transmit Packet Successful (TPOK) signal pin. For use in systems where the processor handles the transmit buffer management.

Write—no effect.

Bit 6

Read—Net Busy—A copy of the Receive Carrier Detect (XCD) input.

Write—no effect.

Bit 5

Read—Transmitted Packet was Received—Indicates that shortly after transmission was completed a good packet was received by the receiver. This is used to indicate self-reception of the packet, which allows the software to take advantage of the hardware address matching even in systems which are designed for half duplex operation. This bit is cleared as each transmission begins.

Write—no effect.

Bit 4

Read—Shorted—Set if the Receive Carrier Detect (XCD) stops during packet transmission. Either a collision or shorted coax can cause the bit to be set. This bit is cleared as each transmission begins. —Write—no effect.

Bit 3

Read—Underflow—Set when data to be transmitted is not available to the parallel to serial converter before the converter is empty. Transmission is aborted immediately while bytes will be accepted from the FIFO until an EOF is encountered.

Write—0, no effect; 1, clear the error condition.

Bit 2

Read—Collision—Set when a collision terminates transmission of a packet.

Write—0, no effect; 1, clear the error condition.

Bit 1

Read—16 Collisions—Set when the 16th collision for a single packet aborts transmission. Bytes are strobed through FIFO normally to discard the packet.

Write—0, no effect; 1, clear the error condition.

Bit 0

Read—Parity Error—Set when the parallel to serial converter detects a parity error in the data. If parity check is enabled transmission is aborted while the bytes continue to be strobed from the FIFO, until EOF.

Write—0, no effect; 1, clear the error condition.

Transmit Masks—Address 01H

The interrupt conditions which define the signal at TINT are defined by setting the bits of this register.

Bit 7—Rd/Wr—Gates 'Ready For Packet'
Bit 6—no bit, read as 0
Bit 5—Rd/Wr—Gates 'Transmit Received'
Bit 4—no bit, read as 0.
Bit 3—Rd/Wr—Gates 'Underflow'
Bit 2—Rd/Wr—Gates 'Collision'
Bit 1—Rd/Wr—Gates '16 Collisions'
Bit 0—Rd/Wr—Gates 'Parity Error'

Receive Status—Address 02H

This register indicates the status of the receiver.

Bit 7

Read—Packet OK—Set when CRC of a legal length packet received is correct.

Write—0, no effect; 1, clear the error condition.

Bit 6

not used

Bit 5

not used

Bit 4

Read—Reset Packet—Set when a packet is received successfully and the field type is 0900H. The bit is cleared at the beginning of the next packet reception. The bit is set only if the Node ID matches, not multicast or broadcast. Reset packets are recognized in any Address Match mode from NONE to PROMISCUOUS.

Write—no effect

Bit 3

Read—Short Packet—Set if a packet does not meet the minimum length requirements of the Ethernet specification.

Write—0, no effect; 1, clear condition.

Bit 2

Read—Alignment Error—Set if a packet has bad CRC at the last octet boundary and the number of bits are not divisible by eight.

Write—0, no effect; 1, clear condition.

Bit 1

Read—CRC Error—Set if the CRC does not verify at the end of the packet.

Write—0, no effect; 1, clear the error condition.

Bit 0

Read—Overflow—Set if the internal asynchronous FIFO is full when a byte is available from the serial to parallel converter.

Write—0, no effect; 1, clear error condition.

Register Description
(Continued)

Receive Masks—Address 03H

The interrupt conditions which define the signal at RINT are defined by setting the bits of this register.

Bit 7—Rd/Wr—Gates 'Packet OK'
Bit 6—no bit, read as 0.
Bit 5—no bit, read as 0.
Bit 4—Rd/Wr—Gates 'Reset Packet'
Bit 3—Rd/Wr—Gates 'Short Packet'
Bit 2—Rd/Wr—Gates 'Alignment Error'
Bit 1—Rd/Wr—Gates 'CRC Error'
Bit 0—Rd/Wr—Gates 'Overflow'

Transmit Mode—Address 04H

Bits 7-4

Read Only—Collision Attempts—Indicates the number of collisions occured before the last packet was sent (or aborted). This is a testing aid as the number is cleared at the beginning of a subsequent transmission.

Bit 3

Rd/Wr—Ignore Parity—if set this bit prevents the setting of the Parity Error condition.

Bit 2

Rd/Wr—TM—A bit whose complement is available as signal pin TM. Intended to control the power to the transceiver or any other function external to the chip.

Bit 1

Rd/Wr—LBC—A bit whose complement is available as signal pin LBC. Intended to control the loopback function of the Encoder/Decoder or any other function external to the chip.

Bit 0

Rd/Wr—Disable Contention—When this bit is set the transmitter disregards Receive Carrier Detect. This special function would only be used if the MB8795B EDLC were used in a two wire point to point link, in true full duplex operation. In this case the Collision Detect signal (a low level will inhibit the start of transmission) acts as carrier sense for the transmitter while collisions during transmissions are ignored.

Receive Mode—Address 05H

Bit 7

Rd/Wr—Test Mode—For chip testing this bit:

1) Inhibits the receiver from accumulating CRC. The last four bytes of a packet are shifted into the CRC register and checked without being modified.

2) Changes the backoff algorithm so that the pseudo-random number generator is disabled and the number to backoff becomes 2^{n-1} +1, where n is the number of collisions. Also, the slot time is reduced to one (1) byte.

Bit 6

not used.

Bit 5

not used.

Bit 4

Rd/Wr—Address Size—When set this bit reduces the Node ID address match to 5 bytes instead of the normal 6. This is used where the node is performing some multiplex function on the least significant byte of the destination address.

Bit 3

Rd/Wr—Short Packet Enable—For testing, when this bit is set the receiver will successfully receive any packet of ten (10) bytes or more. This function is used in half duplex systems for the loopback check and can be used by all testing programs to reduce testing time.

Bit 2

Rd/Wr—Reset Enable—When this bit is zero, the checking done for the special type field is disabled.

Bit 1-0

Rd/Wr—Address Match Mode—

- Mode 0—accept no packets
- Mode 1—accept Node ID packets, multicasts which match the first three bytes of the Node ID packets, and broadcast packets.
- Mode 2—accept Node ID packets, and all multicasts including broadcast of course
- Mode 3—promiscuous, accept all packets.

Reset—Address 06H

Bit 7

Write Only—Reset—This latch is writeable and will hold the device in the reset state while set. It is set by the external reset pin RST being low. After power up the software should first initialize all the modes and masks, and then clear the reset.

Bit 6-0

not used

TDR LSB—Address 07H

Bits 7-0

Read Only—contains the least significant 8 bits of the TDR register which counts how many bits were successfully transmitted. Counting stops on collision or drop of carrier. Count is reset with each transmission.

Node ID—Addresses 10-15H

These 6 bytes are Rd/Wr and represent the address against which th frame addresses are matched during Address Match Modes 1 and 2. Bit 0 of address 10H is equivalent to the multicast bit.

TDR MSB—Address 17H

Bits 7-6

not used

Bits 5-0

Read Only—Contains the most significant six bits of the TDR register which was described above.

Register Description
(Continued)

Interface Signal Description

Power Group

V_{CC}—+5V power supply (two pins)

GND—ground (two pins)

Control Group

$\overline{CE}$ (Chip enable, low active input)

This active low signal gates all control port reads and writes.

RDA,RDB,$\overline{RDC}$ (Control read, inputs)

These two active high and one active low signals are ANDed with $\overline{CE}$ to form read signals inside the MB8795B EDLC.

WRA,WRB,$\overline{WRC}$ (Control write, inputs)

These two active high and one active low signals are ANDed with $\overline{CE}$ to form write strobes inside the MB8795B EDLC. One of the signals is intended to be a clock so that address, data, and other controls will be stable when the internal write is active.

SA0-3 (Control port address, input)

These four signals address the 16 possible registers of the MB8795B EDLC. SA0 is the least significant bit of the address.

IOD0-7 (Control port data, 3-state outputs and inputs)

These eight signals are the bi-directional data used to read and write the 16 possible internal registers of the MB8795B EDLC.

Transmit Group

TD0-7 (Transmit data bytes, inputs)

Eight bits of data to be transmitted.

TPAR (Transmit data parity, input)

Optional parity accompanying the transmit byte data.

TEOF (Transmit data end of frame, input)

Required data bit which signals the last byte of the frame. After the byte having this bit is sent, CRC transmission will start.

$\overline{TEM}$ (Transmit byte register not empty, output)

Indicates that the asynchronous FIFO has no room for a byte.

TSTB (Transmit byte register strobe, positive edge-trigger input)

Strobes the transmit data into the asynchronous FIFO.

TRET (Transmit packet - retransmit packet, output)

Indicates that a collision or underflow has occurred. Buffer management logic should discard any remaining bytes of the current packet and then restart transmission of the packet.

TPOK (Transmit packet successful, output)

Indicates to the buffer management that it will not be required to retransmit the current packet again and thus can proceed to the next packet.

Receive Group

RD0-7 (Receive data bytes, 3-state outputs)

Eight bits of data being received.

RPAR (Receive data parity, 3-state output)

Odd parity computed on the incoming data stream.

REOF (Receive data end of frame, 3-state output)

A tenth data bit which accompanies the last byte of the frame, which is only present if reception was successful. Successful reception means that a packet had good CRC, appropriate length and an address match in the current mode.

$\overline{ROEN}$ (Receive byte output enable, low active input)

3-state enable for the ten data bits above. This allows multiplexing the receive data port with the transmit and control ports in low cost systems.

RRDY (Receive byte ready, output)

Indicates that a byte is available at the output of the async FIFO.

RSTB (Receive byte strobe, positive edge trigger input)

Strobes the receive data out of the async FIFO to the host system.

RDIS (Receive packet discard, output)

Indicates that the bytes received so far should be discarded because of bad address, bad length or bad CRC. This signal and the REOF output are mutually exclusive.

Physical Link Group

RCKN (Receive data clock, negative edge trigger input)

This signal is generated by the Ethernet Encoder/Decoder (EED) MB502A. It is a strobe frequency source for the receive bit clock and is used to strobe RXD.

RXD (Receive serial data, input)

Decoded data from the MB502A EED.

TCKN (Transmit data clock, negative edge trigger input)

Generated by the MB502A EED as a strobe frequency source for the transmit bit clock.

TEN (Transmit encode enable, output)

High true enable for Manchester encoding. This signal is strobed and stable at the same time as TXD.

TXD (Transmit serial data, output)

Serial data to be encoded onto the Ethernet Coax. Gated by TEN

XCD (Receive carrier detect, input)

Carrier detect signal of the decoder. Used by the receiver as data gate and by the transmitter as contention information.

Register Description
(Continued)

XCOL (Collision presence, input)

A TTL copy of the Collision presence pair of the transceiver cable. The idle state is indicated by a logic "1" and the collision is indicated by a 10 MHz square wave.

LBC (Loopback Control, output)

A copy of a software setable latch used to command the MB502A EED to operate in Loopback mode.

Misc. Group

PRST (Packet reset, output)

Indicates that a complete and legal packet of type 0900H was received. This is intended to be used as a remote reset function.

$\overline{\text{RINT}}$ (Receive interrupt, output)

A logic "0" indicates the receiver interrupt condition coincides with its corresponding mask bit.

$\overline{\text{TINT}}$ (Transmitter interrupt, output)

Same as $\overline{\text{RINT}}$ for transmitter interrupt.

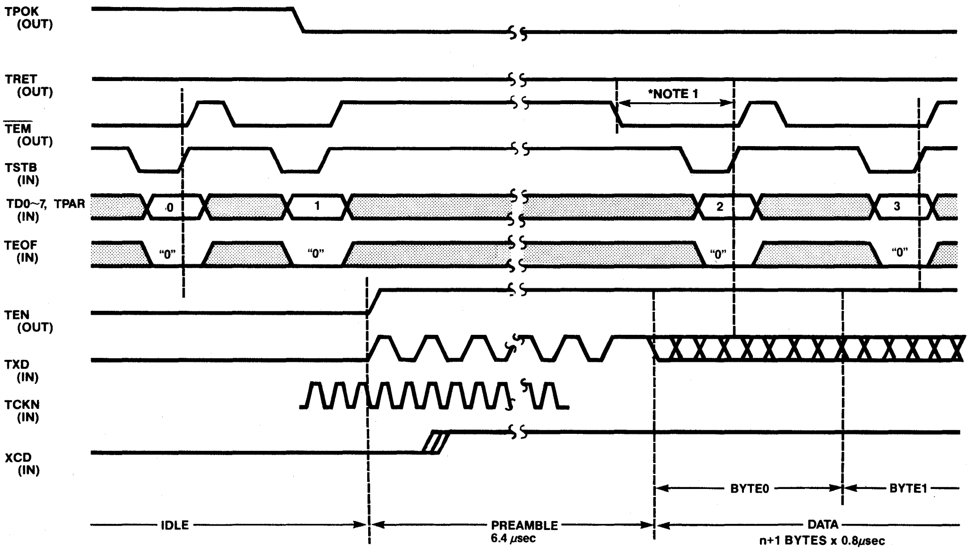
$\overline{\text{RST}}$ (Reset, low active input)

TM (Test mode, output)

A copy of a software loadable latch. Intended to control a circuit to turn the Transceiver power on and off.

Timing Diagram

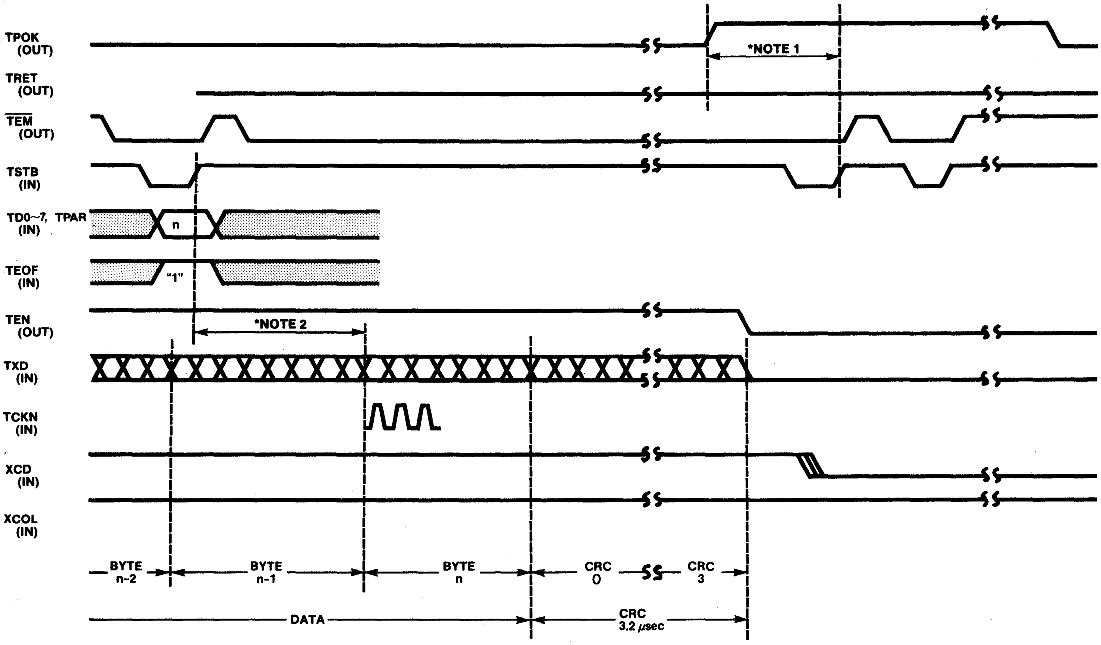
Transmit Good Packet (1)



***Note 1:** This period could be as great as 1½ byte times.

Timing Diagram
(Continued)

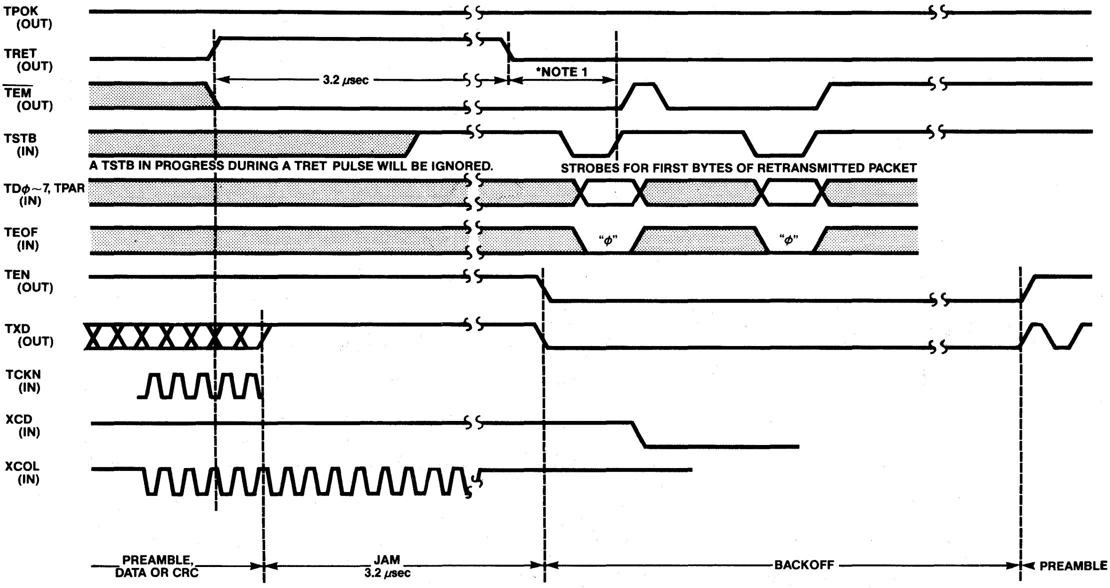
Transmit Good Packet (2)



*Note 1: Must be less than ≈ 5.0 μ sec. to guarantee minimum packet spacing.
*Note 2: This could be ½-2½ byte times.

Timing Diagram
(Continued)

Transmit Collision—First Fifteen Collisions only



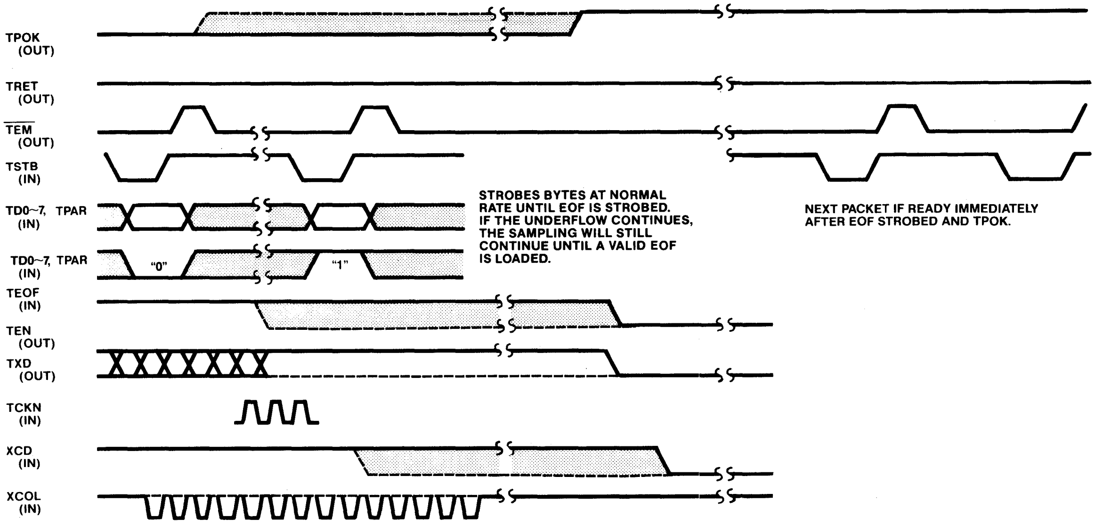
TRANSMIT 16TH COLLISION, PARITY ERROR, UNDERFLOW ERROR
- SOLID LINES INDICATE 16TH COLLISION.
- DOTTED LINES INDICATE PARITY ERROR OR UNDERFLOW ERROR.

***Note 1:** Must be less than ≈ 5.0 μ sec. to guarantee minimum backoff time.

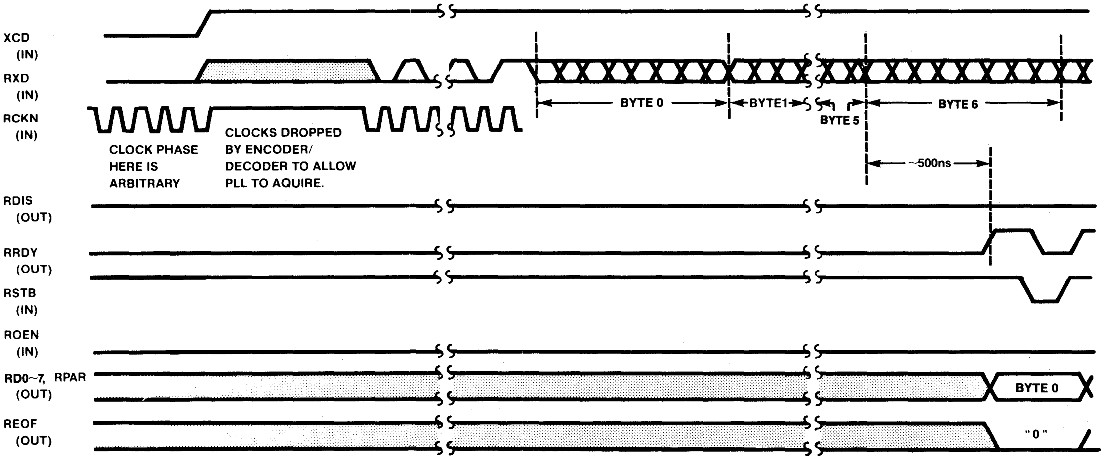
Timing Diagram
(Continued)

Transmit 16th Collision, Parity Error, Underflow Error

- Solid lines indicate 16th collision.
- Dotted lines indicate parity error or underflow error.

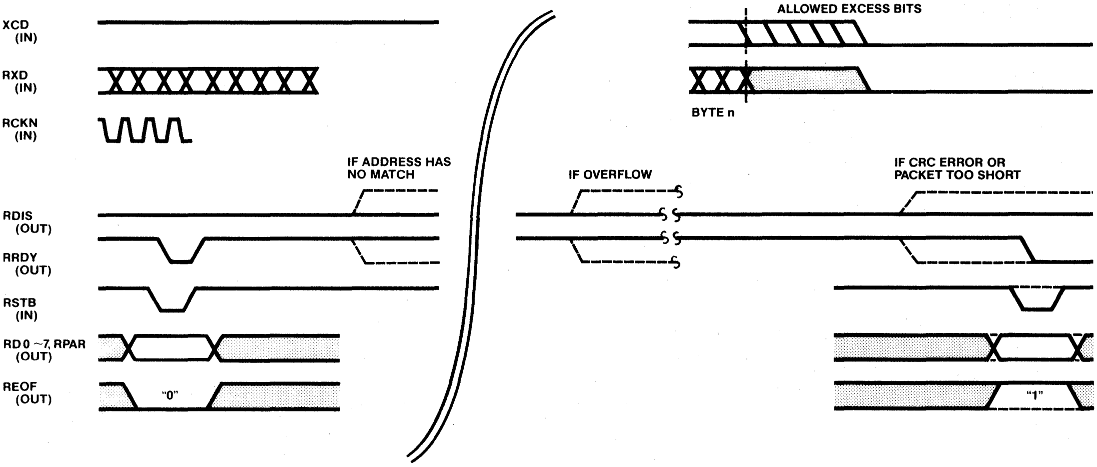

TPOK (OUT)
TRET (OUT)
TEM (OUT)
TSTB (IN)
TD0~7, TPAR (IN)
TD0~7, TPAR (IN)
"0"
"1"
TEOF (IN)
TEN (OUT)
TXD (OUT)
TCKN (IN)
XCD (IN)
XCOL (IN)
STROBES BYTES AT NORMAL RATE UNTIL EOF IS STROBED. IF THE UNDERFLOW CONTINUES, THE SAMPLING WILL STILL CONTINUE UNTIL A VALID EOF IS LOADED.
NEXT PACKET IF READY IMMEDIATELY AFTER EOF STROBED AND TPOK.

Receive

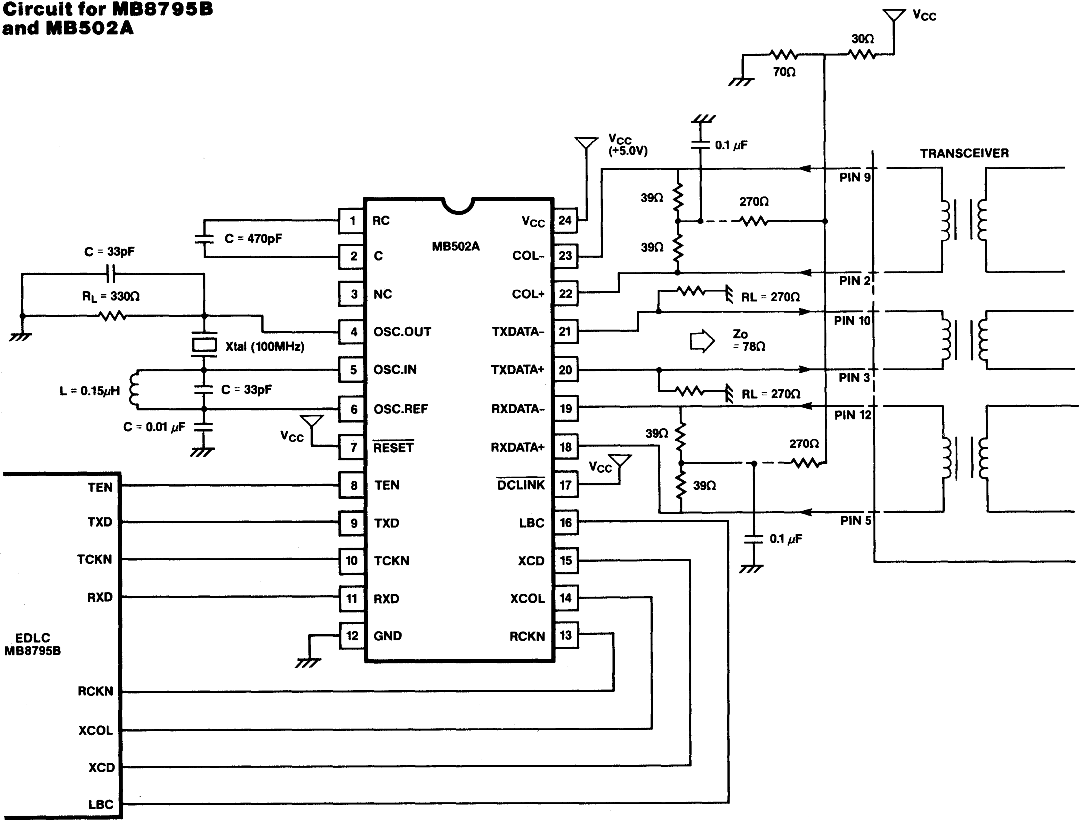


Timing Diagram
(Continued)

Receive—Address Mismatch, Overflow Error, CRC Error, Packet Length Error

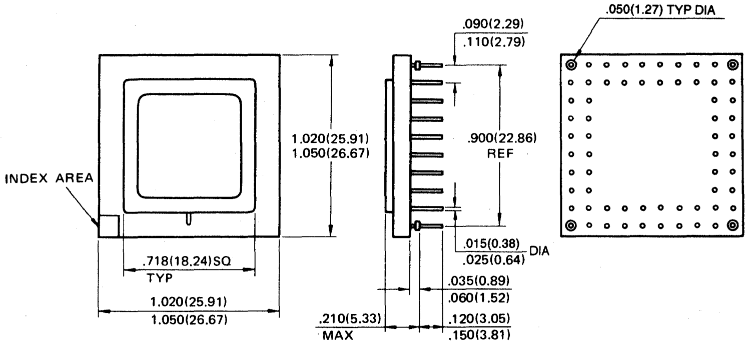


Typical Application Circuit for MB8795B and MB502A



Package Dimensions
Dimensions in inches
(millimeters)

64-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE (CASE No.: PGA-64C-A02)



Section 6

Signal Processors and Peripherals

FUJITSU

GENERAL PURPOSE DIGITAL SIGNAL PROCESSOR

MB 8764

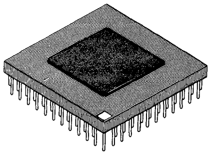
December 1985
Edition 2.0

GENERAL PURPOSE DIGITAL SIGNAL PROCESSOR

The Fujitsu MB 8764 is a general purpose silicon-gate CMOS digital signal processor (DSP) integrated circuit. The MB 8764 features a high-speed pipelined multiplier, supports concurrent operations with compound instructions and multiple data paths, offers flexible and expandable memory options and has an on-chip DMA channel.

With its high-speed operation, the MB 8764 gives high throughput in various applications, such as telecommunications, signal processing and image processing.

Being packaged in the 88-pin pin grid array, the MB 8764 allows a complex system to be built with the external program ROM and data RAM accessed through dedicated address and data buses.

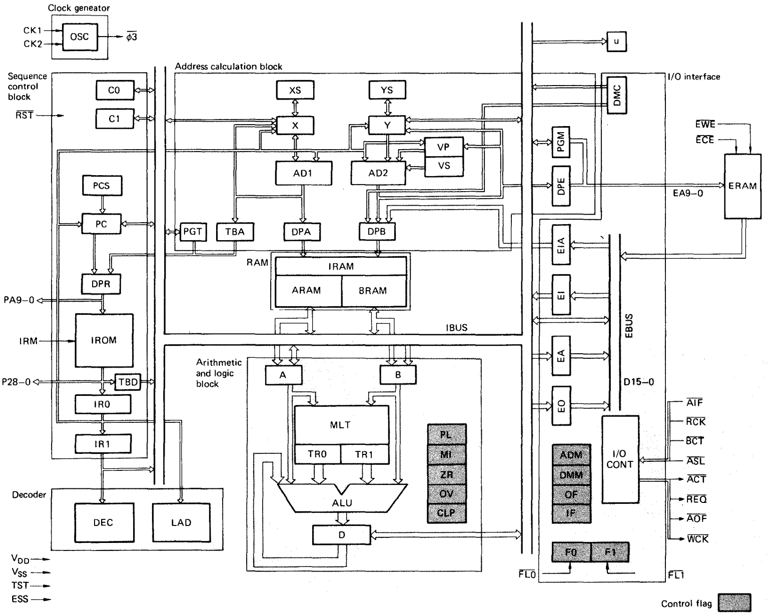


CERAMIC PACKAGE
RIT-88C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

- General purpose high-speed digital signal processing
- High speed operation
  - 100ns cycle time
- Parallel pipelined multiply function
  - 16 bits x 16 bits → 26 bits
- Divide function
  - 26 bits ÷ 16 bits → 16 bits
- Program ROM
  - 1024 words x 24 bits
  - Internal (mask-programmed) and external ROM selectable
- Part of the program ROM can be used for constant data storage
- Two built-in 128 x 16 bits RAMs
- Expansion RAM function
  - Expandable up to 1024 words x 16 bits
  - Two access speed rates can be selected
- Numerous I/O functions
  - 16-bit parallel interface
  - Three input modes and two output modes including DMA
- Powerful instruction set using compound instructions
  - One level of subroutine nesting (multi-level nesting can be programmed)
  - Two levels of loop nesting (multi-level nesting can be programmed)
  - Compound instructions (for example, an arithmetic/logic instruction combined with a move instruction) enable concurrent processing
  - 15 arithmetic/logic instructions
- Addressing
  - Direct addressing
  - Indexed addressing
  - Immediate addressing
  - Virtual shift addressing
- Silicon-gate CMOS process
- Single 5 volt power supply, TTL I/O interface (except pins for clock signals)
- 88-pin space-saving pin grid array package
- Support tool, including cross-assembly software and evaluation board

Fig. 1 – BLOCK DIAGRAM



FUNCTION OF BLOCK

Block	Function
Clock generator	This block generates a cycle clock ($\overline{\phi3}$) used for internal operations. The clock pulses can be generated by supplying a clock signal from an external circuit through external pins CK1 and CK2, or by a crystal resonator and capacitors connected to CK1 and CK2. The master clock (MCLK) obtained by either of the above two methods has the same frequency as that of the CK1/CK2 clock and generates a cycle clock $\overline{\phi3}$ having the frequency of the machine cycle (which is half the MCLK frequency). All internal operations are timed by the cycle clock $\overline{\phi3}$.
Sequence control block	This block controls the DSP instruction execution sequence. The program counter (PC) is reset to address 0 by the $\overline{RST}$ pulse, and is incremented by 1 at each leading edge of $\overline{\phi3}$ after $\overline{RST}$ is turned off. The PC output is connected to the address input of the internal microinstruction ROM (IROM) via the ROM pointer (DPR), and the ROM data is read out sequentially according to the PC value. The DPR value is also output through PA9 to PA0 to the outside to permit access to an external ROM (EROM). Data from the EROM is input to the MB 8764 through P23 to P0. At any given time, either the IROM or EROM can be used, and the choice is controlled by the IRM input. The IROM is a mask ROM with a capacity of 1,024 words x 24 bits. The ROM that has the same organization can be used for the EROM. The IROM and EROM are functionally identical. The ROM output data is transferred to the instruction register IR0 at the beginning of a cycle (that is, at the leading edge of $\overline{\phi3}$), moved to the instruction register IR1 at the beginning of the following cycle, then decoded and executed. To perform a branch instruction,address can be loaded into PC through IR0 and the IBUS, and the PC value can be saved in RAM or in another register through the IBUS. PCS is single PC stack used for subroutine execution. Two loop counters, C0 and C1, are provided to facilitate the handling of loops. This block also has a cycle counter (CYC) that controls execution of multi-cycle instructions. This counter automatically stops incrementing PC during execution of a multi-cycle instruction.

FUNCTION OF BLOCK (Cont'd)

Block	Function
Decoder	Instruction codes fetched from the instruction ROM and transferred to instruction registers IR0 and IR1 at the beginning of each cycle are moved to the look-ahead decoder (LAD) and decoder (DEC), respectively, then interpreted and executed. Execution of an instruction (the execution cycle) usually takes place while the instruction is stored in IR1. The DEC output controls the enable lines of the registers required for execution. Before an instruction is executed, LAD controls calculation of the effective address in RAM, interprets operations to be performed in the arithmetic and logic block, and decodes the number of cycles required for the instruction. The number of cycles required for an instruction is the number of machine cycles during which the instruction is stored in IR1.
Address calculation block	This block calculates the effective (execution) address in RAM (IRAM/ERAM) or ROM (table ROM). The address calculation block consists of index registers X and Y, stacks XS and YS for index registers X and Y, a 7-bit adder (AD1), an 8-bit adder (AD2), the virtual shift pointer (VP), and the virtual shift mode register (VS). An effective address is calculated in the LAD cycle, and the result is used as the execution address in the following execution cycle. An address in the table ROM is first calculated in AD1, then used to read table data through the table address register (TBA) and ROM pointer (DPR). To access IRAM by an instruction having one address, the effective address is first calculated in AD2, then the result is used to access IRAM through the RAM pointer (DPB). To access IRAM by an instruction having two addresses, the effective address in ARAM is calculated in AD1, the effective address in BRAM is calculated in AD2, and the results are used to access ARAM and BRAM through DPA and DPB. An address in ERAM is calculated by AD2 and the result is used to access ERAM through the ERAM pointer (DPE). Note that the table ROM is accessed by adding the value of page register PGT as the MSB element of the address, and the ROM data (16-bit) is output to IBUS through TBD. ERAM is accessed by adding the value of page register PGM as the MSB element of the address.
RAM	This device has two 128-word x 16-bit RAM areas called ARAM and BRAM. ARAM and BRAM can be used as two independent RAMs, or as a single RAM (IRAM) having a continuous address space. If the internal RAM is not sufficient, an external RAM (ERAM) can be connected to the chip. The ERAM can be used as an extension of BRAM or IRAM, but its address space is independent of BRAM or IRAM.
Arithmetic and logic block	Arithmetic and logic instructions are executed in this block. Execution of an instruction is timed by the machine cycle. This block consists of input registers A and B, an accumulator D that receives the operation result, a multiplier MLT, and an arithmetic and logic unit ALU. Multiplication is performed by a two-stage parallel multiplier in which MLT and ALU functions are pipelined. MLT multiplies the values of A and B unconditionally at each instruction and stores the intermediate results in the temporary registers TR0 and TR1. The final result of multiplication is obtained by having the ALU add the values of TR0 and TR1 according to a subsequent multiply instruction. Since the multiplier has a two-stage pipeline structure, it takes two cycles to obtain the multiplication result in D after data have been loaded into A and B. Operations other than multiplication are performed by the ALU alone, and the result is stored directly in D. The arithmetic and logic block also includes operation flags (PL, MI, ZR, and OV) that can be used to indicate conditions for conditional branch instructions. Register D has a longer bit length than the internal bus (IBUS), so a control register CLP is provided to output clipped data when the D value overflows the IBUS.
I/O interface	The I/O interface is used to exchange data between the DSP chip and an external circuit. It consists of I/O registers, an I/O controller and flags. The I/O controller controls data transfer to/from the external circuit independently of the execution of instructions. Data can be input from an external circuit through EI with or without address information through EIA. There are three input modes: the P, D, and A modes. These modes are distinguished by values set by instructions in the mode registers ADM and DMM. When data is set in EI, the input flag IF is set. In the P mode, the EI value is transferred to another register or to RAM by the program. In the D or A mode, the EI value is transferred to IRAM by cycle stealing. In the D mode, DMC is selected as the IRAM address, while in the A mode, EIA is selected. IF is reset when the EI contents are transferred to another location. Data is output to an external circuit through EA and EO. There are two output modes, and they are distinguished by the instruction data placed in EA. OF is set when data is placed in EA, and is reset when data output to the external circuit is completed. The data exchange between the DSP and an external circuit as explained above is performed through I/O control pins for synchronization with the external circuit. The I/O interface also includes the F0 and F1 flags. These are set by external input signals and used for program control or synchronization.

PIN ASSIGNMENT

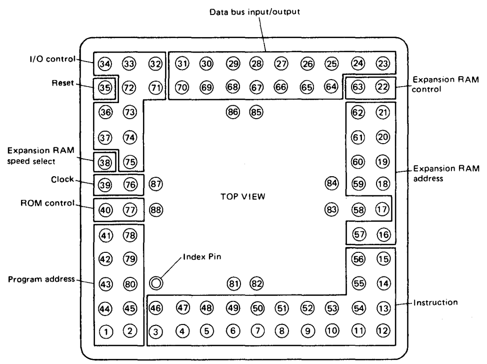


Fig. 2 – PIN ASSIGNMENT

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	PA1	16	EA0	31	D_{14}	46	P23	61	EA7	76	CK2
2	PA0	17	–	32	$\overline{\text{REQ}}$	47	P21	62	EA9	77	TST
3	P22	18	EA3	33	$\overline{\text{BCT}}$	48	P18	63	$\overline{\text{ECE}}$	78	PA9
4	P20	19	EA5	34	$\overline{\text{RCK}}$	49	P16	64	D_2	79	PA6
5	P19	20	EA6	35	$\overline{\text{RST}}$	50	P15	65	D_4	80	PA4
6	P17	21	EA8	36	$\overline{\text{FLO}}$	51	P13	66	D_7	81	GND
7	P14	22	$\overline{\text{EWE}}$	37	$\overline{\text{WCK}}$	52	P10	67	D_9	82	V_{CC}
8	P12	23	D_0	38	ESS	53	P8	68	D_{10}	83	V_{CC}
9	P11	24	D_1	39	CK1	54	P6	69	D_{12}	84	GND
10	P9	25	D_3	40	IRM	55	P3	70	D_{15}	85	GND
11	P7	26	D_5	41	PA8	56	P1	71	$\overline{\text{ACT}}$	86	V_{CC}
12	P5	27	D_6	42	PA7	57	EA1	72	$\overline{\text{AIF}}$	87	V_{CC}
13	P4	28	D_8	43	PA5	58	–	73	$\overline{\text{FL1}}$	88	GND
14	P2	29	D_{11}	44	PA3	59	EA2	74	$\overline{\text{AOF}}$		
15	P0	30	D_{13}	45	PA2	60	EA4	75	$\overline{\text{ASL}}$		

No.	Name	I/O	Function
78	PA9	Output	Program address MSB
41	PA8	Output	Program address BIT8
42	PA7	Output	Program address BIT7
79	PA6	Output	Program address BIT6
43	PA5	Output	Program address BIT5
80	PA4	Output	Program address BIT4
44	PA3	Output	Program address BIT3
45	PA2	Output	Program address BIT2
1	PA1	Output	Program address BIT1
2	PA0	Output	Program address LSB
46	P23	I/O	Instruction MSB
3	P22	I/O	Instruction BIT22
47	P21	I/O	Instruction BIT21
4	P20	I/O	Instruction BIT20
5	P19	I/O	Instruction BIT19
48	P18	I/O	Instruction BIT18
6	P17	I/O	Instruction BIT17
49	P16	I/O	Instruction BIT16
50	P15	I/O	Instruction BIT15
7	P14	I/O	Instruction BIT14
51	P13	I/O	Instruction BIT13
8	P12	I/O	Instruction BIT12
9	P11	I/O	Instruction BIT11
52	P10	I/O	Instruction BIT10
10	P9	I/O	Instruction BIT9
53	P8	I/O	Instruction BIT8
11	P7	I/O	Instruction BIT7
54	P6	I/O	Instruction BIT6
12	P5	I/O	Instruction BIT5
13	P4	I/O	Instruction BIT4

No.	Name	I/O	Function
55	P3	I/O	Instruction BIT3
14	P2	I/O	Instruction BIT2
56	P1	I/O	Instruction BIT1
15	P0	I/O	Instruction LSB
39	CK1	Input	Master clock input pin 1
76	CK2	Input	Master clock input pin 2
35	$\overline{\text{RST}}$	Input	Initialization
40	IRM	Input	Internal/external ROM switching
77	TST	Input	Internal ROM test mode
62	EA9	Output	Expansion RAM address MSB
21	EA8	Output	Expansion RAM address BIT8
61	EA7	Output	Expansion RAM address BIT7
20	EA6	Output	Expansion RAM address BIT6
19	EA5	Output	Expansion RAM address BIT5
60	EA4	Output	Expansion RAM address BIT4
18	EA3	Output	Expansion RAM address BIT3
59	EA2	Output	Expansion RAM address BIT2
57	EA1	Output	Expansion RAM address BIT1
16	EA0	Output	Expansion RAM address LSB
70	D15	I/O	Data bus I/O MSB
31	D14	I/O	Data bus I/O BIT14

No.	Name	I/O	Function
30	D13	I/O	Data bus I/O BIT13
69	D12	I/O	Data bus I/O BIT12
29	D11	I/O	Data bus I/O BIT11
68	D10	I/O	Data bus I/O BIT10
67	D9	I/O	Data bus I/O BIT9
28	D8	I/O	Data bus I/O BIT8
66	D7	I/O	Data bus I/O BIT7
27	D6	I/O	Data bus I/O BIT6
26	D5	I/O	Data bus I/O BIT5
65	D4	I/O	Data bus I/O BIT4
25	D3	I/O	Data bus I/O BIT3
64	D2	I/O	Data bus I/O BIT2
24	D1	I/O	Data bus I/O BIT1
23	D0	I/O	Data bus I/O LSB
34	$\overline{\text{RCK}}$	Input	Data read clock
33	$\overline{\text{BCT}}$	Input	Data bus output enable
72	$\overline{\text{AIF}}$	Input	Data input request
36	$\overline{\text{FL0}}$	Input	Flag input
73	$\overline{\text{FL1}}$	Input	Flag input
75	$\overline{\text{ASL}}$	Input	Data output type specification in E mode
37	$\overline{\text{WCK}}$	Output	Data write clock
74	$\overline{\text{AOF}}$	Output	Output data type specification in I mode
71	$\overline{\text{ACT}}$	Output	Input enable
32	$\overline{\text{REQ}}$	Output	Data bus request
22	$\overline{\text{EWE}}$	Output	ERAM write clock
63	$\overline{\text{ECE}}$	Output	ERAM chip enable
38	ESS	Input	ERAM speed select

ABSOLUTE MAXIMUM RATINGS*1

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{CC}	-0.3^{*2}	7.0	V
Input voltage	V_I	-0.3^{*2}	$V_{CC} + 0.3^{*2}$	V
Output voltage	V_O	-0.3^{*2}	$V_{CC} + 0.3^{*2}$	V
Operating temperature	T_{OP}	0	85	°C
Storage temperature	T_{STG}	–55	150	°C

Note: *1 Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*2 This value applies in a steady condition. It may be 0.5 V in a transient condition (for 20 to 30 ns).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature	T_{OP}	0		85	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise specified.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input high voltage	V_{IH}	Other than CK1, CK2	2.0		V_{CC} +0.3	V
	V_{IHCK}	CK1, CK2	4.0		V_{CC} +0.3	V
Input low voltage	V_{IL}	Other than CK1, CK2	–0.3		0.8	V
	V_{ILCK}	CK1, CK2	–0.3		0.6	V
Output high voltage	V_{OH}	I_{OH} = –0.4 mA	2.7		V_{CC}	V
Output low voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 to 5.5 V	–25		25	μA
Input leakage current (Three-state pin input)	I_{LZ}	V_I = 0 to 5.5 V	–40		40	μA
Static power supply current	I_{CCS}			1		mA
Power supply current	I_{CC}	f_{OP} = 8 MHz		60		mA

CAPACITANCE

(V_{CC} = V_I = 0 V, f_M = 8 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input pin	C_{IN}			5	pF
Output pin	C_{OUT}			5	pF
I/O pin	$C_{I/O}$			8	pF

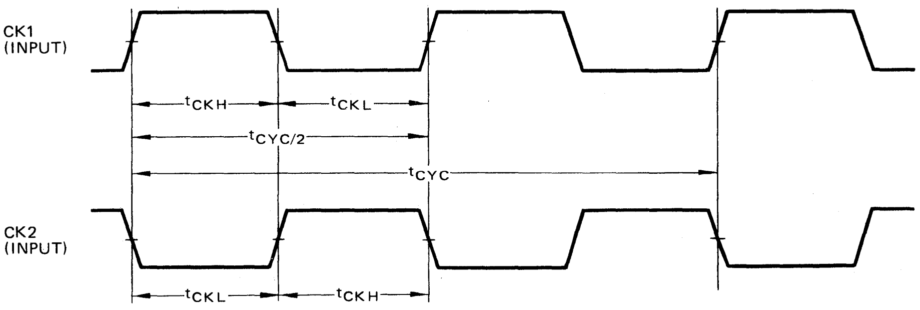
AC CHARACTERISTICS

EXTERNAL CLOCK TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time *1	t_{CYC}	100			ns
High voltage pulse width	t_{CKH}	20			ns
Low voltage pulse width	t_{CKL}	20			ns

Note: *1 Value when ERAM (extended RAM) is not used. When ERAM is used, follow the specifications for the ERAM interface AC characteristics. This note also applies to the following AC characteristics.

Fig. 3 – EXTERNAL CLOCK TIMING DIAGRAM



INTERNAL OSCILLATOR (Crystal oscillator connected)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time	t_{CYC}	100			ns
Crystal frequency	f_{CYC}		16	20	MHz

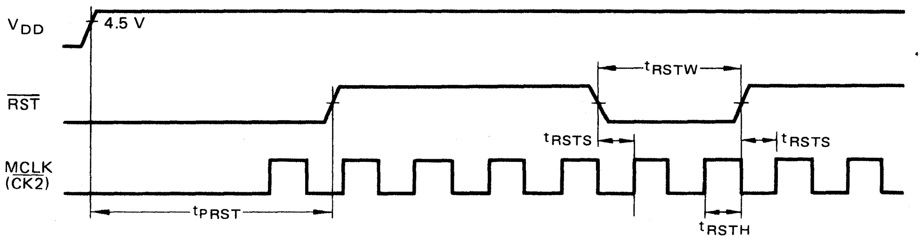
RESET INPUT TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Power-on reset *1	t_{PRST}		1		ms
MCLK setup *2	t_{RSTS}	20			ns
MCLK hold *2	t_{RSTH}	15			ns
Reset input pulse width	t_{RSTW}	t_{CYC} +35			ns

Note: *1 The time specification for power-on reset applies to the internal oscillation mode.
In the external clock mode, the reset pulse must be entered so that the leading edge of MCLK ($\overline{CK2}$) can be produced while $\overline{RST}$ = 0.

*2 In the external clock mode, MCLK is considered to be $\overline{CK2}$ (the inversion of the clock input from CK2).
This note also applies to the following AC characteristics.

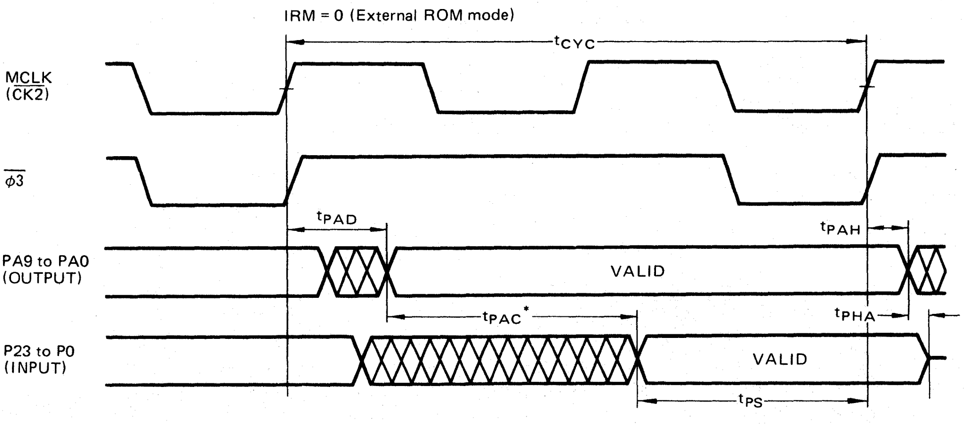
Fig. 4 – RESET INPUT TIMING DIAGRAM



EXTERNAL ROM INTERFACE TIMING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Address output delay (from MCLK pulse)	t_{PAD}	C_L = 50pF		60	75	ns
Address output hold (from MCLK pulse)	t_{PAH}	C_L = 50pF	20			ns
Data hold time (to address)	t_{PHA}	C_L = 50pF	0			ns
Data setup (before MCLK pulse)	t_{PS}	C_L = 50pF	10	10		ns

Fig. 5 – EXTERNAL ROM INTERFACE TIMING DIAGRAM



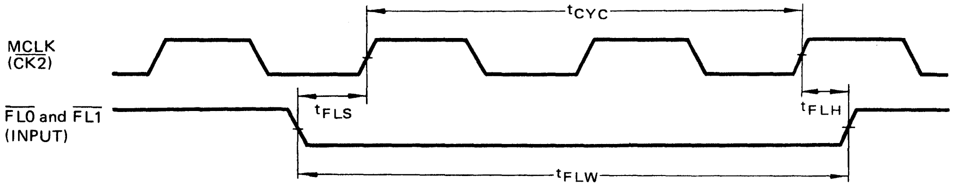
Note: *t_{PAC} is the address access time provided by the specification of the external ROM.

FLAG ($\overline{FL0}$ and $\overline{FL1}$) INPUT TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Setup time	t_{FLS}	15			ns
Hold time	t_{FLH}	30			ns
Pulse width*1	t_{FLW}	t_{CYC} + 45			ns

Note: *1 t_{FLW} (Min) = 2 x t_{CYC} + 45 when ERAM is used with ESS = 1.

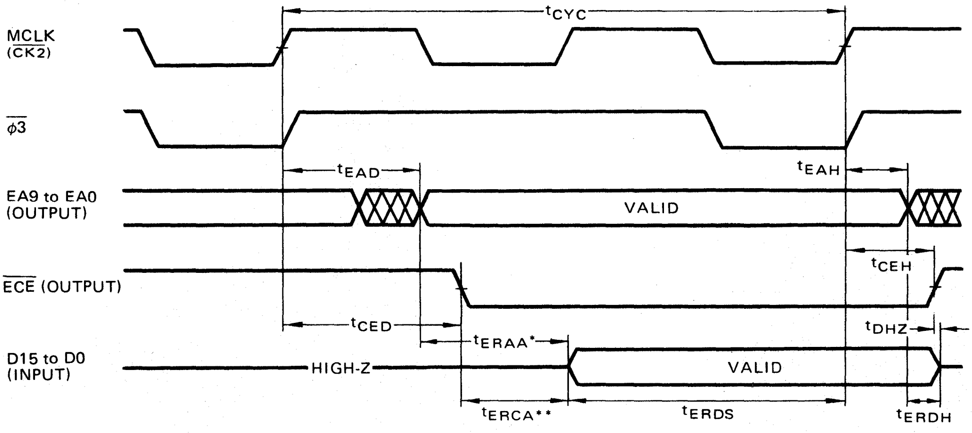
Fig. 6 – FLAG INPUT TIMING DIAGRAM



EXPANSION RAM INTERFACE TIMING (ESS = 0, Read Cycle)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Address output delay	t_{EAD}	C_L = 50pF		50	60	ns
Address output hold	t_{EAH}	C_L = 50pF	10	13		ns
Chip enable output delay	t_{CED}	C_L = 50pF		57	70	ns
Chip enable output hold	t_{CEH}	C_L = 50pF	17	19		ns
Output disable	t_{DHZ}	C_L = 50pF	0			ns
Data input setup time	t_{ERDS}	C_L = 50pF	30	25		ns
Data input hold time	t_{ERDH}	C_L = 50pF	0			ns

Fig. 7 – EXPANSION RAM INTERFACE TIMING DIAGRAM (ESS = 0, Read Cycle)

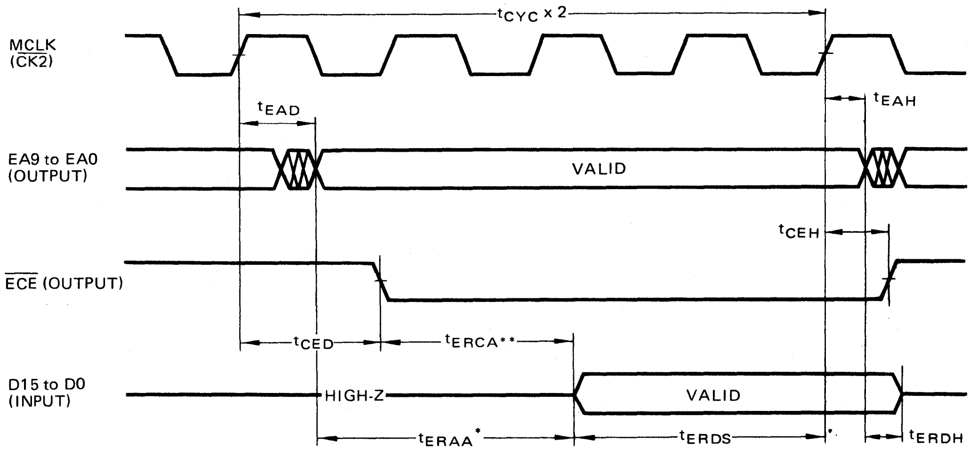


Note: *t_{ERAA} is the address access time provided by the specification of the expansion RAM.
**t_{ERCA} is the chip select access time provided by the specification of the expansion RAM.

EXPANSION RAM INTERFACE TIMING (ESS = 1, Read Cycle)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Address output delay	t_{EAD}	C_L = 50pF		50	60	ns
Address output hold	t_{EAH}	C_L = 50pF	10	13		ns
Chip enable output delay	t_{CED}	C_L = 50pF		57	70	ns
Chip enable output hold	t_{CEH}	C_L = 50pF	17	19		ns
Data input setup time	t_{ERDS}	C_L = 50pF	30	25		ns
Data input hold time	t_{ERDH}	C_L = 50pF	0			ns

Fig. 8 – EXPANSION RAM INTERFACE TIMING DIAGRAM (ESS = 1, Read Cycle)

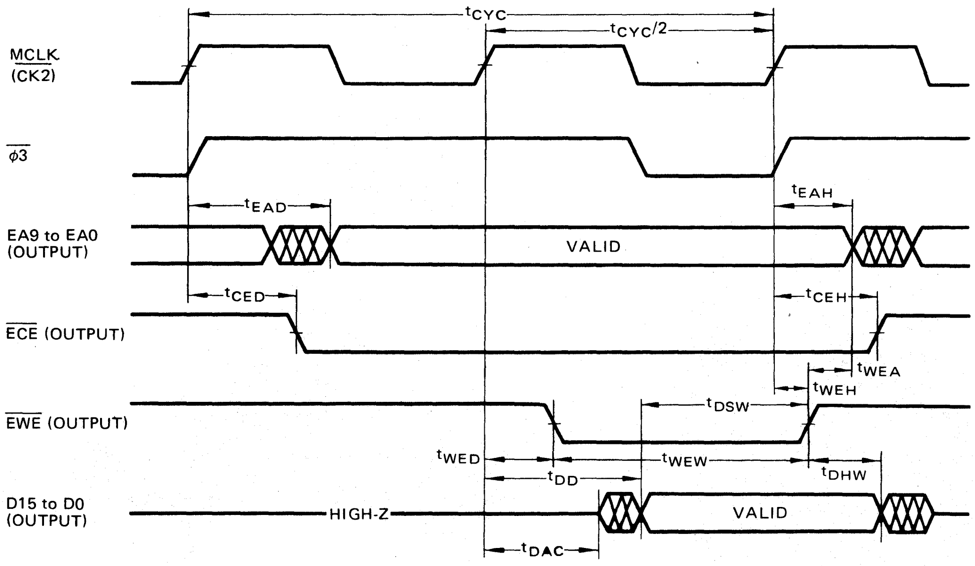


Note: *t_{ERAA} is the address access time provided by the specification of the expansion RAM.
**t_{ERCA} is the chip select access time provided by the specification of the expansion RAM.

EXPANSION RAM INTERFACE TIMING (ESS = 0, Write Cycle)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Address output delay	t_{EAD}	C_L = 50pF		50	60	ns
Address output hold	t_{EAH}	C_L = 50pF	10	13		ns
Address hold (after $\overline{EWE}$)	t_{WEA}	C_L = 50pF	5			ns
Chip enable output delay	t_{CED}	C_L = 50pF		57	70	ns
Chip enable output hold	t_{CEH}	C_L = 50pF	17	19		ns
Write enable output delay	t_{WED}	C_L = 50pF		40	50	ns
Write enable output hold	t_{WEH}	C_L = 50pF	5		35	ns
Write enable pulse width	t_{WEW}	C_L = 50pF	$\frac{t_{CYC}}{2} - 30$			ns
Data output delay	t_{DD}	C_L = 50pF + 1TTL		52	70	ns
Data setup (before $\overline{EWE}$)	t_{DSW}	C_L = 50pF + 1TTL	$\frac{t_{CYC}}{2} - 50$			ns
Data hold (after $\overline{EWE}$)	t_{DHW}	C_L = 50pF + 1TTL	5			ns
Data output active delay	t_{DAC}	C_L = 50pF + 1TTL		52	70	ns

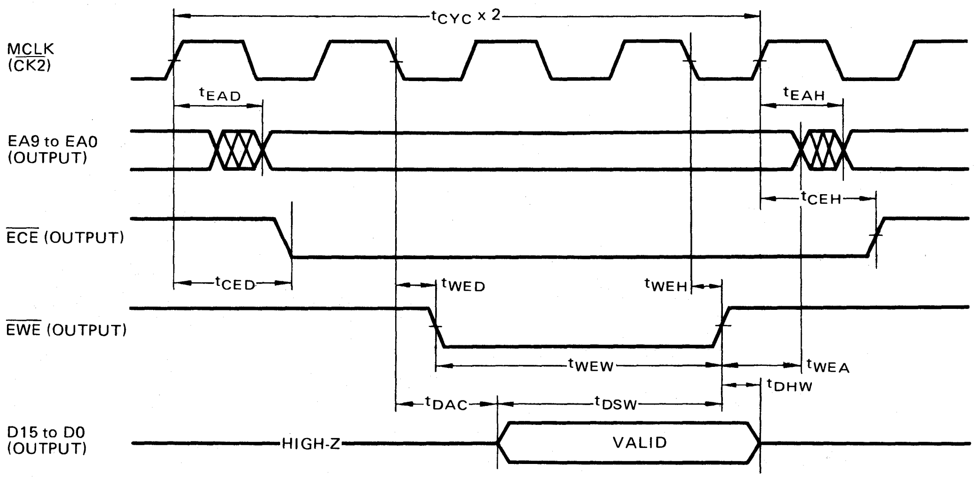
Fig. 9 – EXPANSION RAM INTERFACE TIMING DIAGRAM (ESS = 0, Write Cycle)



EXPANSION RAM INTERFACE TIMING (ESS = 1, Write Cycle)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Address output delay	t_{EAD}	C_L = 50pF		50	60	ns
Address output hold	t_{EAH}	C_L = 50pF	10	13		ns
Address output hold (after $\overline{EWE}$)	t_{WEA}	C_L = 50pF		25		ns
Chip enable output delay	t_{CED}	C_L = 50pF		57	70	ns
Chip enable output hold	t_{CEH}	C_L = 50pF	17	19		ns
Write enable output delay	t_{WED}	C_L = 50pF			50	ns
Write enable output hold	t_{WEH}	C_L = 50pF	10		35	ns
Write enable pulse width	t_{WEW}	C_L = 50pF	t_{CYC} – 40			ns
Data output active delay	t_{DAC}	C_L = 50pF + 1TTL		57	75	ns
Data setup (during $\overline{EWE}$)	t_{DSW}	C_L = 50pF + 1TTL	t_{CYC} – 65			ns
Data hold (after $\overline{EWE}$)	t_{DHW}	C_L = 50pF + 1TTL	5			ns

Fig. 10 – EXPANSION RAM INTERFACE TIMING DIAGRAM (ESS = 1, Write Cycle)

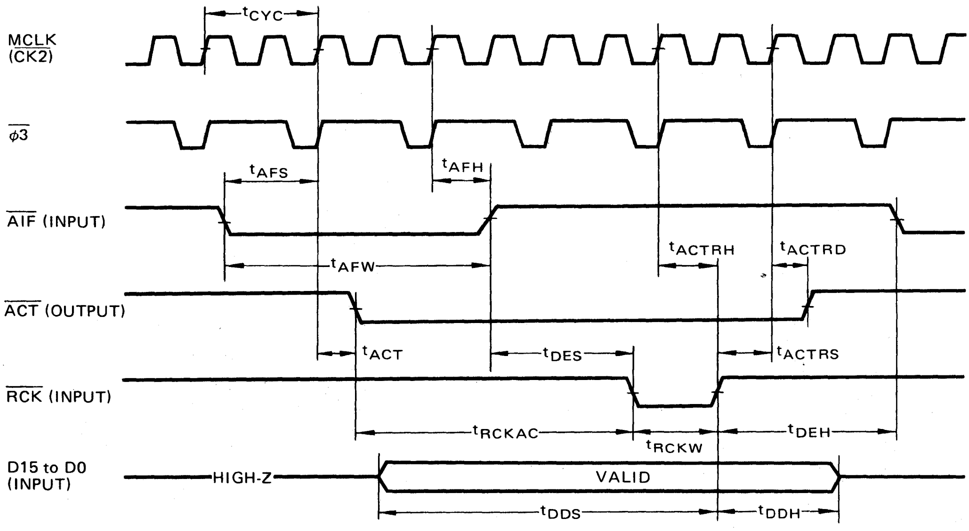


P MODE AND D MODE INPUT TIMING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{AIF}}$ setup	t_{AFS}		30			ns
$\overline{\text{AIF}}$ hold	t_{AFH}		20			ns
$\overline{\text{AIF}}$ pulse width *1	t_{AFW}		t_{CYC} +50			ns
$\overline{\text{ACT}}$ fall delay	t_{ACT}	C_L = 50pF + 1TTL			70	ns
$\overline{\text{ACT}}$ reset delay	t_{ACTRD}	C_L = 50pF + 1TTL			70	ns
$\overline{\text{RCK}}$ input enable	t_{RCKAC}		0			ns
$\overline{\text{RCK}}$ pulse width	t_{RCKW}		40			ns
$\overline{\text{RCK}}$ enable setup	t_{DES}		35			ns
$\overline{\text{RCK}}$ enable hold	t_{DEH}		25			ns
Data setup	t_{DDS}		25			ns
Data hold	t_{DDH}		25			ns
$\overline{\text{ACT}}$ reset setup	t_{ACTRS}		60			ns
$\overline{\text{ACT}}$ reset hold	t_{ACTRH}		10			ns

Note: *1 t_{AFW} (Min) =2 x t_{CYC} + 50 when ERAM is used with ESS = 1.

Fig. 11 – P MODE AND D MODE INPUT TIMING DIAGRAM

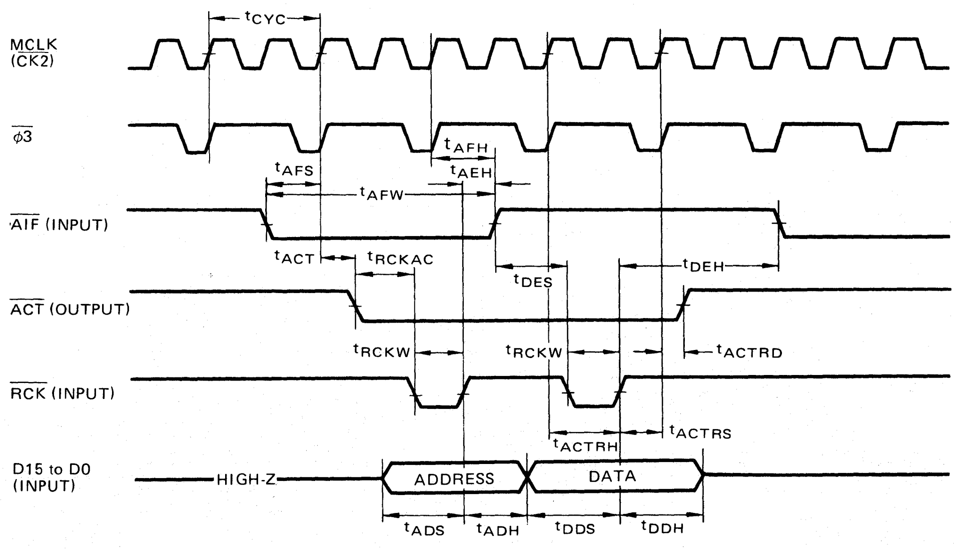


A MODE INPUT TIMING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{AIF}}$ setup	t_{AFS}		30			ns
$\overline{\text{AIF}}$ hold	t_{AFH}		20			ns
$\overline{\text{AIF}}$ pulse width *1	t_{AFW}		t_{CYC} + 50			ns
$\overline{\text{ACT}}$ fall delay	t_{ACT}	C_L = 50pF + 1TTL			70	ns
$\overline{\text{ACT}}$ reset delay	t_{ACTRD}	C_L = 50pF + 1TTL			70	ns
$\overline{\text{RCK}}$ input enable	t_{RCKAC}		0			ns
$\overline{\text{RCK}}$ pulse width	t_{RCKW}		40			ns
$\overline{\text{RCK}}$ enable hold	t_{AEH}		25			ns
$\overline{\text{RCK}}$ enable setup	t_{DES}		35			ns
$\overline{\text{RCK}}$ enable hold	t_{DEH}		25			ns
Address setup	t_{ADS}		25			ns
Address hold	t_{ADH}		25			ns
Data setup	t_{DDS}		25			ns
Data hold	t_{DDH}		25			ns
$\overline{\text{ACT}}$ reset setup	t_{ACTRS}		60			ns
$\overline{\text{ACT}}$ reset hold	t_{ACTRH}		10			ns

Note: *1 t_{AFW} (Min) = 2 x t_{CYC} + 50 when ERAM is used with ESS = 1.

Fig. 12 — A MODE INPUT TIMING DIAGRAM

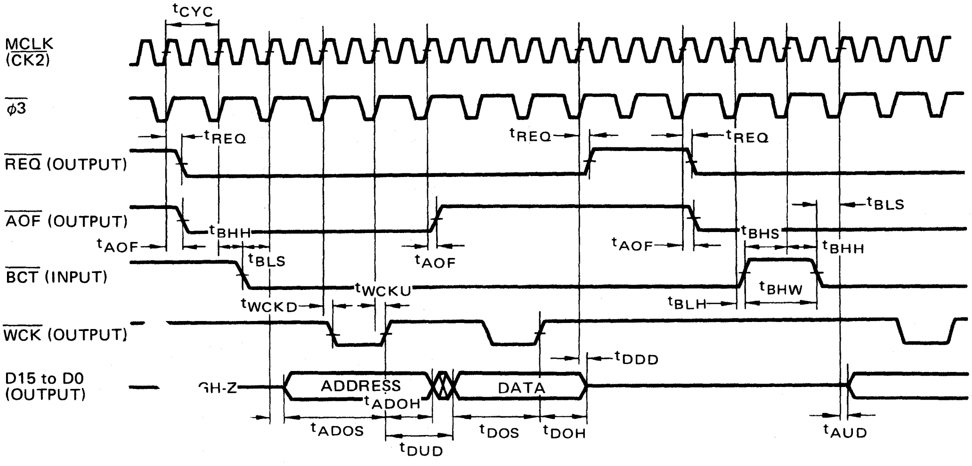


I MODE OUTPUT TIMING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{REQ}}$ output delay	t_{REQ}	C_L = 50pF + 1TTL			75	ns
$\overline{\text{AOF}}$ output delay	t_{AOF}	C_L = 50pF + 1TTL			65	ns
$\overline{\text{BCT}}$ level 0 setup	t_{BLS}		40			ns
$\overline{\text{BCT}}$ level 0 hold	t_{BLH}		15			ns
$\overline{\text{BCT}}$ level 1 setup	t_{BHS}		40			ns
$\overline{\text{BCT}}$ level 1 hold	t_{BHH}		15			ns
$\overline{\text{BCT}}$ level 1 pulse width *1	t_{BHW}		t_{CYC} + 55			ns
$\overline{\text{WCK}}$ fall delay	t_{WCKD}	C_L = 50pF + 1TTL			65	ns
$\overline{\text{WCK}}$ rise delay	t_{WCKU}	C_L = 50pF + 1TTL			65	ns
Address output delay	t_{AUD}	C_L = 50pF + 1TTL			85	ns
Data output delay	t_{DUD}	C_L = 50pF + 1TTL			80	ns
Data output disable	t_{DDD}	C_L = 50pF + 1TTL			70	ns
Address setup	t_{ADOS}	C_L = 50pF + 1TTL	170			ns
Address hold	t_{ADOH}	C_L = 50pF + 1TTL	65			ns
Data setup	t_{DOS}	C_L = 50pF + 1TTL	170			ns
Data hold	t_{DOH}	C_L = 50pF + 1TTL	65			ns

Note: *1 t_{BHW} (Min) = 2 x t_{CYC} + 55 when ERAM is used with ESS = 1.

Fig. 13 — I MODE OUTPUT TIMING DIAGRAM

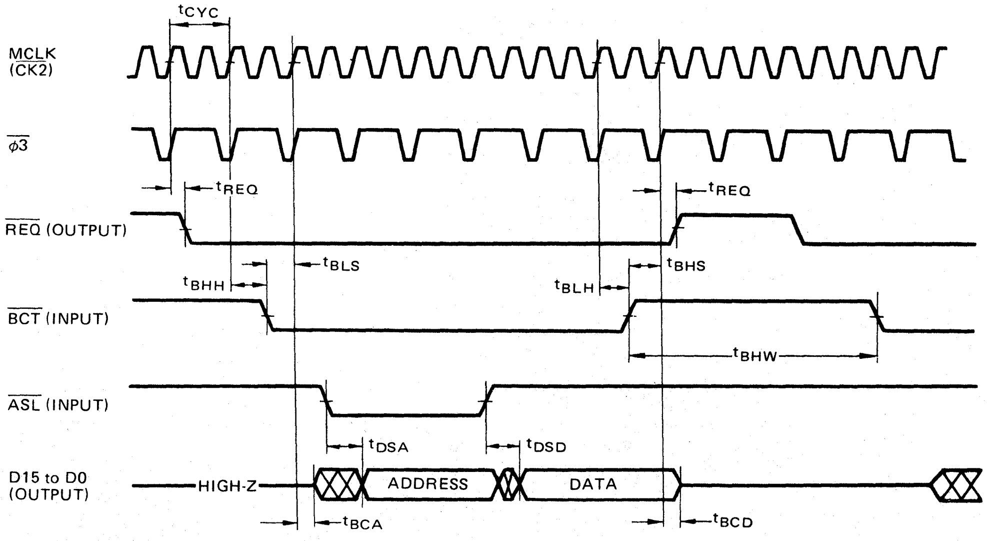


E MODE OUTPUT TIMING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{REQ}$ output delay	t_{REQ}	C_L = 50pF + 1TTL			75	ns
$\overline{BCT}$ level 0 setup	t_{BLS}		40			ns
$\overline{BCT}$ level 0 hold	t_{BLH}		15			ns
$\overline{BCT}$ level 1 setup	t_{BHS}		40			ns
$\overline{BCT}$ level 1 hold	t_{BHH}		15			ns
$\overline{BCT}$ level 1 pulse width *1	t_{BHW}		t_{CYC} +55			ns
Output active delay	t_{BCA}	C_L = 50pF + 1TTL			85	ns
Address output from fall of $\overline{ASL}$	t_{DSA}	C_L = 50pF + 1TTL			85	ns
Data output from rise of $\overline{ASL}$	t_{DSD}	C_L = 50pF + 1TTL			85	ns
Output inactive	t_{BCD}	C_L = 50pF + 1TTL			70	ns

Note: *1 t_{BHW} (Min) = 2 x t_{CYC} + 55 when ERAM is used with ESS = 1.

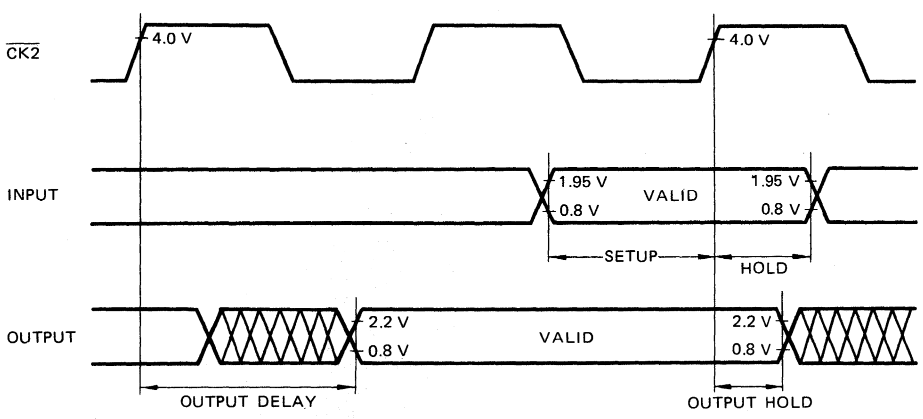
Fig. 14 – E MODE OUTPUT TIMING DIAGRAM



AC CHARACTERISTICS MEASUREMENT CONDITIONS

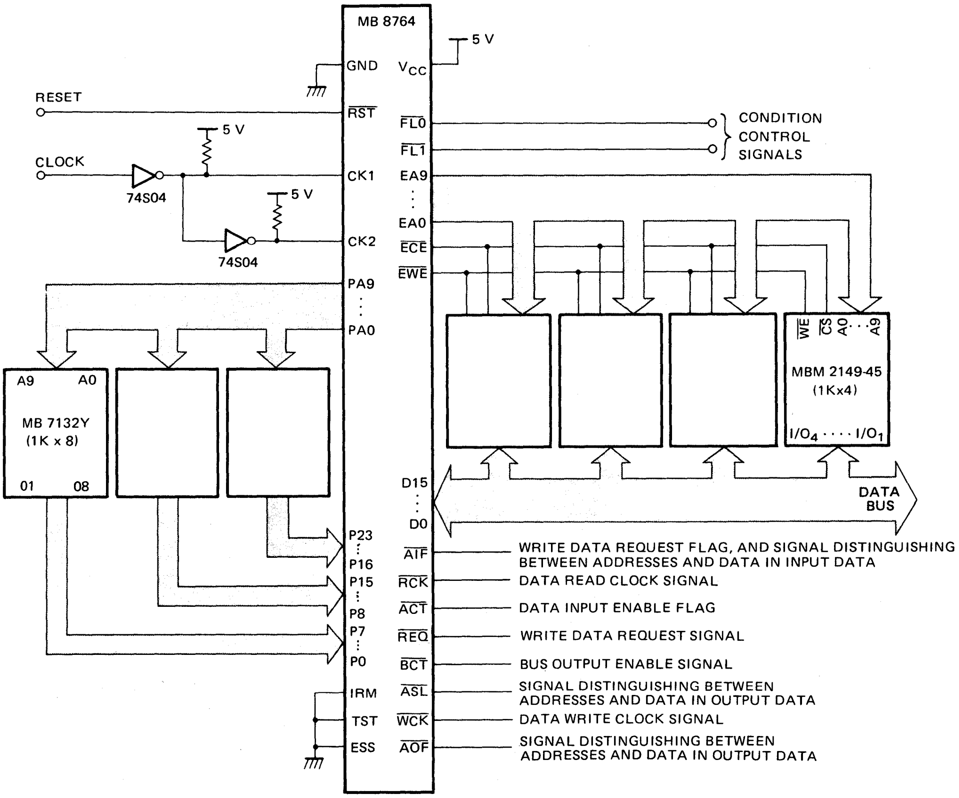
Parameter	Symbol	Condition
Power supply voltage	V_{DD}	5 V ± 10%
Ambient temperature	T_A	0 to 85°C

Fig. 15 – AC CHARACTERISTICS MEASUREMENT WAVEFORMS



APPLICATION INFORMATION

Fig. 16 – EXAMPLE OF MB 8764 APPLICATION CIRCUIT
(with 1K-word External ROM and 1K-word External RAM)



INSTRUCTION SET

ARITHMETIC AND LOGIC INSTRUCTIONS

Mnemonic	Processing performed	Mnemonic	Processing performed
NOP	No operation	ABS	|D| → D
ADD	A + B → D	NEG	–D → D
MLT	A x B → D	SRA	Shift D right arithmetic → D
SUB	B – A → D	SLA	Shift D left arithmetic → D
MSM	D + A x B → D	AND	D ∩ A → D
MRD	D – A x B → D	ORA	D ∪ A → D
SUM	D + A → D	DIV	D ÷ A → D
RED	D – A → D	COM	$\overline{D}$ → D

TRANSFER INSTRUCTIONS

Mnemonic			Processing performed
LTB:	(Arithmetic/logic instruction)	\$a, \$b	ROMT → A, BRAM/ERAM → B
LAB:	(Arithmetic/logic instruction)	\$a, \$b	ARAM → A, BRAM/ERAM → B
MAB:	(Arithmetic/logic instruction)	\$a, \$b	ARAM → BRAM/ERAM
MBA:	(Arithmetic/logic instruction)	\$a, \$b	BRAM/ERAM → ARAM
MOV:	(Arithmetic/logic instruction)	\$a, Reg [:Reg . .]	IRAM/ERAM → Register
MOV:	(Arithmetic/logic instruction)	#\$d, Reg [:Reg . .]	Immediate data (d) → Register
MOV:	(Arithmetic/logic instruction)	Reg, Reg [:Reg . .]	Register → Register
LDI:	(Arithmetic/logic instruction)	#\$d	d → A
LIB:	(Arithmetic/logic instruction)	#\$d	d → A, BRAM → B

JUMP INSTRUCTIONS

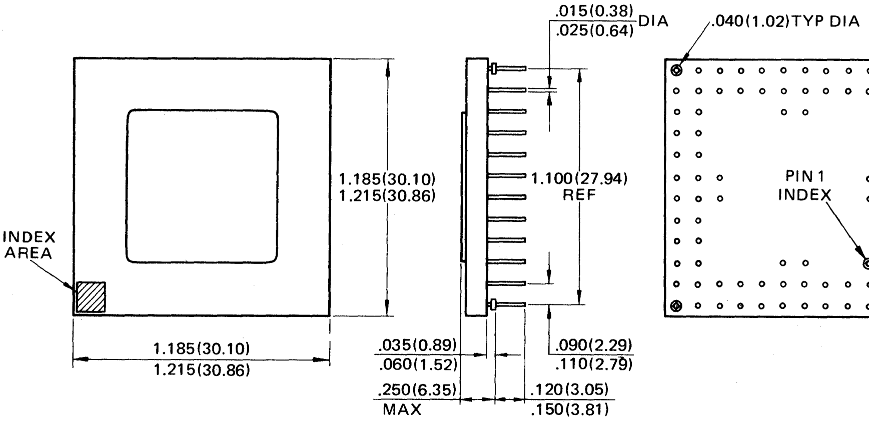
Mnemonic			Processing performed
JMP:	(Arithmetic/logic instruction)	#\$d	Unconditional jump (d → PC)
JOC:	(Arithmetic/logic instruction)	#\$d, flag	Conditional jump (d→PC)
JOC:	(Arithmetic/logic instruction)	\$a, flag	Conditional jump (IRAM/ERAM → PC)
JSR:	(Arithmetic/logic instruction)	#\$d	Jump to subroutine (PC → PCS, d → PC)
RTS:	(Arithmetic/logic instruction)		Return from subroutine

MISCELLANEOUS INSTRUCTIONS

Mnemonic			Processing performed
CLR:	[Reg [:Reg . . .] . . .]		Clear register
SET:	[Reg [:Reg . . .] . . .]		Set register
MXY:	(Arithmetic/logic instruction)	$\#\$d_1, \#Sd_2$	X + d_1 → X, Y + d_2 → Y
LIY:	(Arithmetic/logic instruction)	#\$d	d → A,BRAM → B, Y + 1 → Y
AVP:	(Arithmetic/logic instruction)	#\$d	VP + d → VP
LVP:	(Arithmetic/logic instruction)	#\$d	d → VP
ADY:	(Arithmetic/logic instruction)		Y+YS → Y
GXY:	(Arithmetic/logic instruction)		XS → X, YS → Y
SXY:	(Arithmetic/logic instruction)	#\$d	d → C1, X → XS, Y → YS, O → X, O → Y
NOP:	(Arithmetic/logic instruction)		No operation

PACKAGE DIMENSIONS

88-LEAD CERAMIC (METAL SEAL) REPEATED QUAD IN-LINE PACKAGE
(CASE No.: RIT-88C-A01)



Dimensions in
inches (millimeters)

Digital Signal Processor

MB87064

April 1986
Edition 1.0

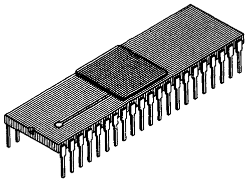
PRELIMINARY

DESCRIPTION

The Fujitsu MB87064 is a general-purpose LSI silicon gate Digital Signal Processor (DSP). The device is fabricated in low-power CMOS and features a high-speed pipelined multiplier, supports concurrent operations with compound instructions and multiple data paths, and offers flexible and expandable memory options. The MB87064 is housed in a 42-pin DIP.

Except for some changes in the instruction set and minor modifications in the hardware, the low-cost MB87064 DSP is a functional clone for Fujitsu's full-featured MB8764 DSP. The low-cost MB87064 is particularly useful in systems where the additional features of the MB8764 are simply not required. Since basic functions of the two parts are identical, this data sheet describes only those differences that affect system design. For complete functional detail pertaining to hardware and software, it is recommended that the user obtain data sheets for both parts (MB87064 and MB8764). If further information regarding Digital Signal Processing is desired, the user should request "Support Documentation for the MB8764" from the nearest Fujitsu sales office.

Both the MB87064 and the MB8764 are well suited for applications such as telecommunications, imaging work, and other signal-processing functions that require extensive computations and complex analysis.



DIP-42C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

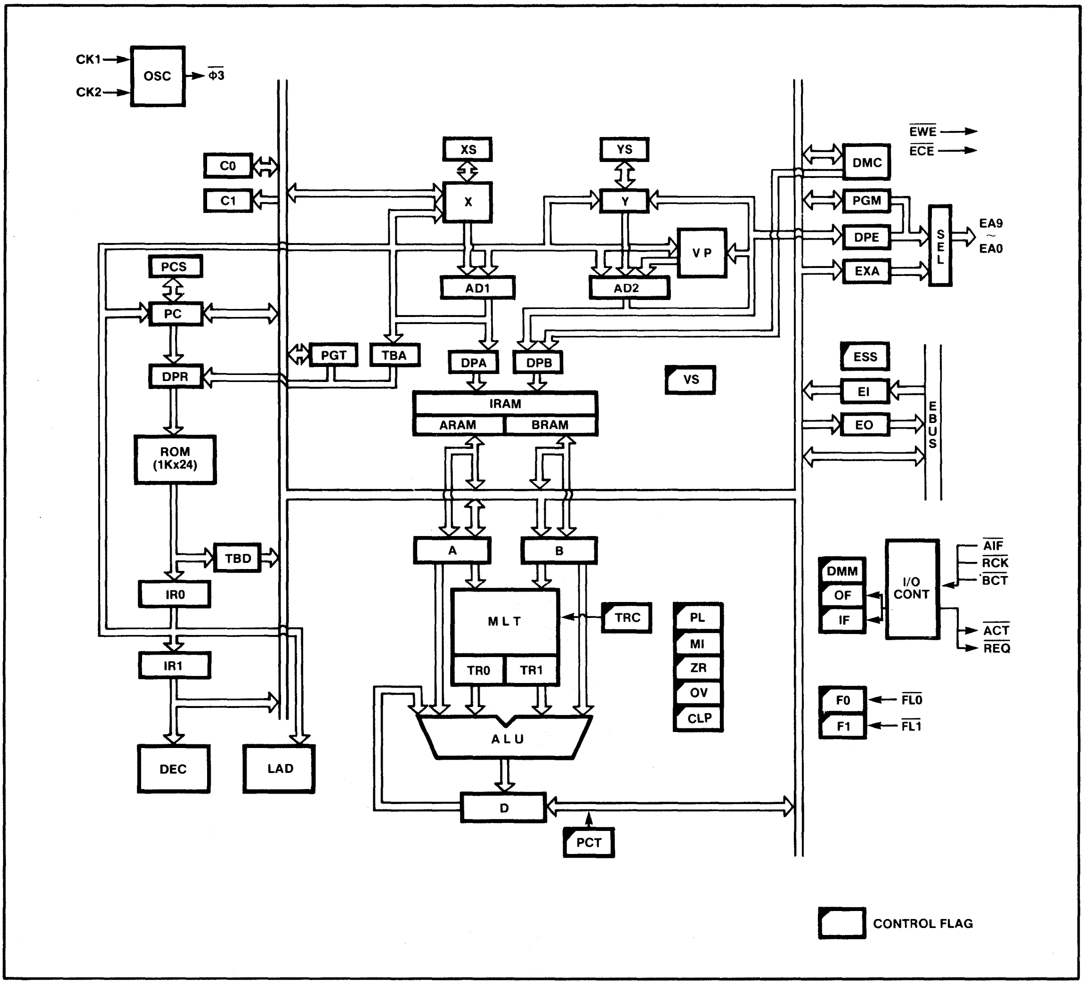
Table 1. Comparison of Features (MB87064 and MB8764)

Item	MB8764	MB87064
Hardware Architecture	Common Hardware Architecture • Parallel pipelined multiply function 16 bits x 16 bits → 26 bits • Divide function 26 bits ÷ 16 bits → 16 bits	
Instruction Set	MB8764 Instruction Set	Basically the same as the MB8764 but with few modifications
Operation Cycle Time	100ns	
Package	PGA88 Ceramic[1] LCC84 Ceramic	DIP42 Ceramic[1]
Program ROM	Internal (mask-programmable) ROM of 1024 words × 24 bits	
	External ROM of 1024 words × 24 bits selectable	No External ROM function
Data RAM	Built-in 2 blocks of 128 words × 16 bits Expansion RAM up to 1024 words × 16 bits	
I/O Functions	16-bit Parallel Interface	
	Three Input Modes Two Output Modes	Two Input Modes One Output Mode (Brand-new)
Addressing	Same Addressing Functions • Direct Addressing • Immediate Addressing • Indexed Addressing • Virtual Shift Addressing	
Support Tools	Common Support Tools • Evaluation Board • Softwares (Assemblers, Linkers, Software Simulators, Monitor) • In-Circuit Emulation Board[2]	
Applications	• Flexible system with external program memory • Small Volume Production with Internal/External ROM • System evaluation before Production	• High Volume Production with Mask ROM

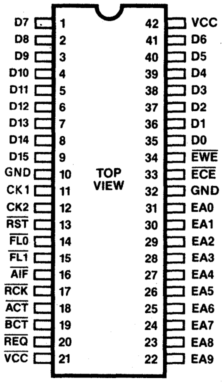
Notes:

1. Plastic package is scheduled for the future.
2. Soon to be available.

BLOCK DIAGRAM



PIN DESCRIPTIONS


D7 1
D8 2
D9 3
D10 4
D11 5
D12 6
D13 7
D14 8
D15 9
GND 10
CK1 11
$\overline{\text{CK2}}$ 12
$\overline{\text{RST}}$ 13
$\overline{\text{FL0}}$ 14
$\overline{\text{FL1}}$ 15
$\overline{\text{AIF}}$ 16
$\overline{\text{RCK}}$ 17
$\overline{\text{ACT}}$ 18
$\overline{\text{BCT}}$ 19
$\overline{\text{REQ}}$ 20
$\overline{\text{VCC}}$ 21
TOP VIEW
42 VCC
41 D6
40 D5
39 D4
38 D3
37 D2
36 D1
35 D0
34 $\overline{\text{EWE}}$
33 $\overline{\text{ECE}}$
32 GND
31 EA0
30 EA1
29 EA2
28 EA3
27 EA4
26 EA5
25 EA6
24 EA7
23 EA8
22 EA9

Pin No.	Designator	Function		Pin No.	Designator	Function	
		Input/Output Pins:				**Output Pins:**	
09	D15	Data bus	Bit 15 (MSB)	22	EA9	Expansion RAM Address	MSB
08	D14	Data bus	Bit 14	23	EA8	Expansion RAM Address	Bit 8
07	D13	Data bus	Bit 13	24	EA7	Expansion RAM Address	Bit 7
06	D12	Data bus	Bit 12	25	EA6	Expansion RAM Address	Bit 6
05	D11	Data bus	Bit 11	26	EA5	Expansion RAM Address	Bit 5
04	D10	Data bus	Bit 10	27	EA4	Expansion RAM Address	Bit 4
03	D9	Data bus	Bit 9	28	EA3	Expansion RAM Address	Bit 3
02	D8	Data bus	Bit 8	29	EA2	Expansion RAM Address	Bit 2
01	D7	Data bus	Bit 7	30	EA1	Expansion RAM Address	Bit 1
41	D6	Data bus	Bit 6	31	EA0	Expansion RAM address	LSB
40	D5	Data bus	Bit 5	34	$\overline{\text{EWE}}$	ERAM Write Clock Output	
39	D4	Data bus	Bit 4	33	$\overline{\text{ECE}}$	ERAM Chip Enable Output	
38	D3	Data bus	Bit 3	11	CK1	Master Clock Input Pin 1	
37	D2	Data bus	Bit 2	12	CK2	Master Clock Input Pin 2	
36	D1	Data bus	Bit 1	13	$\overline{\text{RST}}$	Initialization Input	
35	D0	Data bus	Bit 0 (LSB)	16	$\overline{\text{AIF}}$	Data Input Request	
10	GND	Circuit Ground		17	$\overline{\text{RCK}}$	Data Read Clock Input	
32	GND	Circuit Ground		18	$\overline{\text{ACT}}$	Data Input Enable Output	
42	V_{CC}	+5V Power Supply		20	$\overline{\text{REQ}}$	Data Bus Request Output	
21	V_{CC}	+5B Power Supply		19	$\overline{\text{BCT}}$	Data Bus Output Enable Input	
				14	$\overline{\text{FL0}}$	Flag Input	
				15	$\overline{\text{FL1}}$	Flag Input	

PIN MODIFICATIONS

Based on the pin configuration of the MB8764, the following modifications have been made for the MB87064.

Removal of pins caused by no external ROM:

PA9 ~ PA0 (10 pins)
IRM (1 pin)
P23 ~ P0 (24 pins)
TST (1 pin)

Removal of pins caused by reduction/modification of input/output mode:

$\overline{\text{ASL}}$ (1 pin)
$\overline{\text{AOF}}$ (1 pin)
$\overline{\text{WCK}}$ (1 pin)

Removal of pins caused by modification of external RAM speed control (hardware → software):

$\overline{\text{ESS}}$ (1 pin)

Removal of unneeded power/ground pins:

GND (2 pins)
V_{CC} (2 pins)

FUNCTIONAL DESCRIPTION

Program Memory

The program for the MB87064 is provided from the internal (mask-programmed) ROM with a capacity of 1024 words × 24 bits. The MB87064 cannot access external ROM.

Input/Output Modes

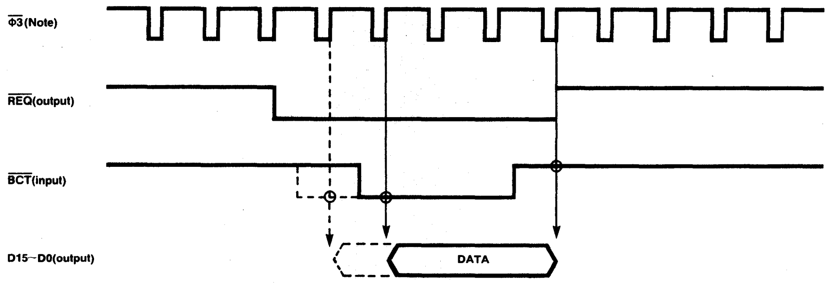
Input Modes

Two operating modes (D and P) are used to input data from an external device to the MB87064. The function and timing specification for the two input modes are the same as those in the MB8764. The selected input mode is loaded into the mode (DMM) register by the program.

Output Mode

Only one output mode is provided to transfer data from the MB87064 to an external peripheral. The output mode in the MB87064 is a modified version of the E mode in the MB8764. Output mode timing is shown in the following diagram.

Output Mode Timing


$\overline{\Phi 3}$(Note)
$\overline{\text{REQ}}$(output)
$\overline{\text{BCT}}$(input)
D15~D0(output)
DATA

Note:
Φ3 is the cycle clock that controls internal operations of the DSP.

Registers/Flags

Register Omission

Input address register EIA, output address register EA, unit register U, and address mode register ADM are not required in the MB87064.

New Registers and Flags

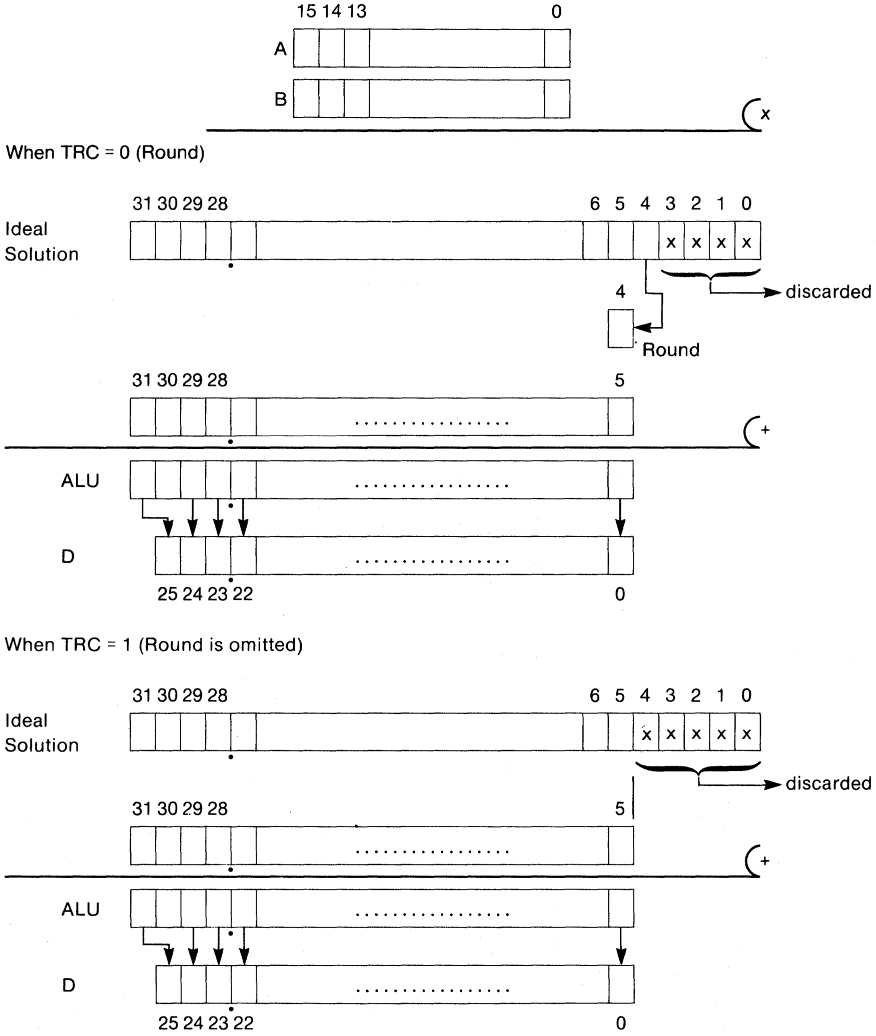
ESS Flag. Because the ESS pin has been removed, the MB87064 controls ERAM access speed by the ESS flag which, in turn, is controlled by the SET/CLR instructions. The low-speed mode (ESS = 1) is specified by the "SET ESS" instruction. It is cleared by the "CLR ESS" instruction and the high-speed mode (ESS = 0) is then specified. When the device is reset, the high-speed mode is selected by default.

Because the ESS pin has been removed, the MB87064 controls ERAM access speed through the ESS flag. A two cycle access is selected by setting the ESS flag (ESS = 1). and the single cycle access is selected by clearing the ESS flag (ESS = 0).

ESS is cleared upon reset (ESS = 0).

TRC Register. The TRC register is a 1-bit register used to control the truncation of the multiplication result. The TRC Register is controlled by the SET/CLR instructions.

When TRC is set to "1", the multiplication result is truncated to 26-bits without rounding. When TRC is set to "0", the result is rounded to 26-bits. (Same as the MB8764.)



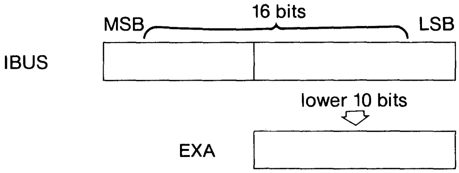
PCT Register. In the MB8764, even when operating in the CLIP mode with the overflow flag set, if two maximum negative numbers are multiplied together [(8000H) × (8000H)], the resulting output from the D register to IBUS is (0000H). Also, if positive or negative overflows occur, the resulting output may not be the maximum positive or negative values [(8000H) or (7FFFH)]. The MB87064 selects the PCT (protect mode) to avoid this overflow problem. The protect mode is controlled by the "PCT" flag. The "PCT" flag is set by the "SET PCT" instruction and cleared by the "CLR PCT" instruction.

The "PCT" flag is also cleared by a reset input. As with the MB8764, the normal mode is selected when the "PCT" flag is cleared.

EXA Register. The MB8764 outputs the contents of page register PGM and data pointer register DPE to the EA9 ~ EA0 pins regardless of ERAM access.

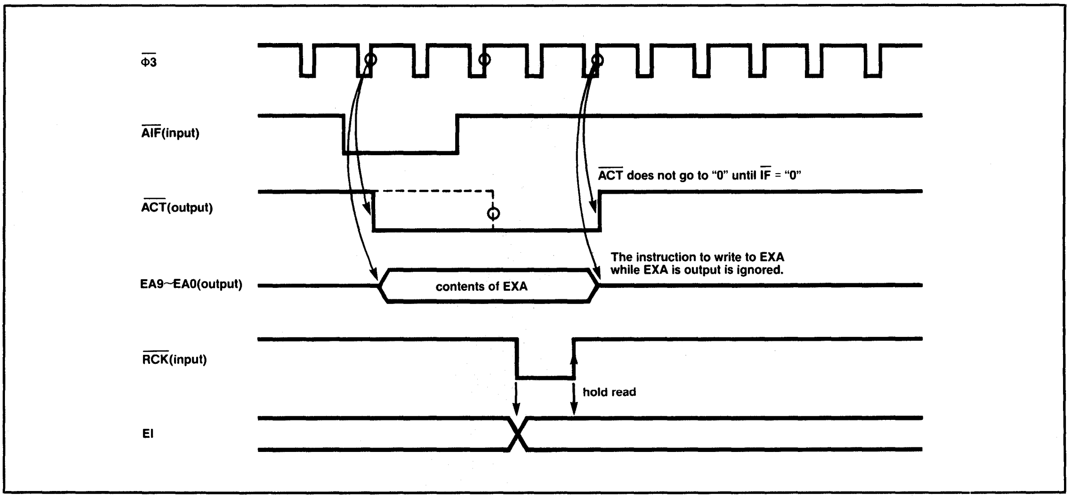
The MB87064 outputs the contents of PGM and DPE when ERAM is being accessed and outputs the contents of EXA when the I/O bus is being accessed for data transfer to-or-from an external circuit.

- The contents of EXA Register

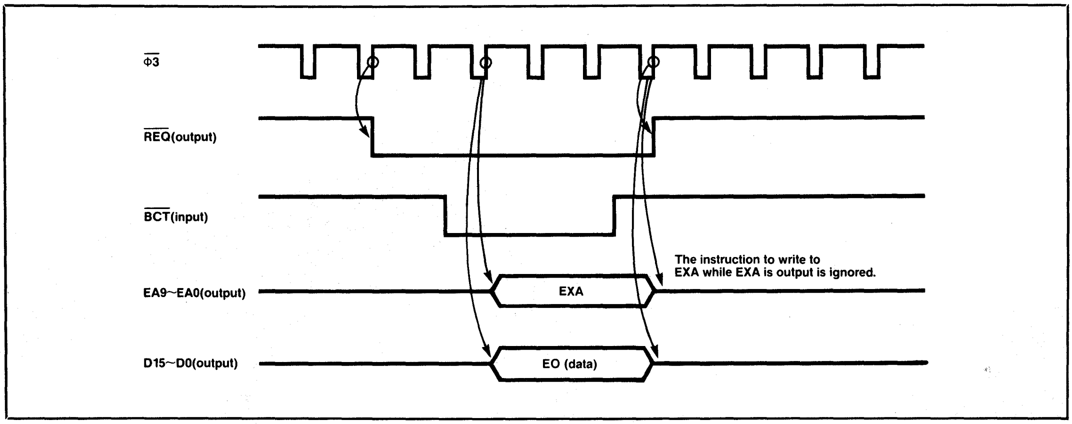


- Timing Specifications
- When ERAM is accessed:
  Same as MB8764 (input/output)
- When I/O bus is accessed:
  See the following timing diagram:

Input (P Mode/D Mode)


Φ3
AIF(input)
ACT does not go to "0" until IF = "0"
ACT(output)
The instruction to write to EXA while EXA is output is ignored.
EA9~EA0(output)
contents of EXA
RCK(input)
hold read
EI

Output (New Mode)



Chip Enable Control Output ($\overline{\text{ECE}}$)

In the MB8764, $\overline{\text{ECE}}$ is always set to "0" (expansion RAM enable state) except when the I/O bus is being accessed for data transfer to-or-from an external circuit. In the MB87064, $\overline{\text{ECE}}$ is set to "0" only when ERAM is being accessed. This modification helps to reduce the power consumption of ERAM.

Hi-Impedance State of EA9 ~ EA0

Pins EA9 ~ EA0 are placed in the high-impedance state when neither ERAM nor I/O bus is accessed. This avoids address bus conflicts when multiple DSPs are used.

Reset Input According to $\overline{\text{FL0}}$ and $\overline{\text{FL1}}$ Status

The Reset signal ($\overline{\text{RST}}$) must be input while $\overline{\text{FL0}}$ and $\overline{\text{FL1}}$ are set to "1". The operation of the reset input flag is the same as the MB8764.

INSTRUCTION SET MODIFICATIONS

The MB87064 has the same instruction set as the MB8764 except for the following modifications to the SET/CLR and MOV instructions.

SET/CLR Instructions

According to ADM flag removal, the following instructions are removed:

SET ADM
CLR ADM

The following instructions are added:

SET ESS	CLR ESS
SET TRC	CLR TRC
SET PCT	CLR PCT

Object code of SET instruction

MSB LSB

1	1	1	0	1	0	0	0	0	0	0	0	0			0	0			0				
													a	b			c	d		e	f	g	h

a	b	c	d	e	f	g	h	set register	
1	0	0	0	0	0	0	0	DMM	
0	1	0	0	0	0	0	0	PCT	← new
0	0	1	0	0	0	0	0	VS	
0	0	0	1	0	0	0	0	ESS	← new
0	0	0	0	1	0	0	0	CLP	
0	0	0	0	0	1	0	0	TRC	← new

Object code of CLR instruction

MSB LSB

1	1	1	0	0																			
					a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s

a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	cleared register	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F1	
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DMC	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	B	
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Y	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	DMM	
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	PCT	← new
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	IF	
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	OF	
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	VS	
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	ESS	← new
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	OV	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	CLP	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	TRC	← new

- multiple registers can be specified
- execution cycle: one

MOV Instruction

According to the EXA register addition, the destination of EXA register is added to the following MOV instruction:

```
MOV[:arithmetic/logic operation]$a(8)[([Y][E])],Reg[:Reg[:...]...]
```

machine code

MSB LSB

0	1	0	0	← c →	← t →	E	Y	← a →

a: RAM address c: operation
t: destination

t						destination register	
1	0	0	0	0	0	EO	
0	1	0	0	0	0	A	
0	0	1	0	0	0	B	
0	0	0	1	0	0	D	
0	0	0	0	1	0	EXA (lower 10 bits of RAM data)	← new

- Two or more destination registers can be selected at once.

MOV Instruction (Cont.)

- An arithmetic/logic operation cannot be performed when the destination register is D.

According to EXA register addition, the processing of "d → EXA" is added.

MOV #$d,Reg

machine code

MSB LSB

1	1	1	1	t	1	d

t			processing	mnemonic	
0	0	0	d → EO	MOV #$d,EO	
0	0	1	output instruction	MOV #$d,EA(Note)	
0	1	0	d → D	MOV #$d,D	
0	1	1	d → B	MOV #$d,B	
1	0	1	d(lower ten bits) → EXA	MOV #$d,EXA	← new

Note:
Though the EA register does not exist, this instruction does exist in the MB87064 to maintain compatibility of output instruction with MB8764. This instruction is only effective as an output instruction and the processing of "d → EA" is ignored.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage	V_{CC}	-0.3[2]	6.0	V
Input Voltage	V_I	-0.3[2]	V_{CC} + 0.3[2]	V
Output Voltage	V_O	-0.3[2]	V_{CC} + 0.3[2]	V
Operating Temperature	T_{OP}	-40	85	°C
Storage Temperature	T_{STG}	-55	150	°C

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This value applies for a steady-state condition. The incremental voltage can be increased to a value of 0.5V for periods not to exceed 20-to-30 nanoseconds.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_{OP}	-40		85	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise specified.)

Operating Temperature Range = 0°C to 70°C

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input High Voltage	V_{IH}	Other than CK1, CK2	2.2		V_{CC} + 0.3	V
	V_{IHCK}	CK1, CK2	4.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	Other than CK1, CK2	-0.3		0.8	V
	V_{ILCK}	CK1, CK2	-0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	2.7		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0		0.4	V
Input Leakage Current	I_{LI}	V_I = 0 to 5.5V	-10		10	μA
Input Leakage Current (Three-state Pin Input)	I_{LZ}	V_I = 0 to 5.5V	-20		20	μA
Static Power Supply Current	I_{CCS}			10		μA
Power Supply Current	I_{CC}	f_{OP} = 8MHz		50		mA

Operating Temperature Range = -40°C to 85°C

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input High Voltage	V_{IH}	Other than CK1, CK2	2.8		V_{CC} + 0.3	V
	V_{IHCK}	CK1, CK2	4.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	Other than CK1, CK2	-0.3		0.8	V
	V_{ILCK}	CK1, CK2	-0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	2.7		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0		0.4	V
Input Leakage Current	I_{LI}	V_I = 0 to 5.5V	-25		25	μA
Input Leakage Current (Three-state Pin Input)	I_{LZ}	V_I = 0 to 5.5V	-40		40	μA
Static Power Supply Current	I_{CCS}			50		μA
Power Supply Current	I_{CC}	f_{OP} = 8MHz		60		mA

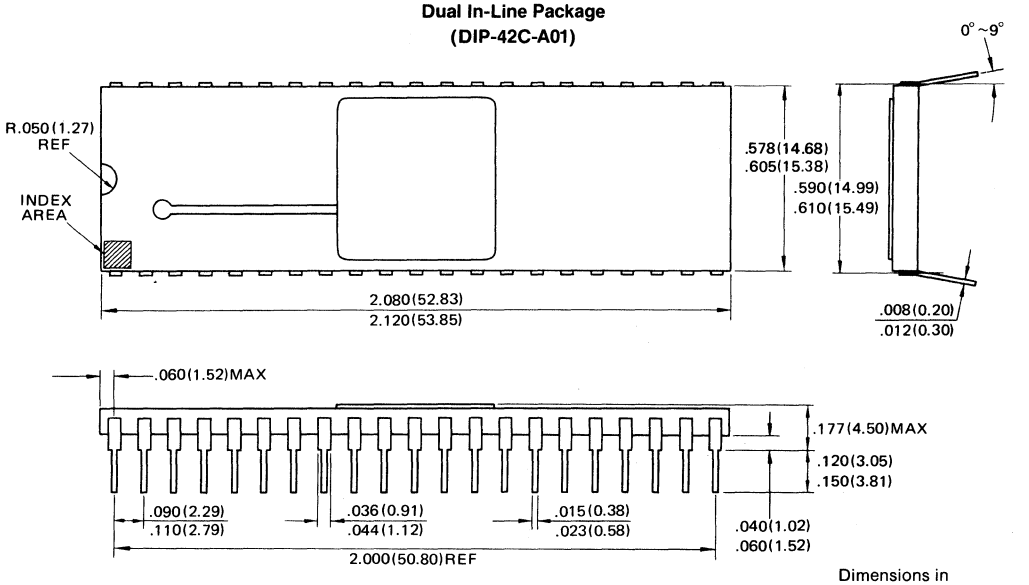
INPUT/OUTPUT CAPACITANCE

(V_{CC} = V_I = 0V, f_{OP} = 8MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Pin	C_{IN}			6	pF
Output Pin	C_{OUT}			6	pF
I/O Pin	$C_{I/O}$			8	pF

Package Dimension

42-Lead Ceramic Multi
Dual In-Line Package
(DIP-42C-A01)



Dimensions in
inches (millimeters)

FUJITSU

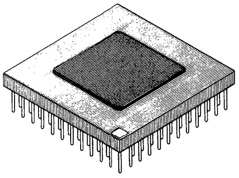
ADPCM DIGITAL SIGNAL PROCESSOR

MB87067 MB87068

April 1986
Edition 1.0

DESCRIPTION

The Fujitsu MB87067/MB87068 Digital Signal Processor (DSP) consists of two MB8764 DSPs each with an applications-specific program in the internal ROM. Together, the MB87067/MB87068 chip set provides all coding/decoding functions required to process Adaptive Pulse Code Modulation (ADPCM) signals. The MB87067 provides the encoding function and the MB87068 provides the decoding function. Under direction of the ADPCM programs stored in the two devices, the chip set allows the user to implement a CCITT standard ADPCM CODEC without any program development work. For complete electrical characteristics and functional detail of the MB8764 DSP, the user should refer to the current data sheet and, for additional DSP support, contact the nearest Sales Office of Fujitsu.



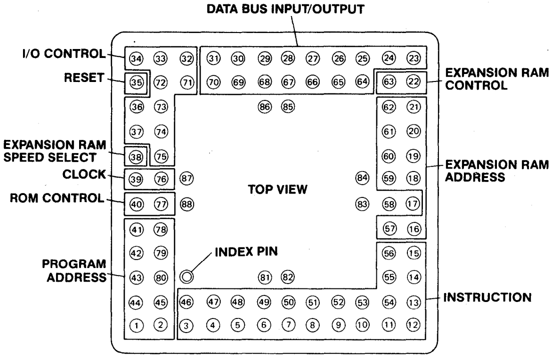
Ceramic Package
RIT-88C-A01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- High-performance design based on MB8764 DSP (Same electrical and timing specifications.)
- CCITT standard ADPCM coding/decoding (Selectable μ-law/A-law PCM).
- MB87067 provides u-law PCM bit-steal function: 7-bit decode function and bit-steal receiving function.
- ADPCM bit-steal function with transmit/receive signaling.
- TTL interface.
- Silicon gate CMOS fabrication process.
- Single 5-volt power supply.
- 88-pin grid array (PGA) package.

PIN ASSIGNMENTS



No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	PA1	16	EA0	31	D14	46	P23	61	EA7	76	CK2
2	PA0	17	—	32	$\overline{REQ}$	47	P21	62	EA9	77	TST
3	P22	18	EA3	33	$\overline{BCT}$	48	P18	63	$\overline{ECE}$	78	PA9
4	P20	19	EA5	34	$\overline{RCK}$	49	P16	64	D2	79	PA6
5	P19	20	EA6	35	$\overline{RST}$	50	P15	65	D4	80	PA4
6	P17	21	EA8	36	$\overline{FL0}$	51	P13	66	D7	81	GND
7	P14	22	$\overline{EWE}$	37	$\overline{WCK}$	52	P10	67	D9	82	VCC
8	P12	23	D0	38	ESS	53	P8	68	D10	83	VCC
9	P11	24	D1	39	CK1	54	P6	69	D12	84	GND
10	P9	25	D3	40	IRM	55	P3	70	D15	85	GND
11	P7	26	D5	41	PA8	56	P1	71	$\overline{ACT}$	86	VCC
12	P5	27	D6	42	PA7	57	EA1	72	$\overline{AIF}$	87	VCC
13	P4	28	D8	43	PA5	58	—	73	$\overline{FL1}$	88	GND
14	P2	29	D11	44	PA3	59	EA2	74	$\overline{AOF}$		
15	P0	30	D13	45	PA2	60	EA4	75	$\overline{ASL}$		

PIN DESCRIPTIONS

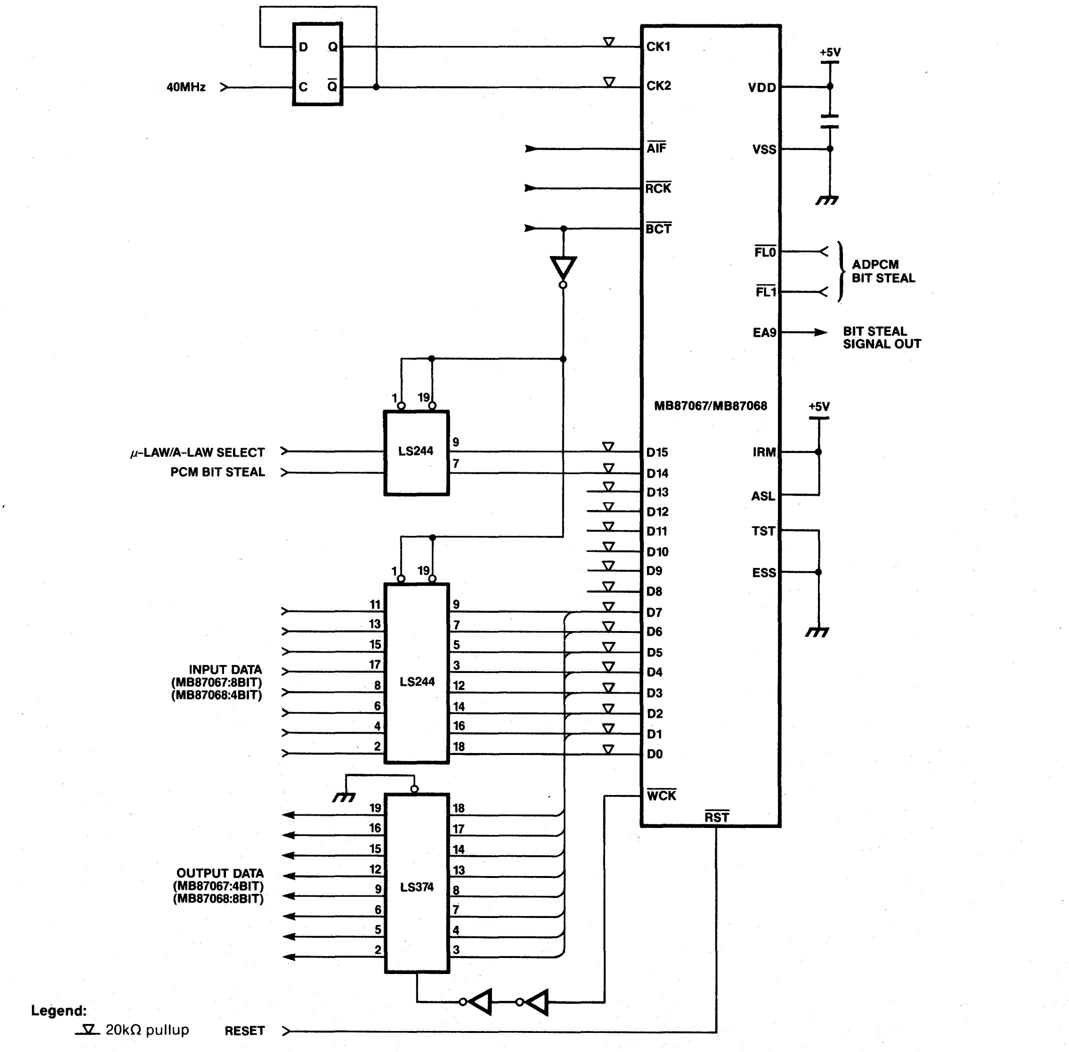
Pin No.	Designator	Function	MB87067	MB87068
70	D15	Data Bus MSB	μ-law/A-law select	
31	D14	Data Bus BIT14	7-bit coding select	*/*
30	D13	Data Bus BIT13	*/*	*/*
69	D12	Data Bus BIT12	*/*	*/*
29	D11	Data Bus BIT11	*/*	*/*
68	D10	Data Bus BIT10	*/*	*/*
67	D9	Data Bus BIT9	*/*	*/*
28	D8	Data Bus BIT8	*/*	*/*
66	D7	Data Bus BIT7	PCM in/ *	* / PCM out
27	D6	Data Bus BIT6	PCM in/ *	* / PCM out
26	D5	Data Bus BIT5	PCM in/ *	* / PCM out
65	D4	Data Bus BIT4	PCM in/ *	* / PCM out
25	D3	Data Bus BIT3	PCM in/ADPCM out	ADPCM in/ PCM out
64	D2	Data Bus BIT2	PCM in/ADPCM out	ADPCM in/ PCM out
24	D1	Data Bus BIT1	PCM in/ADPCM out	ADPCM in/ PCM out
23	D0	Data Bus LSB	PCM in/ADPCM out	ADPCM in/ PCM out
34	$\overline{\text{RCK}}$	Data read clock		
33	$\overline{\text{BCT}}$	Data bus output enable	Control signal	
72	$\overline{\text{AIF}}$	Data input request		
37	$\overline{\text{WCK}}$	Data write clock		
74	$\overline{\text{AOF}}$	Output data type specification		
71	$\overline{\text{ACT}}$	Input enable		
62	EA9	Expansion RAM address MSB	PCM bit steal out	ADPCM bit steal out
36	$\overline{\text{FL0}}$	Flag input	Signaling input	Set to "1"
73	$\overline{\text{FL1}}$	Flag input	Signaling on/off	
35	$\overline{\text{RST}}$	Initialization	Reset	
39	CK1	Master clock input pin 1	20MHz clock	
76	CK2	Master clock input pin 2	20MHz clock	
40	IRM	Internal/External ROM switching	Set to "1"	
77	TST	Internal ROM test mode	Set to "0"	
75	$\overline{\text{ASL}}$	Data output type specification	Set to "1"	
38	ESS	ERAM speed select	Set to "0"	
22	$\overline{\text{EWE}}$	ERAM write clock	NC	
63	$\overline{\text{ECE}}$	ERAM chip enable	NC	
32	$\overline{\text{REQ}}$	Data bus request	NC	

Legend:
*Unused pin

6

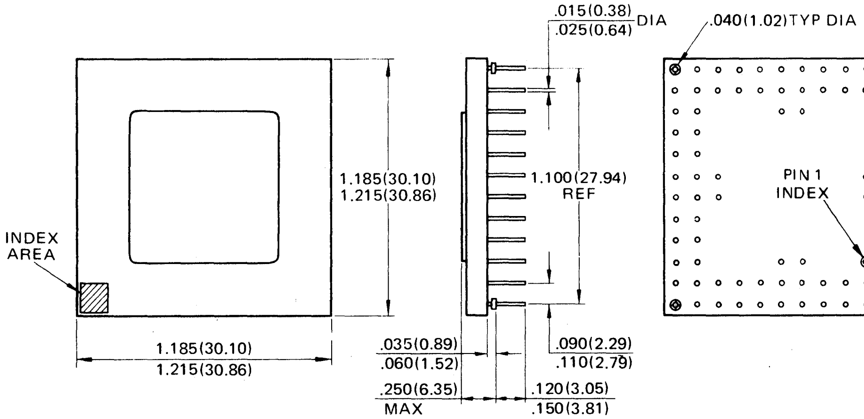
APPLICATIONS

Typical Coding/Decoding Configuration



PACKAGE DIMENSIONS

88-Lead Ceramic (Metal Seal)
Repeated Quad In-Line Package
RIT-88C-A01



Dimensions in
inches (millimeters)

FUJITSU

SERIAL INTERFACE ADAPTER (SIA)

MB87069

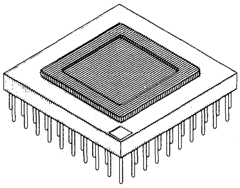
April 1986
Edition 1.0

DESCRIPTION

The Fujitsu MB87069 is a dedicated Serial Interface Adapter (SIA) that provides cost-effective interface support between the Fujitsu MB8764 Digital Signal Processor (DSP), PCM CODECs, and general purpose microprocessors. Some interface examples are shown later in this document.

FEATURES

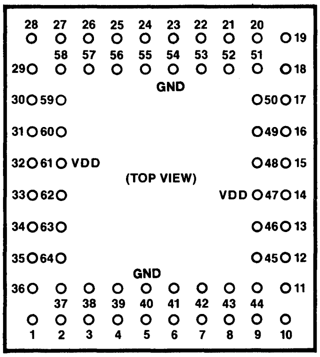
- Supports MB8764 for interface of PCM CODEC and microprocessor
- Serial I/O functions (dual input/output lines)
- Conversion circuits for μ-law/A-law data to linear data and vice-versa
- Interface circuit for microprocessor
- Software-controlled operations from MB8764 or microprocessor
- Silicon-gate CMOS process
- 64-pin Pin Grid Array (PGA) package



PGA-64C-A02

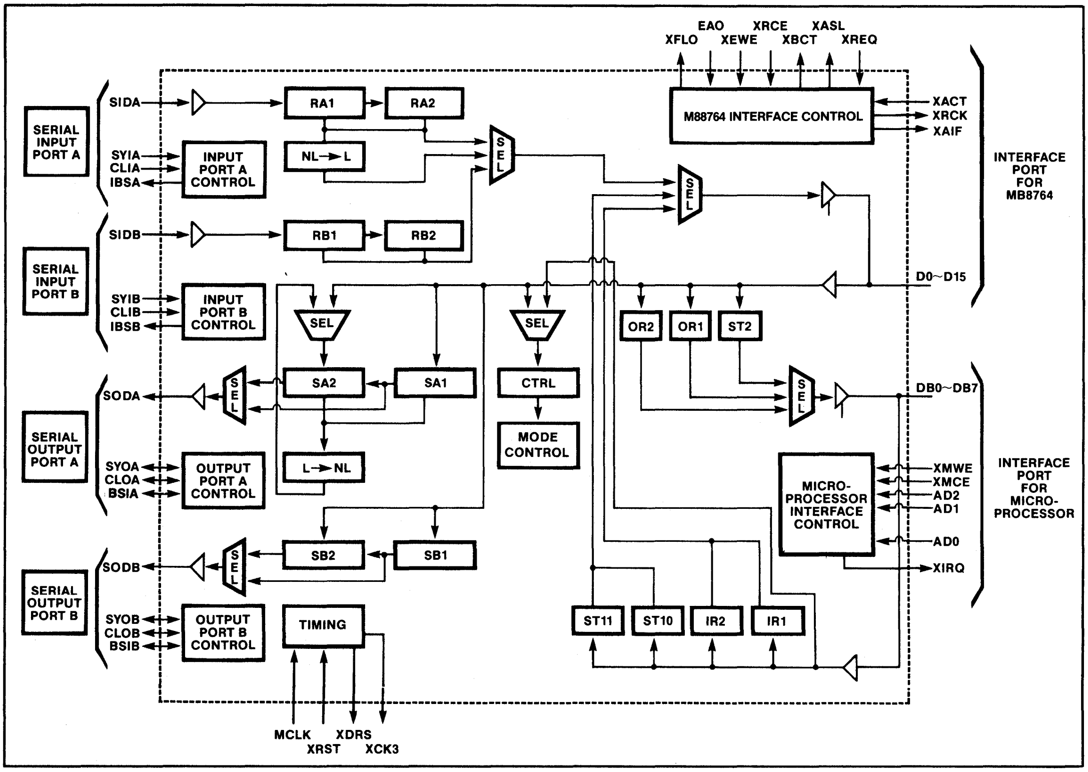
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENTS



Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	Output	XBCT	17	I/O	CLOB	33	Output	XCK3	49	Input	BSIA
2	Output	XAIF	18	I/O	SYOB	34	Output	XASL	50	Output	SODB
3	Input	XACT	19	Input	BSIB	35	Output	XFLO	51	Input	AD2
4	I/O	D15	20	Input	AD1	36	Output	XRCK	52	Input	XMCE
5	I/O	D12	21	Input	AD0	37	Inut	XREQ	53	Input	XMWE
6	I/O	D11	22	I/O	DB7	38	I/O	D14	54	—	GND
7	I/O	D8	23	I/O	DB6	39	I/O	D13	55	I/O	DB4
8	I/O	D6	24	I/O	DB5	40	—	GND	56	I/O	DB2
9	I/O	D5	25	I/O	DB3	41	I/O	D10	57	I/O	DB0
10	I/O	D3	26	I/O	DB1	42	I/O	D9	58	Input	SIDB
11	I/O	D2	27	Output	XIRQ	43	I/O	D7	59	Output	IBSA
12	I/O	D0	28	Output	IBSB	44	I/O	D4	60	Input	SIDA
13	Input	XEWE	29	Input	SYIB	45	I/O	D1	61	—	VCC
14	Input	EA0	30	Input	CLIB	46	Input	XRCE	62	Input	MCLK
15	I/O	SYOA	31	Input	CLIA	47	—	VCC	63	Input	XRST
16	I/O	CLOA	32	Input	SYIA	48	Output	SODA	64	Output	XDRS

BLOCK DIAGRAM



BLOCK ANALYSIS

Registers RA1 and RA2

These two 8-bit shift registers generate parallel data input from serial input port A. Register RA2 is only used for 16-bit inputs; the lower 8 bits are stored in RA1 and the upper 8 bits are stored in RA2.

Registers RB1 and RB2

These two registers perform the same function for serial input port B as RA1 and RA2 perform for port A.

Non-Linear to Linear Converter (NL → L)

Converts μ-law/A-law data to linear data.

Registers SA1 and SA2

When data is received from the MB8764, these registers perform a parallel-to-serial conversion and transfer the data to serial input port A. Register SA2 is only used for 16-bit data; in this case, the lower 8 bits are stored in SA1 and the upper 8 bits are stored in SA2.

Registers SB1 and SB2

These two registers perform the same function for serial input port B as SA1 and SA2 perform for port A.

Linear to Non-Linear Converter (L → NL)

Converts linear data to μ-law/A-law data.

Registers IR1 and IR2

Buffer interface registers for MB8764.

Registers OR1 and OR2

These two interface registers are used when data is transferred from the MB8764 DSP to the microprocessor.

Registers ST2, ST10, and ST11

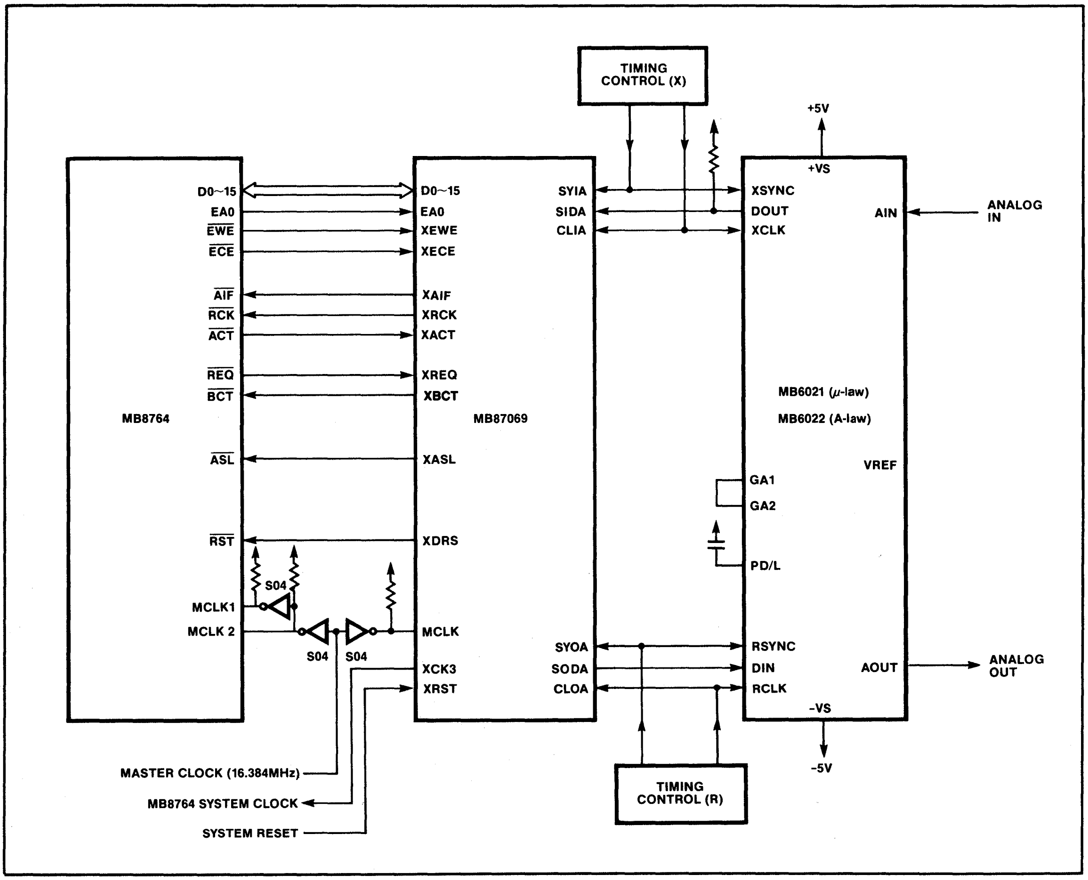
These registers perform handshake interface functions between the microprocessor and the SIA.

Control (CTRL) Register

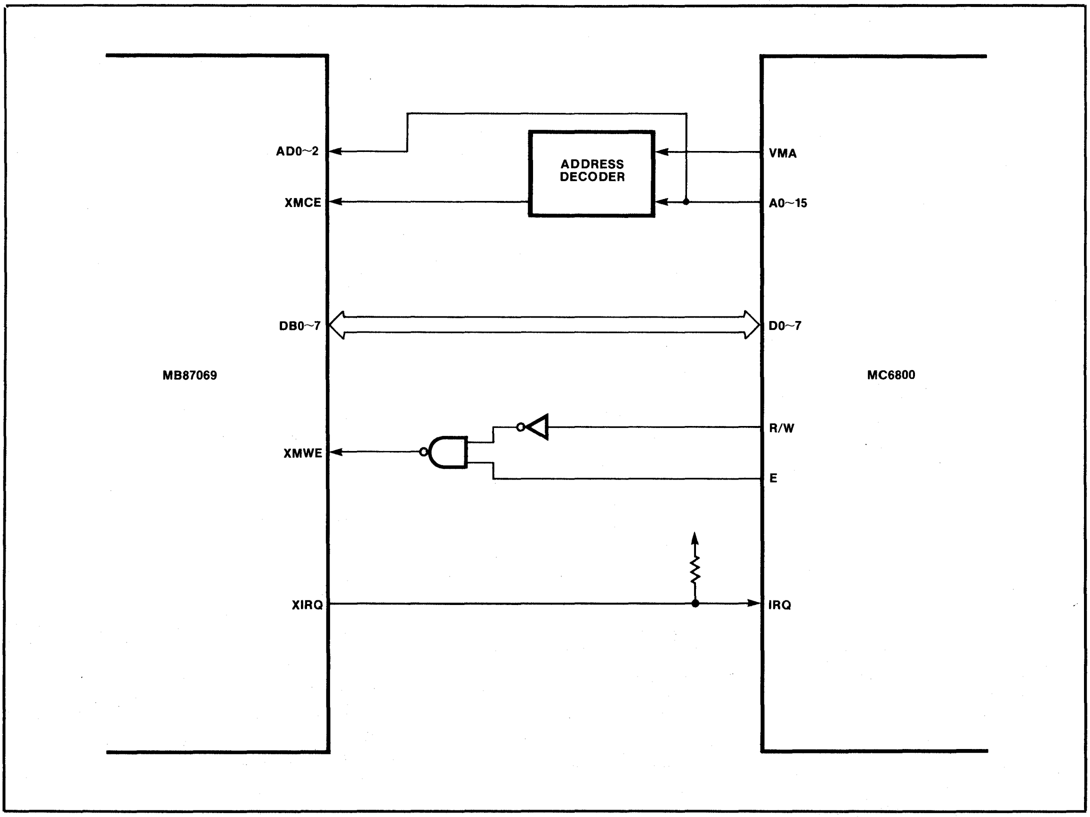
This register specifies the operating mode of the SIA.

TYPICAL APPLICATIONS

Interface Between MB8764 (DSP) and MB6021/22 (CODEC) With MB87069 (SIA)

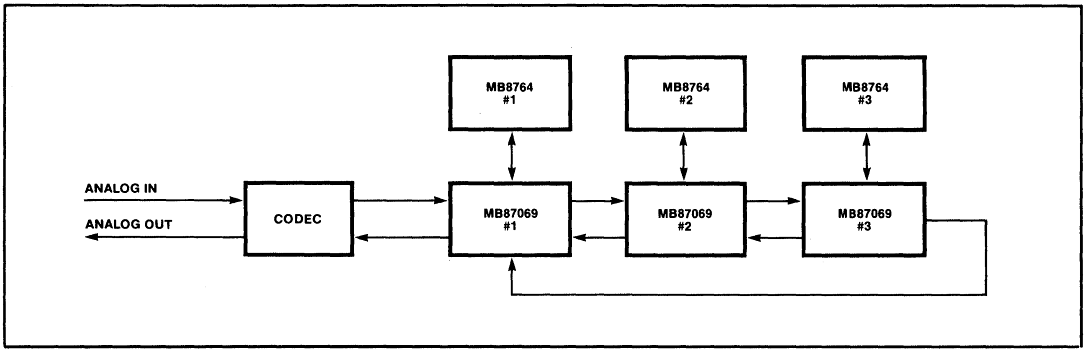


Interface Between MB87069 and Microprocessor (MC6800)

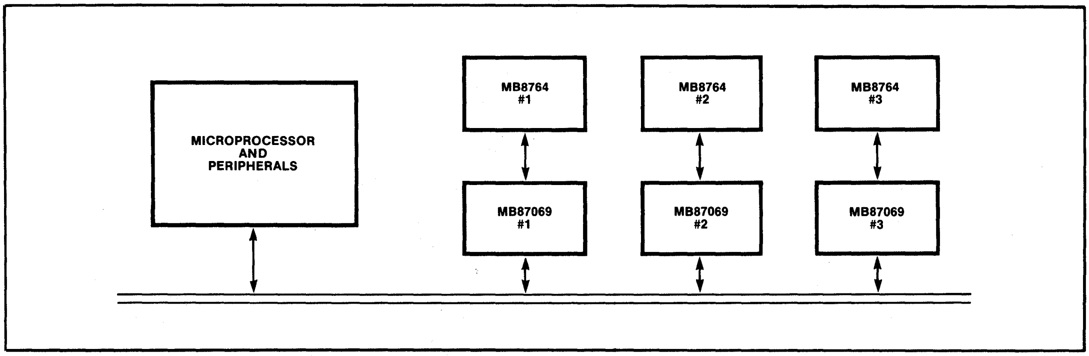


SYSTEM CONFIGURATIONS

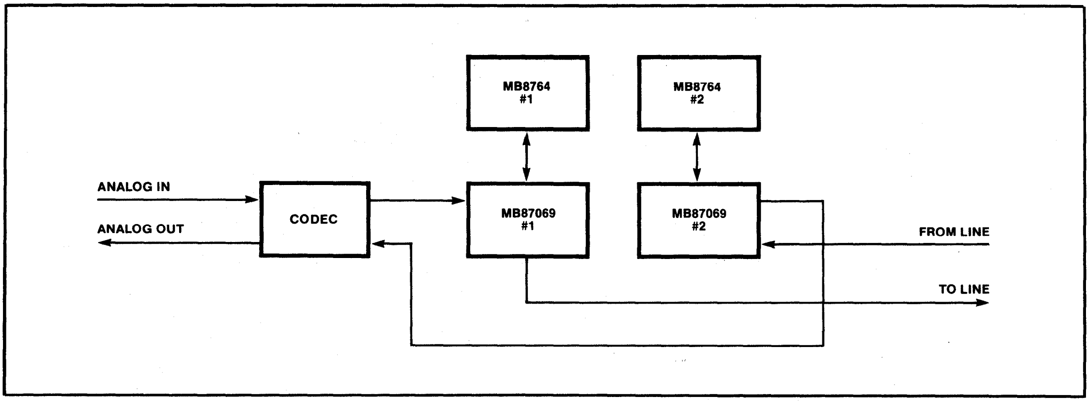
Echo Canceller



Microprocessor Interface Circuit

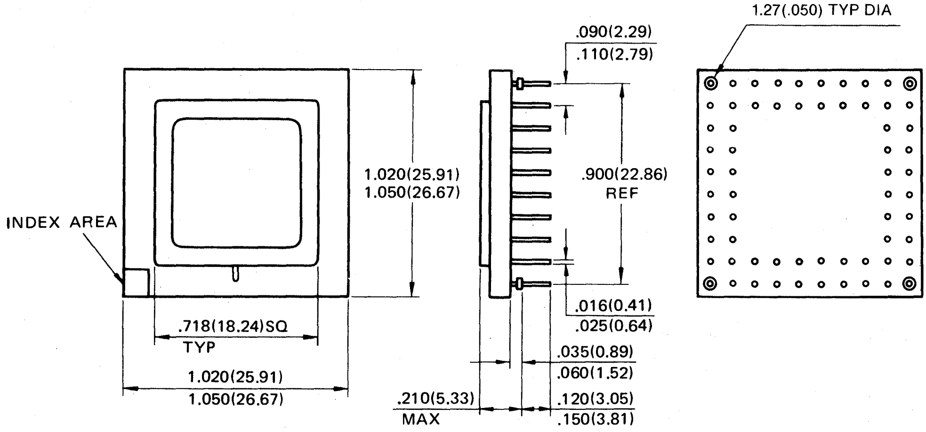


32 kbps ADPCM CODEC



PACKAGE DIMENSIONS

64 Lead Ceramic (Metal Seal) Repeated Quad In-Line Package PGA-64C-A02



Dimensions in
inches (millimeters)

Section 7

ROM Code Development Procedure

FUJITSU

ROM Code Development

4-Bit/8-Bit Microcomputers

ROM CODE DEVELOPMENT

All 4-bit Microcomputers and some 8-bit microcomputers from Fujitsu are available with a mask ROM; thus, the Customer can develop a proprietary system that is efficient and very cost-effective. The ROM can be submitted in the form of an EPROM or the Customer can submit the device actually used to develop the code (MBL8742, MBL8749H, or equivalent). The code submittal must be accompanied by a Data Release Form that specifies mask options, package markings, delivery expectations, production quantities, and other relevant data.

The submitted code is processed by Fujitsu and returned to the Customer in the form of an EPROM for code verification. Before code submittal, the Customer can choose either of two options.

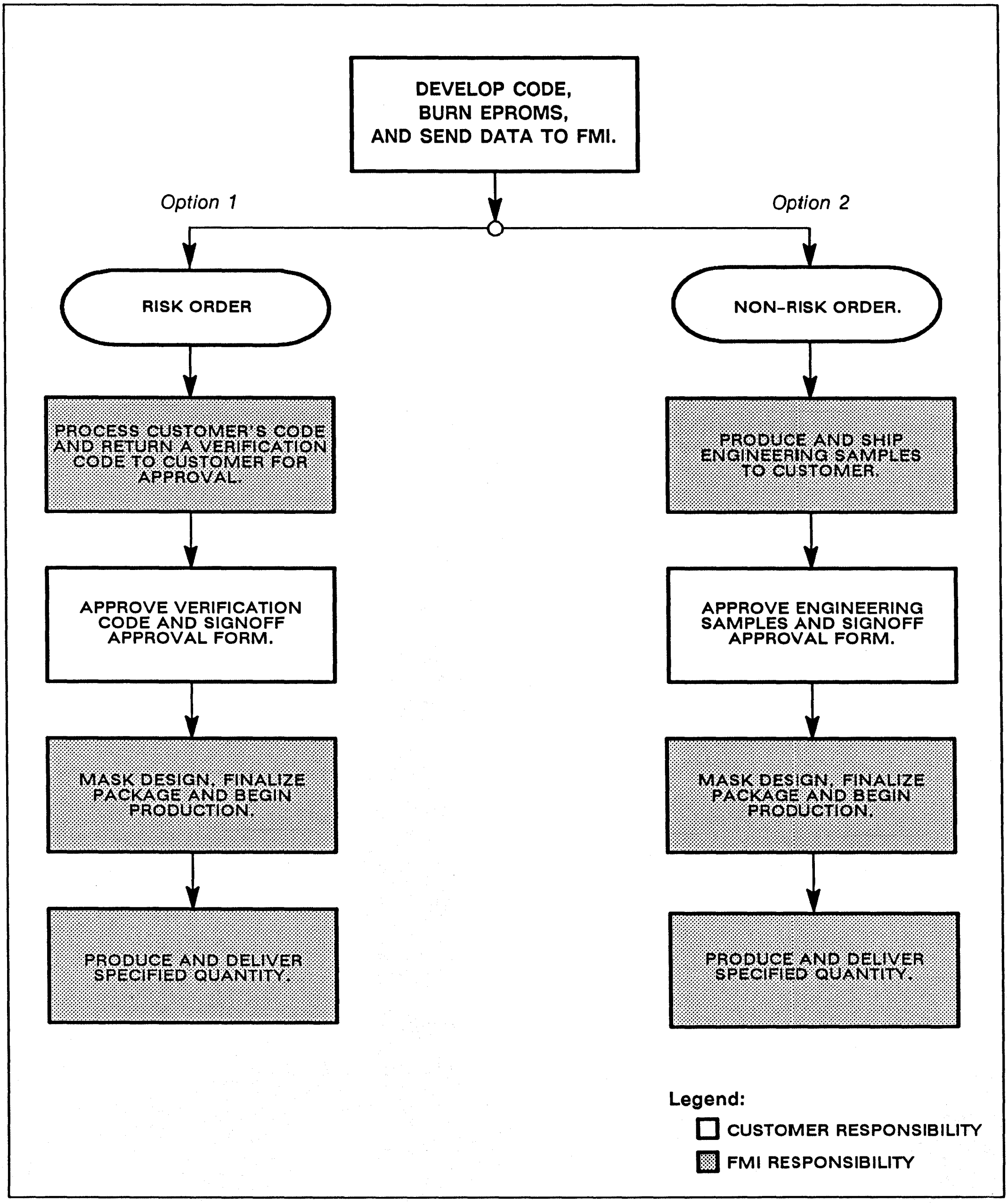
Option 1: If there is absolute certainty that the code is accurate and there will be no changes, the Customer can commit the code to production. In this case, Fujitsu will design the mask, finalize the package specifications, and produce the part in production quantities. As shown in the ROM Code Development Flowchart, the Customer assumes all risks for accuracy of code supplied to Fujitsu.

Option 2: After code verification, the Customer may choose to wait for engineering samples before committing the code to production assuring Customer control of production device configuration. However, the wait for production parts is extended.

For simple codes or for those with minor deviations from working samples, a risk order may be justified. Likewise, if tried-and-proven codes are being processed by Fujitsu to save time or money, a risk order will expedite production. For design prototypes or for systems with complex control features, the non-risk order is recommended.

The Customer should review the following flowchart and become familiar with ROM-code development procedures. All required code-development forms are available at Fujitsu Sales Offices or the Customer can simply contact the FMI Sales Representative for additional information.

FLOWCHART OF ROM CODE DEVELOPMENT


DEVELOP CODE,
BURN EPROMS,
AND SEND DATA TO FMI.
Option 1
Option 2
RISK ORDER
NON-RISK ORDER.
PROCESS CUSTOMER'S CODE AND RETURN A VERIFICATION CODE TO CUSTOMER FOR APPROVAL.
PRODUCE AND SHIP ENGINEERING SAMPLES TO CUSTOMER.
APPROVE VERIFICATION CODE AND SIGNOFF APPROVAL FORM.
APPROVE ENGINEERING SAMPLES AND SIGNOFF APPROVAL FORM.
MASK DESIGN, FINALIZE PACKAGE AND BEGIN PRODUCTION.
MASK DESIGN, FINALIZE PACKAGE AND BEGIN PRODUCTION.
PRODUCE AND DELIVER SPECIFIED QUANTITY.
PRODUCE AND DELIVER SPECIFIED QUANTITY.
Legend:
□ CUSTOMER RESPONSIBILITY
▨ FMI RESPONSIBILITY

Section 8

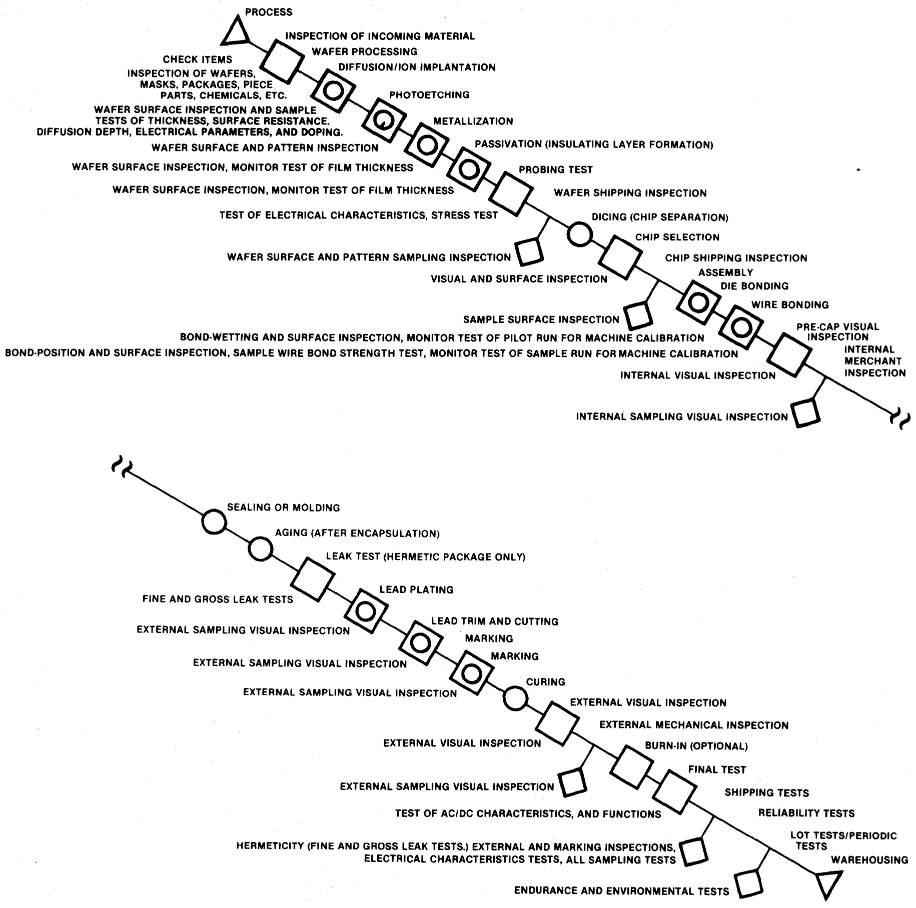
Quality Assurance and Reliability

8

Quality Control at Fujitsu

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The QC process begins with incoming inspection of all raw materials and ends with shipping tests and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology and are ready to serve the Customer in the designated application.

QUALITY CONTROL FLOWCHART


PROCESS
INSPECTION OF INCOMING MATERIAL
CHECK ITEMS
INSPECTION OF WAFERS, MASKS, PACKAGES, PIECE PARTS, CHEMICALS, ETC.
WAFER PROCESSING
DIFFUSION/ION IMPLANTATION
WAFER SURFACE INSPECTION AND SAMPLE TESTS OF THICKNESS, SURFACE RESISTANCE. DIFFUSION DEPTH, ELECTRICAL PARAMETERS, AND DOPING.
PHOTOETCHING
WAFER SURFACE AND PATTERN INSPECTION
METALLIZATION
WAFER SURFACE INSPECTION, MONITOR TEST OF FILM THICKNESS
PASSIVATION (INSULATING LAYER FORMATION)
WAFER SURFACE INSPECTION, MONITOR TEST OF FILM THICKNESS
PROBING TEST
TEST OF ELECTRICAL CHARACTERISTICS, STRESS TEST
WAFER SHIPPING INSPECTION
WAFER SURFACE AND PATTERN SAMPLING INSPECTION
DICING (CHIP SEPARATION)
CHIP SELECTION
VISUAL AND SURFACE INSPECTION
CHIP SHIPPING INSPECTION
SAMPLE SURFACE INSPECTION
ASSEMBLY
DIE BONDING
BOND-WETTING AND SURFACE INSPECTION, MONITOR TEST OF PILOT RUN FOR MACHINE CALIBRATION
WIRE BONDING
BOND-POSITION AND SURFACE INSPECTION, SAMPLE WIRE BOND STRENGTH TEST, MONITOR TEST OF SAMPLE RUN FOR MACHINE CALIBRATION
PRE-CAP VISUAL INSPECTION
INTERNAL VISUAL INSPECTION
INTERNAL MERCHANT INSPECTION
INTERNAL SAMPLING VISUAL INSPECTION
SEALING OR MOLDING
AGING (AFTER ENCAPSULATION)
LEAK TEST (HERMETIC PACKAGE ONLY)
FINE AND GROSS LEAK TESTS
LEAD PLATING
EXTERNAL SAMPLING VISUAL INSPECTION
LEAD TRIM AND CUTTING
MARKING
EXTERNAL SAMPLING VISUAL INSPECTION
MARKING
EXTERNAL SAMPLING VISUAL INSPECTION
CURING
EXTERNAL VISUAL INSPECTION
EXTERNAL MECHANICAL INSPECTION
EXTERNAL VISUAL INSPECTION
BURN-IN (OPTIONAL)
EXTERNAL SAMPLING VISUAL INSPECTION
FINAL TEST
TEST OF AC/DC CHARACTERISTICS, AND FUNCTIONS
SHIPPING TESTS
RELIABILITY TESTS
HERMETICITY (FINE AND GROSS LEAK TESTS.) EXTERNAL AND MARKING INSPECTIONS, ELECTRICAL CHARACTERISTICS TESTS, ALL SAMPLING TESTS
LOT TESTS/PERIODIC TESTS
WAREHOUSING
ENDURANCE AND ENVIRONMENTAL TESTS

Legend:

○ Production process

□ Test/Inspection

⊡ Production process and test/Inspection

◇ QC gate (sampling)

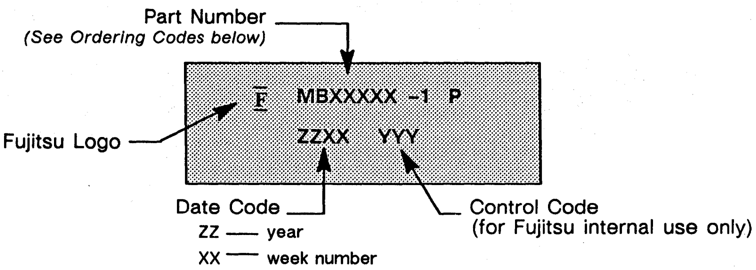
Note:
The flow sequence may vary slightly with individual product type.

Section 9

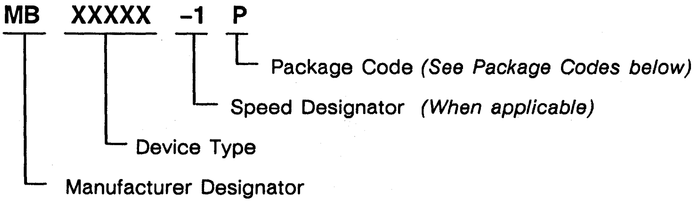
Ordering Information

Ordering Information

Product Marking



Ordering Codes



Package Code *(See Package Codes below)*

Speed Designator *(When applicable)*

Device Type

Manufacturer Designator

MB Device type is Fujitsu Internal Number

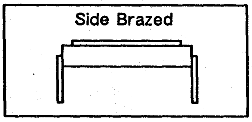
MBL Device type is Second Source

Note: Regarding ordering code, please contact your Fujitsu Sales Office for more information.

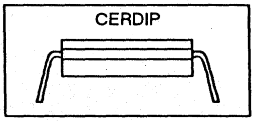
Package Codes

Ceramic		Plastic	
Package Type	*Package Code*	*Package Type*	*Package Code*
LCC (Leaderless Chip Carrier)	CV	LCC (Leaderless Chip Carrier)	PV
PGA (Pin Grid Array)	CR	PGA (Pin Grid Array)	PR
DIP (Side Brazed) [1]	C	DIP (Dual Inline Package)	P
DIP (CERDIP) [2]	Z	Shrink DIP	PSH
Shrink DIP	CSH	Flat	PF
Flat	CF		

1



2



Headquarters Locations

World Headquarters

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Furukawa Sogo Bldg., 6-1
Marunouchi 2-chrome, Chiyoda-ku
Tokyo 100, Japan
Phone National (03) 216-3211
International (Int'l Prefix)
81-3-216-3211
Telex: 2224361 FT TOR J

North/South American Headquarters

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3320 Scott Blvd.
Santa Clara, Ca. 95054-3197
Phone: (408) 562-1000
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FUJITSU SNTA

European Headquarters

Fujitsu Mikroelektronik GmbH
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Lyoner Strabe 44-48 D-6000
Frankfurt 71, F.R. Germany
Phone: 069/66 320
Telex: 0411 963

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Fujitsu Microelectronics FMP
805 Tsim Sha Tsui Centre
West Wing 66
Mody Road, Kowloon
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Phone: 852-3-7320100
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TWX: 910-338-0190

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TWX: (910) 590-8003

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840 Newport Center Drtive
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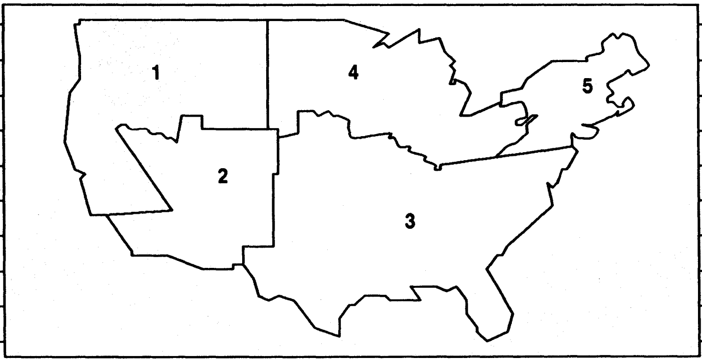
2. (714) 720-9688
3. (214) 669-1616
4. (612) 454-0323
5. (617) 964-7080



Sales Office Locations – Europe

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Fujitsu Mikroelektronik
Bureau de Liaison
Tour Rosny II
93118 Rosny Sous Bois Cedex
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Telex: 41 782

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Telex: 58 068

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Diode
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Avda. de Brasil 5
Madrid 20
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Telex: 42 148

Litton Precision
Condes del Val 8
28030 Madrid
Phone: (1) 250 15 07
Telex: 44 730

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Rabans Close
Aylesbury Bucks
HP 19 3RS
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Hawke
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Sunbury
Midox
TW 16 SDA
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Telex: 9 23 592

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Pipe Thompson Limited
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Ottawa, Ontario K0A 2T0
(613) 258-4067

Pipe Thompson Limited
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